SuperFAP-E^3 Series of 6th Generation MOSFETs

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1. Introduction

With environmental problems drawing attention in recent years, electronic equipment and the switched mode power supplies (SMPS) installed in that equipment are being required to provide greater energy savings and resource conservation. The main challenges to realizing these objectives are achieving lower power consumption through increased efficiency, circuit simplification through a reduced number of components, and lower noise.

In consideration of the above, the power devices used in electronic equipment (including switched mode power supplies) are required to be low-loss, low-noise, damage resistant and easy to use. In particular, since EMI (electromagnetic interference) noise emissions must comply with various legal regulations, it may be obliged to change circuit constants or add filter circuits etc. in the final stage of electronic equipment design, and this may be time consuming for adjustments. Thus, to support the shorter design times of recent electronic equipment there is a growing need for low-noise devices for which EMI noise suppression is easy to implement.

Fuji Electric has a successful track record of combining low drain-source on-resistance and ultra high-speed switching to develop the SuperFAP-G series of low-loss power MOSFETs (metal-oxide-semiconductor field effect transistors) compatible with a drain-source voltage range of 100 to 900 V, and has contributed to realizing higher efficiency in electronic devices.

To satisfy market needs for low-loss, low-noise, damage resistant and easy-to-use power devices, Fuji Electric has recently developed the SuperFAP-E^3 series of 6th generation MOSFETs that balance low-loss characteristics and low noise on high level and successfully combine high performance with ease of use. The characteristics of this new series are described below.

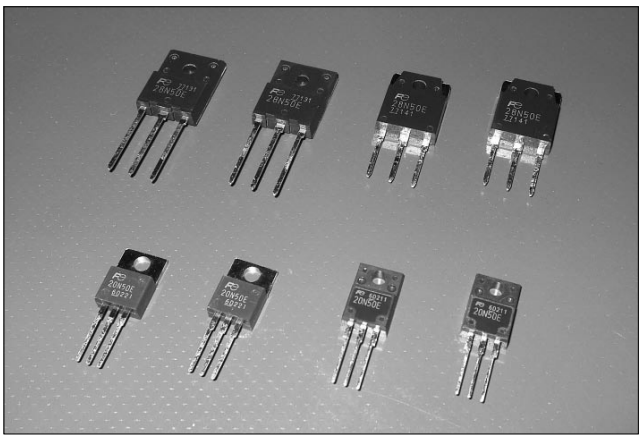
2. Product Overview

Table 1 compares the characteristics of the representative models of the newly developed SuperFAP-E^3 series and conventional devices. The newly developed models realize an approximate 18% improvement in drain-source on-resistance compared to conventional devices of the same chip size, and also realize the industry's top-class of performance as planar type power MOSFETs. Figure 1 shows the external appearance of the SuperFAP-E^3 series devices.

Table 1 Comparison of SuperFAP-E^3 series and conventional device characteristics (comparison for the same chip size)

Series	SuperFAP-E^3 series	SuperFAP-G series (conventional series)
Model	FMA20N50E	2SK3683-01MR
Package	TO-220F	TO-220F
V_{DS}	500 V	500 V
I_D	±20 A	±19 A
P_D	95 W	95 W
$V_{GS\,(th)}$	3±0.5 V	4±1.0 V
$R_{DS\,(on)\,max}$	0.31 Ω	0.38 Ω

Fig.1 External appearance of SuperFAP-E^3 series devices



The SuperFAP-E^3 series includes 500 V and 600 V (drain-source voltage) classes of devices, and the development of devices having a built-in zener diode between the gate and source, and devices having a higher speed parasitic diode are planned for the future. Table 2 lists representative characteristics of models ready for mass-production and model slated for a future product lineup.

Table 2 SuperFAP-E^3 series product list

Drain-source voltage BV_{DSS}	Drain current I_D	Drain-source on-resistance $R_{DS\,(on)}$	Package					Remarks
			TO-220	TO-220F	T-pack (D2-pack)	TO-3P	TO-3PF	
500 V	16 A	0.380 Ω	FMP16N50E	FMA16N50E	FMB16N50E	—	—	In mass-production
	20 A	0.310 Ω	FMP20N50E	FMA20N50E	FMB20N50E	—	—	In mass-production
	7.5 A	0.790 Ω	FMP08N50E	FMA08N50E	FMB08N50E	—	—	In mass-production
	12 A	0.520 Ω	FMP12N50E	FMA12N50E	FMB12N50E	—	—	In mass-production
	23 A	0.245 Ω	—	FMA23N50E	—	FMH23N50E	FMR23N50E	In mass-production
	28 A	0.190 Ω	—	—	—	FMH28N50E	FMR28N50E	In mass-production
600 V	13 A	0.580 Ω	FMP13N60E	FMA13N60E	FMB13N60E	—	—	In mass-production
	16 A	0.470 Ω	FMP16N60E	FMA16N60E	FMB16N60E	—	—	In mass-production
	6 A	1.200 Ω	FMP06N60E	FMA06N60E	FMB06N60E	—	—	In mass-production
	10 A	0.790 Ω	FMP10N60E	FMA10N60E	FMB10N60E	—	—	In mass-production
	19 A	0.365 Ω	—	FMA19N60E	—	FMH19N60E	FMR19N60E	In mass-production
	23 A	0.280 Ω	—	—	—	FMH23N60E	FMR23N60E	In mass-production

3. Design Measures

Requested MOSFET characteristics are summarized in Table 3. Lower loss requires lower on-resistance and lower switching loss. Reducing the gate resistance to suppress the switching loss, however, results in an increase in emission noise. In other words, a tradeoff relation exists between switching loss and emission noise. Moreover, overshoot of the drain voltage is generated when the large current flowing at startup of the power supply is cutoff, and if this overshoot causes avalanche breakdown in the MOSFET, it is important that the MOSFET will not become damaged by the avalanche current. Furthermore, there are also requests for a MOSFET that is easy to use and whose operation is not easily affected by circuit board layouts that change according to the particular electronic equipment design.

Table 3 Market needs of switched mode power supplies and requested characteristics of MOSFETs

Market needs of switched mode power supplies	Requested characteristics of MOSFETs
Low loss and low noise	○ Low on-resistance (combined with high avalanche capability) ○ Design that balances switching loss and emission noise (improved tradeoff)
Damage resistant	○ High avalanche resistance (combined with low on-resistance characteristics)
Easy to use	○ V_{GS} ringing not likely to occur even in the source common wiring is long

3.1 Design of the cellular part

In the conventional SuperFAP-G series, as a result of arranging the p-wells densely and minimizing the spacing between the p-wells, a QPJ (quasi-plane junction) that is analogous to a planar pn junction was utilized. In order to lower the on-resistance even further, a lower resistance wafer must be used, but with the QPJ, sufficient resistance to avalanching could not be ensured when using a lower capability wafer. Thus, to improve the avalanche capability of the newly developed device series based on the conventional QPJ, the p-well width is made narrower, and locations of electric field concentrations are moved from the pn junction at a channel bottom to the bottom surface of a p-well so that the avalanche current flowing into a parasitic bipolar transistor is reduced, and the avalanche capability is aimed to improve. As a result, a wafer having lower resistance than in the SuperFAP-G series may be used while achieving lower on-resistance characteristics and the same high avalanche capability as with the conventional device series. Figure 2 shows the relation between drain-source on-resistance and drain-source breakdown voltage ($R_{DS(on)} - BV_{DSS}$). Figure 2 reveals that $R_{DS(on)}$ has been improved by 18% compared to the conventional device series.

Emission noise is correlated to the switching dv/dt of the drain voltage. Namely, the tradeoff between

switching loss and switching dv/dt must be improved. These characteristics are determined by the ratio of the charge time constant to the gate-drain capacitance (C_{GD}) and the drain-source capacitance (C_{DS}). Figure 3 shows a cross-sectional drawing of the power MOSFET and its equivalent capacitance. C_{GD} is determined by the p-well spacing (gate electrode length) and C_{DS} is determined by the p-well width, and these had to be optimized in the design. In the conventional device series, as a result of the QPJ, low on-resistance characteristics, ultra high-speed switching characteristics and low gate charge (Q_G) characteristics were realized[1]. However, in order to improve the switching loss and switching dv/dt, C_{GD}/C_{DS} had to be made larger than in the conventional device series. But if the p-well spacing is enlarged, electric fields increase in the p-well corner areas, the QPJ state collapses, the breakdown voltage drops and on-resistance characteristics deteriorate. Moreover, higher electric fields in the corner areas lead to the problem of decreased avalanche capability. Thus, in order to maintain the QPJ while improving low on-resistance characteristics and the controllability of switching based on gate resistance, the concentration of the n-substrate in the area facing the gate electrode was optimized, and the p-well spacing was enlarged to mitigate the concentration of electric fields. This improved the ratio of C_{GD}/C_{DS} to approximately twice as big as that of the conventional device series.

Fig.2 $R_{DS(on)} - BV_{DSS}$ characteristics

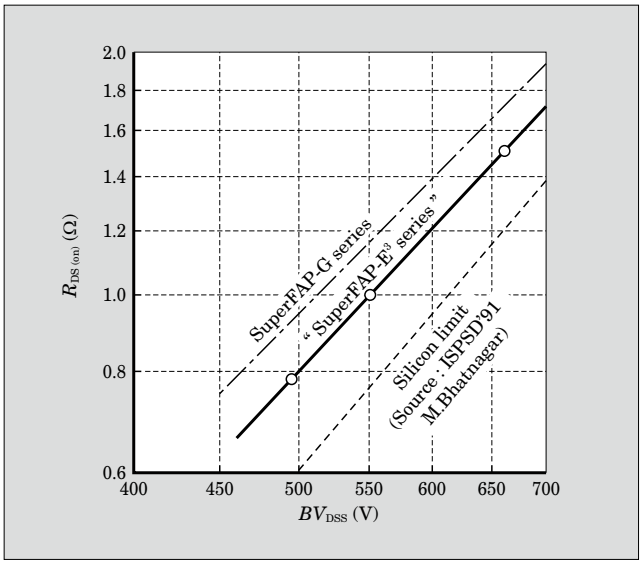
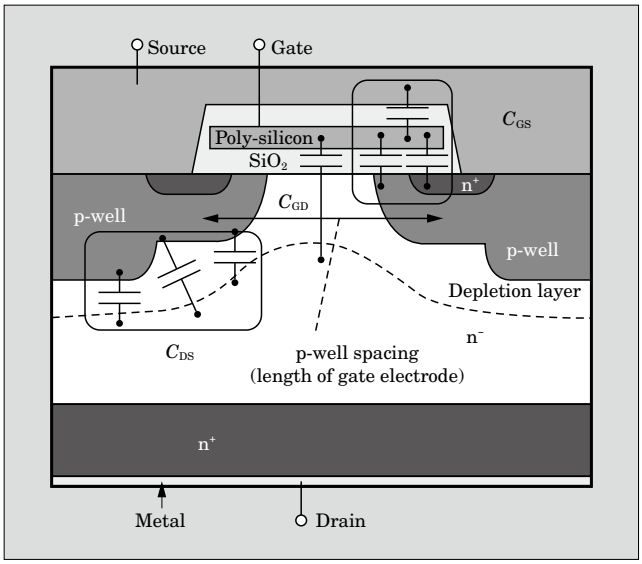


Fig.3 Power MOSFET cross-sectional drawing and equivalent circuit



3.2 Optimized guard-ring technology

With the conventional SuperFAP-G series, in order to mitigate the concentration of electric fields at withstand voltage structures resulting from the use of a low-resistance wafer, an optimized guard-ring structure having non-uniform pitch is used to support the generated withstand voltage close to the silicon limit at the cellular part. In contrast to a field plate structure, this optimized guard-ring is not susceptible to surface charge, and has high reliability, but also has the problem of a long edge length and a poor chip area utilization rate. In the SuperFAP-E^3 series, the guard-ring structure was optimized in order to improve the generated withstand voltage per unit length. Optimization of the guard-ring structure enabled the realization of an edge length of approximately 40% that of the conventional device series, while ensuring high reliability.

4. Effect of the SuperFAP-E^3 and Example Application to Power Supply

The SuperFAP-E^3 series has low loss and high avalanche capability, and an improved tradeoff between emission noise and switching loss. Comparisons between the conventional device series and the SuperFAP-E^3 series are described below.

Fig.4 Temperature rise in offline converter of switched mode power supply for LCD-TV

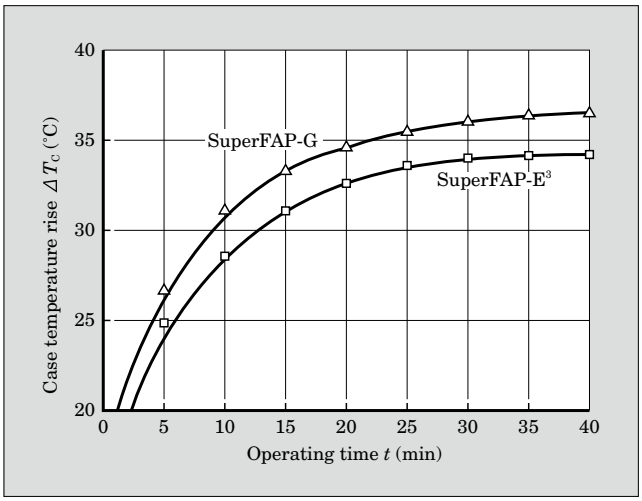


Fig.5 Emission noise – switching loss characteristic (in open frame state)

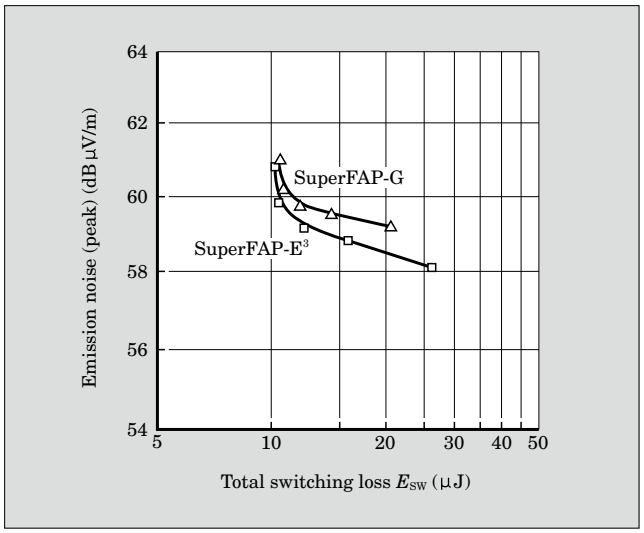


Fig.6 Simulated circuit configuration

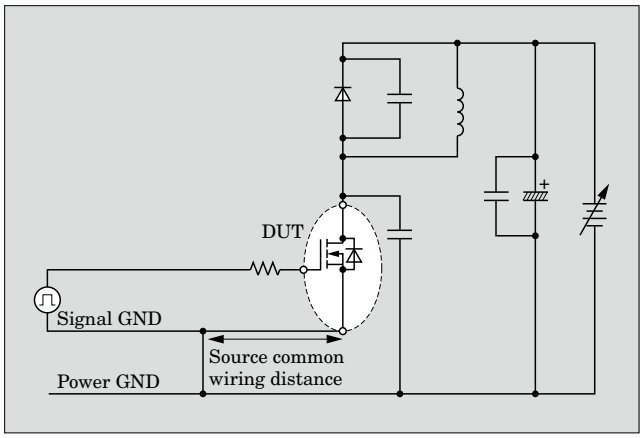
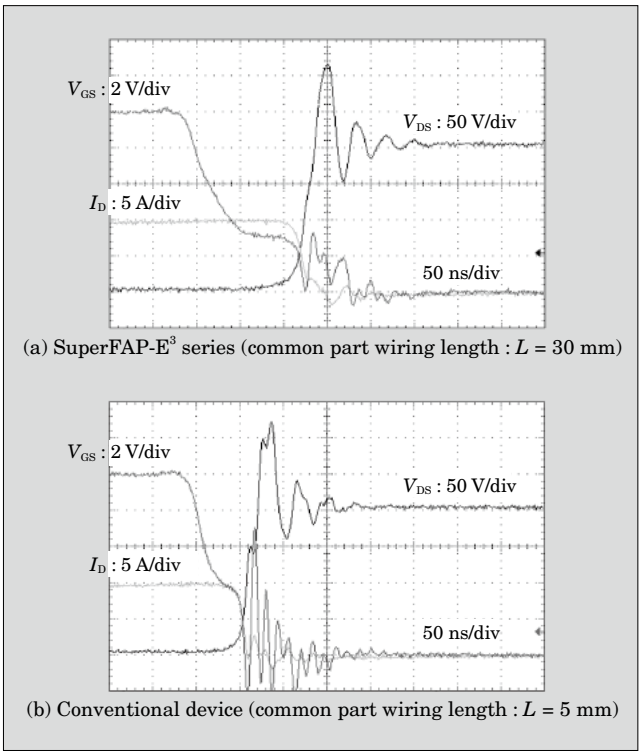


Fig.7 Source common wiring and ringing phenomenon in simulated circuit



4.1 Temperature rise comparison

Figure 4 shows the relationship between conduction time and temperature rise of the device surface in the offline converter of switched mode power supply for LCD-TV. The gate resistance is adjusted to find the appropriate turn-on dv/dt of the drain voltage, which is the drive condition, and the surface temperature of the device is approximately 2 °C lower for the SuperFAP-E^3 series than in the case of the conventional device series.

4.2 Switching characteristics and emission noise verification

Figure 5 shows the relationship between switching loss and emission noise in a typical open frame power supply. Compared to the conventional device series, the SuperFAP-E^3 series has an improved tradeoff relation between switching loss and switching dv/dt of the drain voltage, and exhibits a large change in the level of emission noise in the actual range of gate resistances used in an actual machine, thus improving the controllability of switching dv/dt of the drain voltage by gate resistance.

4.3 V_{GS} ringing comparison

Figure 6 shows the configuration of a simulated circuit and Fig. 7 shows the turn-off waveform of the simulated circuit. With the SuperFAP-E^3 series, even if the source common wiring distance is six times that of the conventional device series, the gate-source voltage (V_{GS}) ringing and waveform distortion will be at the same level or less.

From the above, it is clear that the SuperFAP-E^3 series provides more freedom for the circuit board layout, has a lower incidence rate of mis-operation, and is easier to use than the conventional device series.

5. Postscript

Characteristics of Fuji Electric's newly developed SuperFAP-E^3 series of low-loss and low-noise power MOSFETs have been described above. Fuji Electric intends to expand the product lines of 500 V and 600 V class devices using the newly developed cellular part and optimized guard-ring technology without delay.

Reference

(1) Kobayashi, T. et al. High-Voltage Power MOSFETs Reached Almost to the Silicon Limit. Proceedings of ISPSD'01, 2001, p.435-438.