Innovating Energy Technology

FMH30N60S1

http://www.fujielectric.com/products/semiconductor/ **FUJI POWER MOSFET**

Super J-MOS series

N-Channel enhancement mode power MOSFET

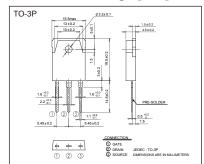
Features

Pb-free lead terminal RoHS compliant

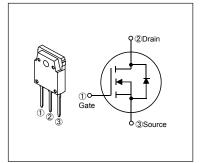
Applications

For switching

Outline Drawings [mm]



Equivalent circuit schematic



■ Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V _{DS}	600	V	
Diani-Source Voltage	V _{DSX}	600	V	V _{GS} =-30V
Outline Park Outline	lo	±30	Α	Tc=25°C Note*1
Continuous Drain Current		±19	Α	Tc=100°C Note*1
Pulsed Drain Current	I _{DP}	±90	Α	
Gate-Source Voltage	V _{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I _{AR}	6.6	Α	Note *2
Non-Repetitive Maximum Avalanche Energy	Eas	849.2	mJ	Note *3
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	kV/μs	V _{DS} ≤ 600V
Peak Diode Recovery dV/dt	dV/dt	12	kV/μs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *5
Maximum Dawar Discination	Б	2.5	W	T _a =25°C
Maximum Power Dissipation	PD	220	VV	Tc=25°C
Operating and Stevens Tomporature range	Tch	150	°C	
Operating and Storage Temperature range	T _{stg}	-55 to +150	°C	

Note *1 : Limited by maximum channel temperature.

Note *2 : T_{ch}≤150°C, See Fig.1 and Fig.2

Note *3 : Starting T_{ch}=25°C, I_{As}=4A, L=97.3mH, V_{DD}=60V, R_G=50Ω, See Fig.1 and Fig.2

E_{AS} limited by maximum channel temperature and avalanche current.

Note *4 : I_F≤-I_D, -di/dt=100A/µs, V_{DD}≤400V, T_{ch}≤150°C.

Note *5 : I_F≤-I_D, dV/dt=12kV/µs, V_{DD}≤400V, T_{ch}≤150°C.

■ Electrical Characteristics at T_c=25°C (unless otherwise specified)

Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V		600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I _D =250µA V _{DS} =V _{GS}		2.5	3.0	3.5	V
Zero Gate Voltage Drain Current los	I _{DSS}	V _{DS} =600V V _{GS} =0V	T _{ch} =25°C	-	-	25	μА
		V _{DS} =480V V _{GS} =0V	T _{ch} =125°C	-	-	250	
Gate-Source Leakage Current	Igss	V _{GS} = ±30V V _{DS} =0V		-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =15A V _{GS} =10V		-	0.106	0.125	Ω
Gate resistance	R _G	f=1MHz, open drain		-	3.2	-	Ω

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• Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	gfs	I _D =15A V _{DS} =25V	13	26	-	S
Input Capacitance	Ciss	V _{DS} =10V	-	2200	-	
Output Capacitance	Coss	V _{GS} =0V	-	4670	-	
Reverse Transfer Capacitance	Crss	f=1MHz	-	430	-	
Effective output capacitance, energy related (Note *6)	C _{o(er)}	V _{GS} =0V V _{DS} =0480V	-	127	-	pF
Effective output capacitance, time related (Note *7)	C _{o(tr)}	V _{cs} =0V V _{cs} =0480V ID=constant	-	450	-	
Turn-On Time	t _{d(on)}	V _{DD} =400V, V _{GS} =10V I _D =15A, R _G =13Ω See Fig.3 and Fig.4	-	31	-	
t _r	tr		-	57	-	no
Turn-Off Time t _d	t _{d(off)}		-	136	-	ns
	t _f		-	17	-	
Total Gate Charge	Q _G	V _{DD} =480V, I _D =30A V _{GS} =10V See Fig.5	-	73	-	
Gate-Source Charge	Q _{GS}		-	18	-	nC
Gate-Drain Charge	Q _{GD}		-	25	-	IIC
Drain-Source crossover Charge	Qsw		-	11.5	-	

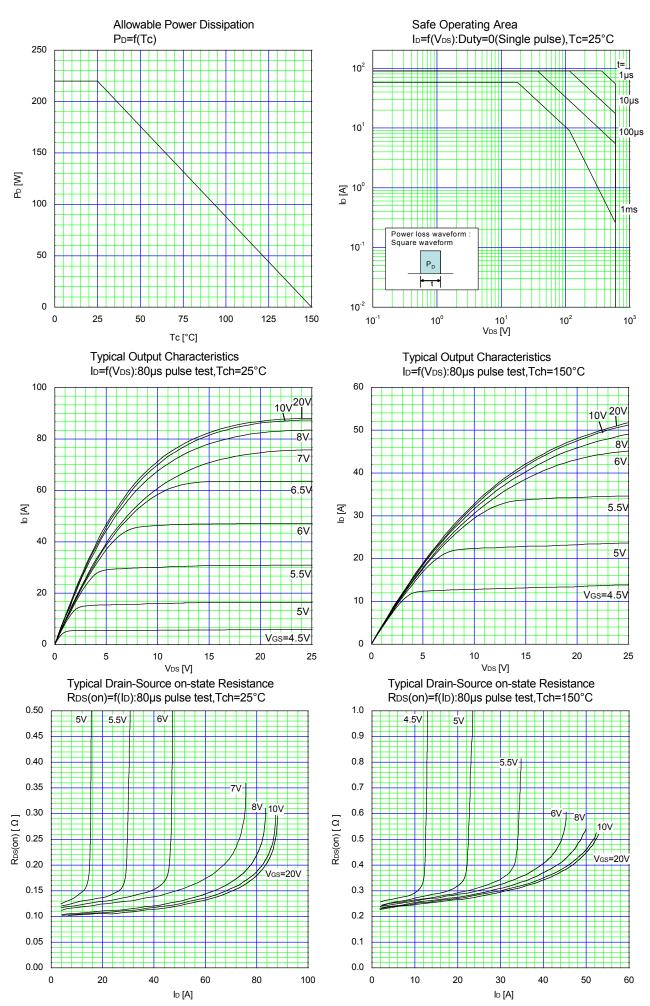
Note *6 : $C_{\text{o(er)}}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}. Note *7 : $C_{\text{o(er)}}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}.

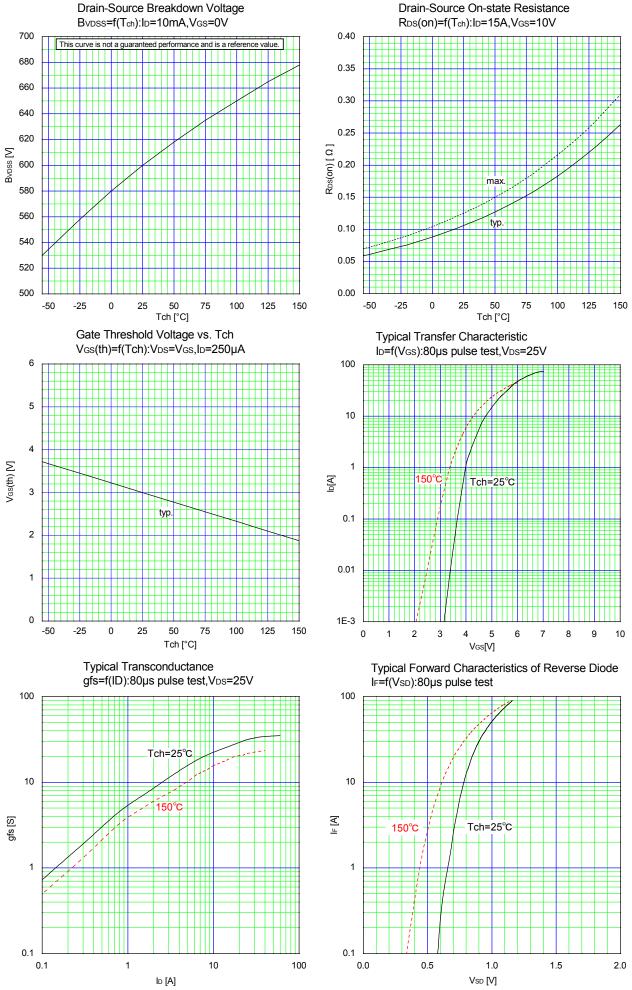
• Reverse Diode

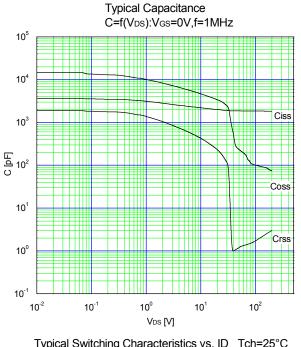
Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	lav	L=21.7mH, T _{ch} =25°C See Fig.1 and Fig.2	6.6	-	-	А
Diode Forward On-Voltage	V _{SD}	I _F =30A, V _{GS} =0V T _{ch} =25°C	-	0.9	1.35	V
Reverse Recovery Time	trr	I _F =30A, V _{cs} =0V V _{DD} =400V -di/dt=100A/μs T _{ch} =25°C See Fig.6	-	430	-	ns
Reverse Recovery Charge	Qrr		-	8.6	-	μC
Peak Reverse Recovery Current	Irp		-	38	-	А

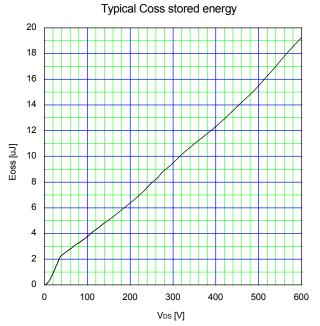
■ Thermal Characteristics

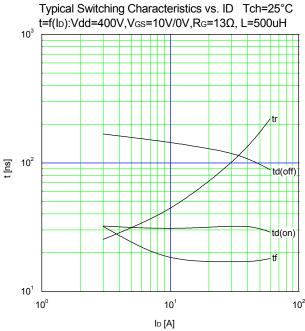
Description	Symbol	min.	typ.	max.	Unit
Channel to Case	R _{th(ch-c)}	-	-	0.57	°C/W
Channel to Ambient	R _{th(ch-a)}	-	-	50	°C/W

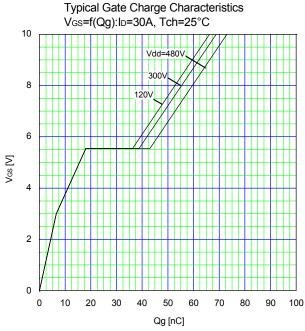


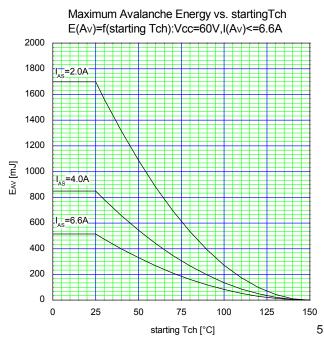


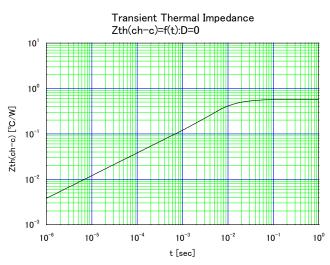












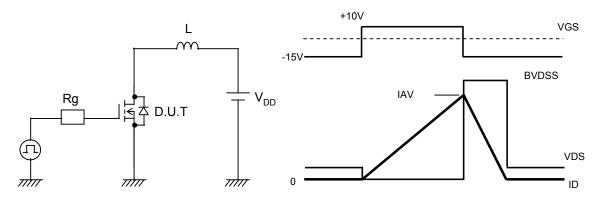


Fig.1 Avalanche Test circuit

Fig.2 Operating waveforms of Avalanche Test

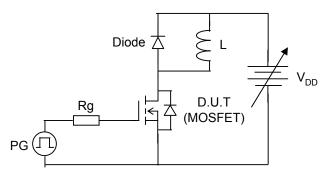


Fig.3 Switching Test circuit

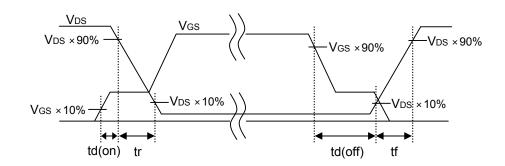


Fig.4 Operating waveform of Switching Test

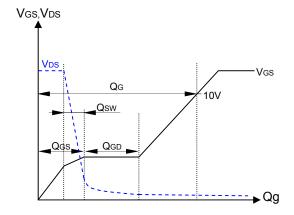


Fig.5 Operating waveform of Gate charge Test

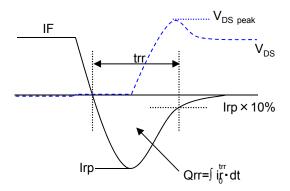
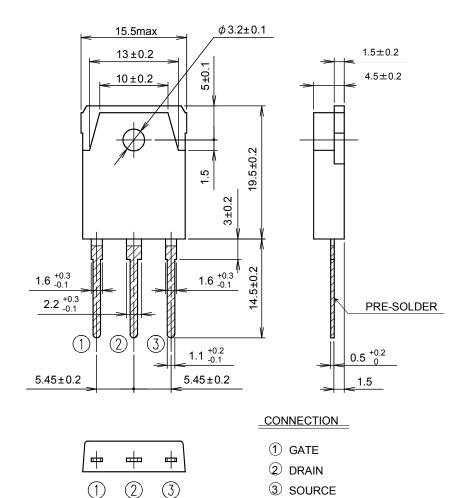


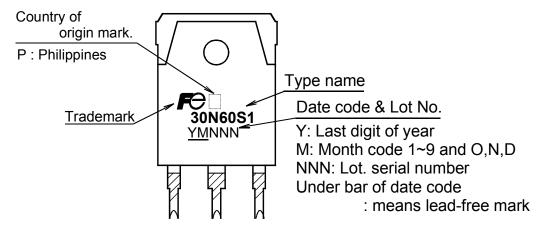
Fig.6 Operating waveform of Reverse recovery Test

Outview: TO-3P Package



JEDEC : TO-3P DIMENSIONS ARE IN MILLIMETERS.

Marking



* The font (font type,size) and the trademark-size might be actually different.

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