

FML12N50ES

FUJI POWER MOSFET

Super FAP-E³ series

N-CHANNEL SILICON POWER MOSFET

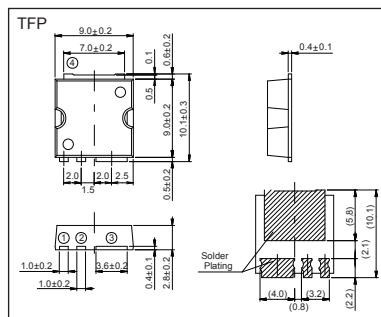
■ Features

- Maintains both low power loss and low noise
- Lower $R_{DS(on)}$ characteristic
- More controllable switching dv/dt by gate resistance
- Smaller V_{GS} ringing waveform during switching
- Narrow band of the gate threshold voltage ($3.7 \pm 0.5V$)
- High avalanche durability

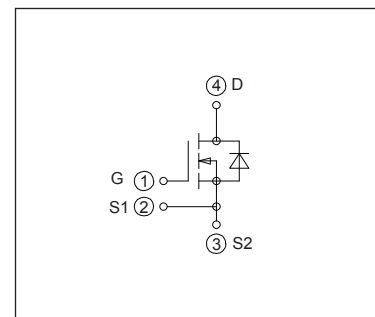
■ Applications

- Switching regulators
- UPS (Uninterruptible Power Supply)
- DC-DC converters

■ Outline Drawings [mm]



■ Equivalent circuit schematic



■ Maximum Ratings and Characteristics

● Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	500	V	$V_{GS} = -30V$
	V_{DSX}	500	V	
Continuous Drain Current	I_D	±12	A	
Pulsed Drain Current	I_{DP}	±48	A	
Gate-Source Voltage	V_{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	12	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E_{AS}	460.8	mJ	Note*2
Repetitive Maximum Avalanche Energy	E_{AR}	18	mJ	Note*3
Peak Diode Recovery dV/dt	dV/dt	6.3	kV/ μs	Note*4
Peak Diode Recovery $-di/dt$	$-di/dt$	100	A/ μs	Note*5
Maximum Power Dissipation	P_D	1.44	W	$T_a=25^{\circ}C$
		180		$T_c=25^{\circ}C$
Operating and Storage Temperature range	T_{ch}	150	$^{\circ}C$	
	T_{stg}	-55 to +150	$^{\circ}C$	

● Electrical Characteristics at Tc=25°C (unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	500	-	-	V
Gate Threshold Voltage	V _{GS} (th)	I _D =250μA, V _{DS} =V _{GS}	3.2	3.7	4.2	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} =500V, V _{GS} =0V	-	-	25	μA
		V _{DS} =400V, V _{GS} =0V	-	-	250	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	10	100	nA
Drain-Source On-State Resistance	R _{DS} (on)	I _D =6A, V _{GS} =10V	-	0.427	0.50	Ω
Forward Transconductance	g _{fs}	I _D =6A, V _{DS} =25V	4.5	9	-	S
Input Capacitance	C _{iss}	V _{DS} =25V	-	1400	2100	pF
Output Capacitance	C _{oss}	V _{GS} =0V	-	160	240	
Reverse Transfer Capacitance	C _{rss}	f=1MHz	-	11.5	17.5	
Turn-On Time	td(on)	V _{GS} =300V	-	31	46.5	ns
	tr	V _{GS} =10V	-	18	27	
Turn-Off Time	td(off)	I _D =6A	-	83	124.5	
	tf	R _G =15Ω	-	16	27	
Total Gate Charge	Q _G	V _{GS} =250V	-	43	56	nC
Gate-Source Charge	Q _{GS}	I _D =12A	-	13	23	
Drain-Source Crossover Charge	Q _{SW}	V _{GS} =10V	-	6	10	
Gate-Drain Charge	Q _{GD}		-	14	21	
Avalanche Capability	I _{AV}	L=2.44mH, T _{ch} =25°C	12	-	-	A
Diode Forward On-Voltage	V _{SD}	I _F =12A, V _{GS} =0V, T _{ch} =25°C	-	0.86	1.30	V
Reverse Recovery Time	trr	I _F =12A, V _{GS} =0V	-	0.37	-	μS
Reverse Recovery Charge	Qrr	-di/dt=100A/μs, T _{ch} =25°C	-	5.0	-	μC

● Thermal Characteristics

Description	Symbol	Test Conditions	min.	typ.	max.	Unit
Thermal resistance	Rth (ch-c)	Channel to case			0.69	°C/W
	Rth (ch-a)	Channel to Ambient			87	°C/W
	Rth (ch-a)	Channel to Ambient Note*6			52	°C/W

Note *1 : Tch≤150°C

Note *2 : Stating Tch=25°C, I_{AS}=5A, L=33.8mH, V_{CC}=50V, R_G=10Ω.

EAS limited by maximum channel temperature and avalanche current.

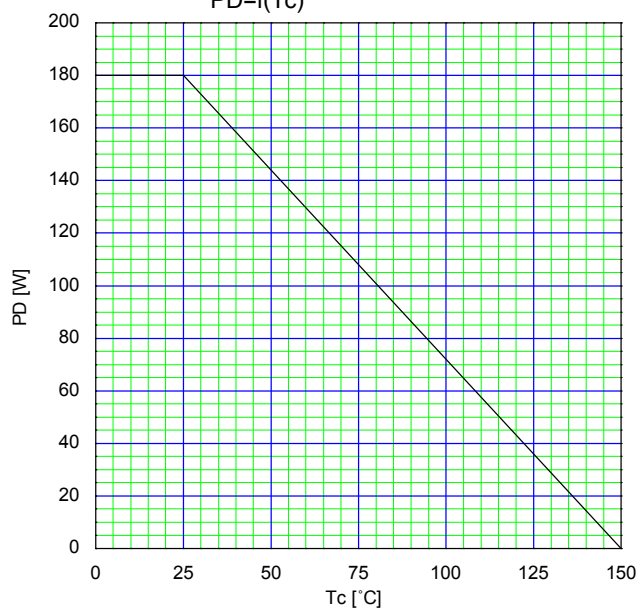
Note *3 : Repetitive rating : Pulse width limited by maximum channel temperature.

Note *4 : $I_F \leq -I_D$, $-di/dt = 100A/\mu s$, $V_{CC} \leq BV_{DSS}$, $T_{ch} \leq 150^\circ C$

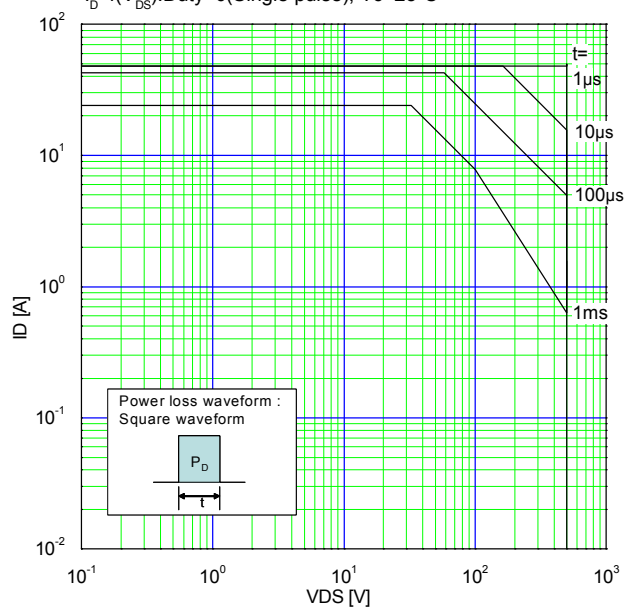
Note *5 : $I_F \leq -I_D$, $dv/dt = 6.3 \text{ kV}/\mu\text{s}$, $V_{CC} \leq BV_{DSS}$, $T_{ch} \leq 150^\circ\text{C}$

Note *6 : Surface mounted on 1000mm², t=1.6mm FR-4 PCB (Drain pad area : 500mm²)

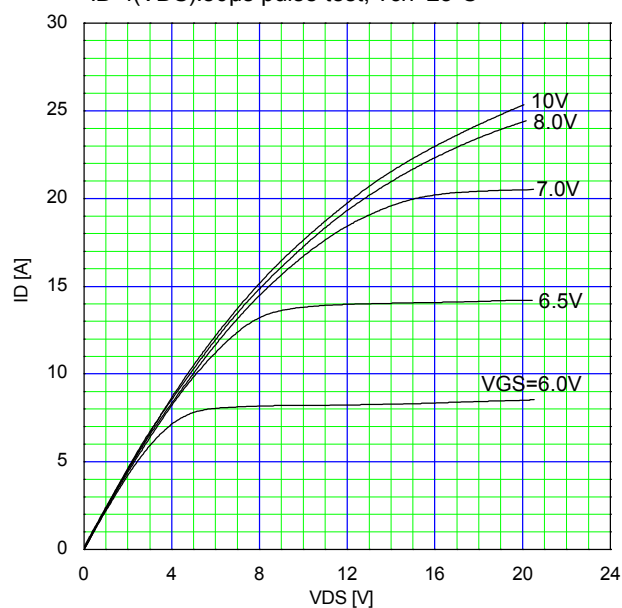
Allowable Power Dissipation
 $P_D = f(T_c)$



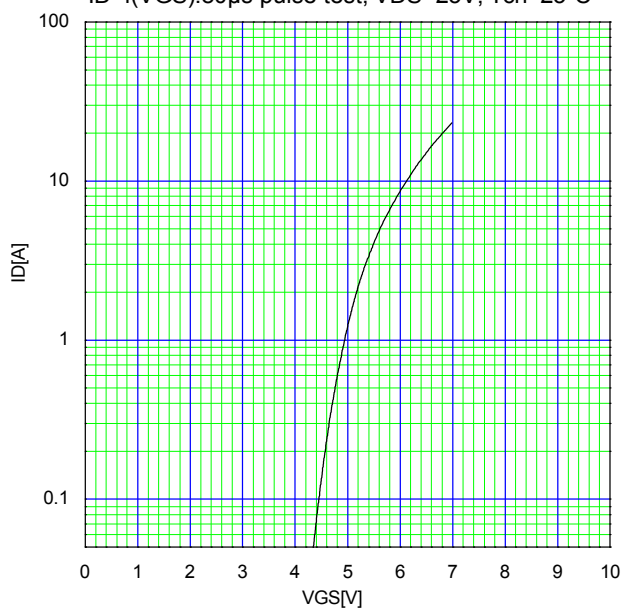
Safe Operating Area
 $I_D = f(V_{DS})$: Duty=0 (Single pulse), $T_c = 25^\circ\text{C}$



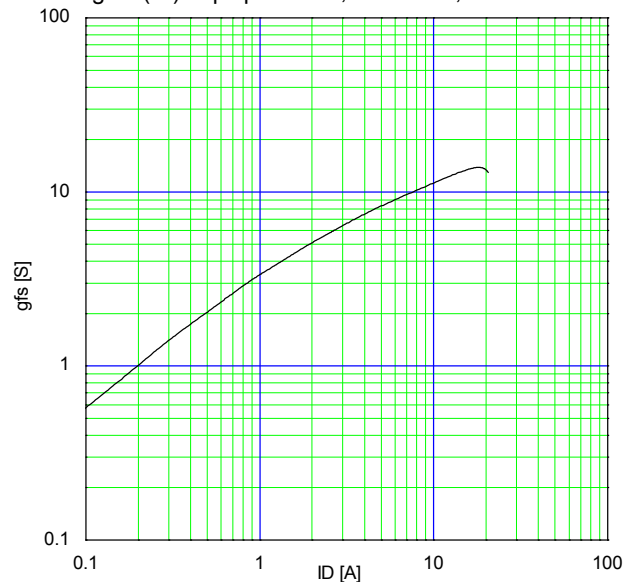
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80 μs pulse test, $T_{ch} = 25^\circ\text{C}$



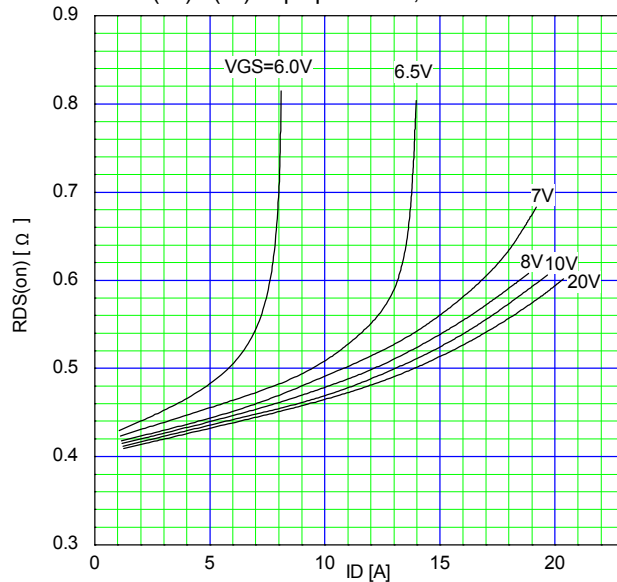
Typical Transfer Characteristic
 $I_D = f(V_{GS})$: 80 μs pulse test, $V_{DS} = 25\text{V}$, $T_{ch} = 25^\circ\text{C}$



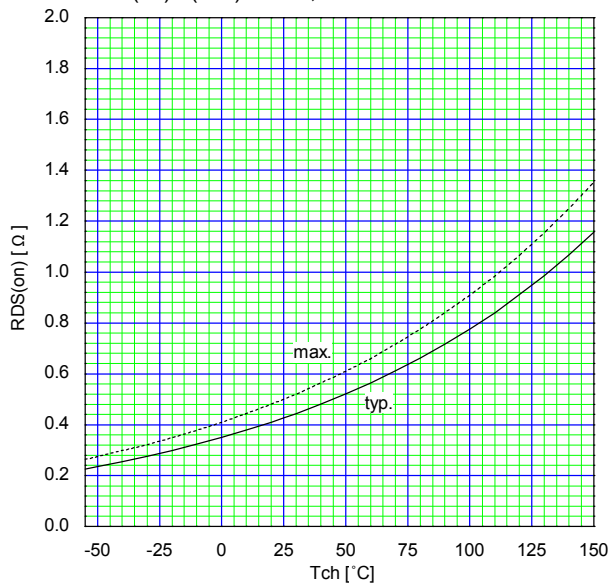
Typical Transconductance
 $g_{fs} = f(I_D)$: 80 μs pulse test, $V_{DS} = 25\text{V}$, $T_{ch} = 25^\circ\text{C}$



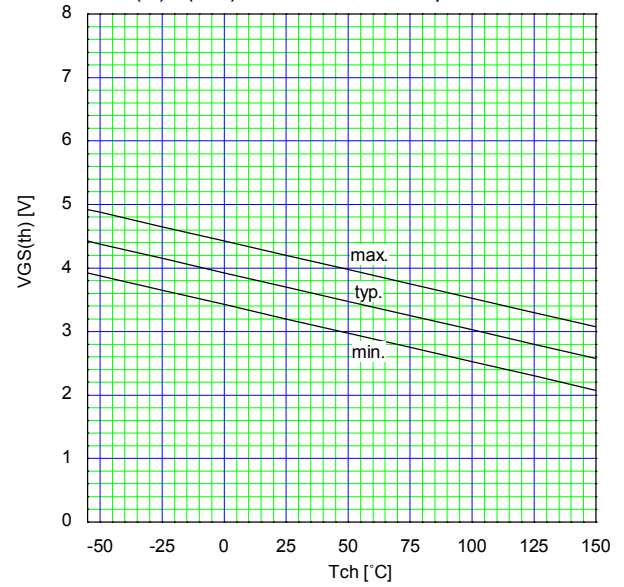
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80 μs pulse test, $T_{ch} = 25^\circ\text{C}$



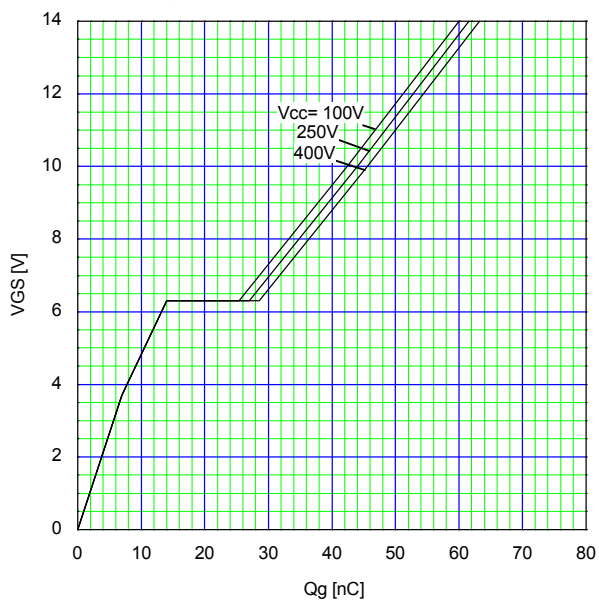
Drain-Source On-state Resistance
 $R_{DS(on)} = f(T_{ch})$: $I_D = 6A$, $V_{GS} = 10V$



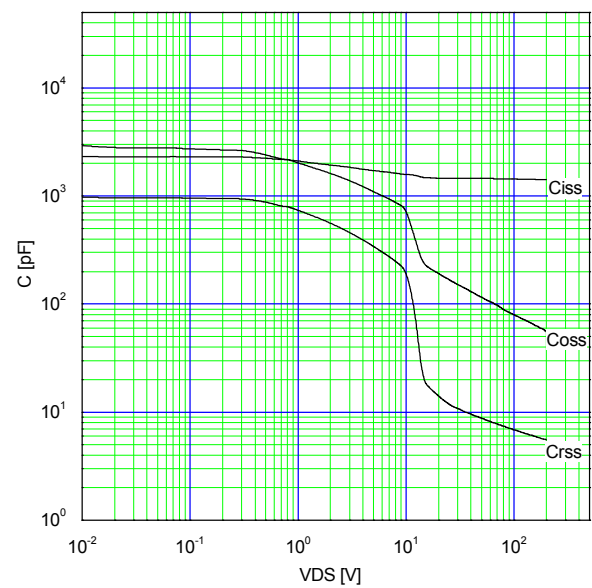
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)} = f(T_{ch})$: $V_{DS} = V_{GS}$, $I_D = 250\mu A$



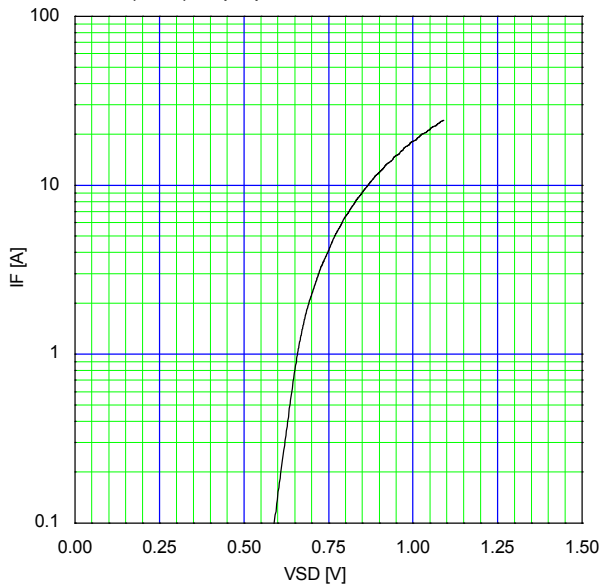
Typical Gate Charge Characteristics
 $V_{GS} = f(Q_g)$: $I_D = 12A$, $T_{ch} = 25^{\circ}C$



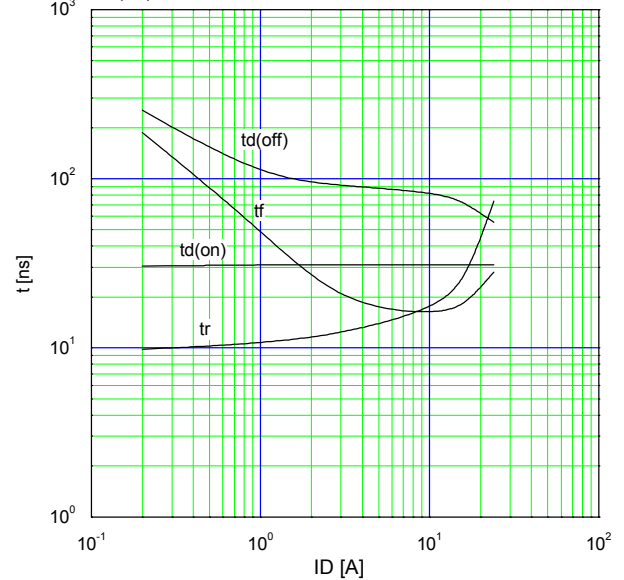
Typical Capacitance
 $C = f(V_{DS})$: $V_{GS} = 0V$, $f = 1MHz$

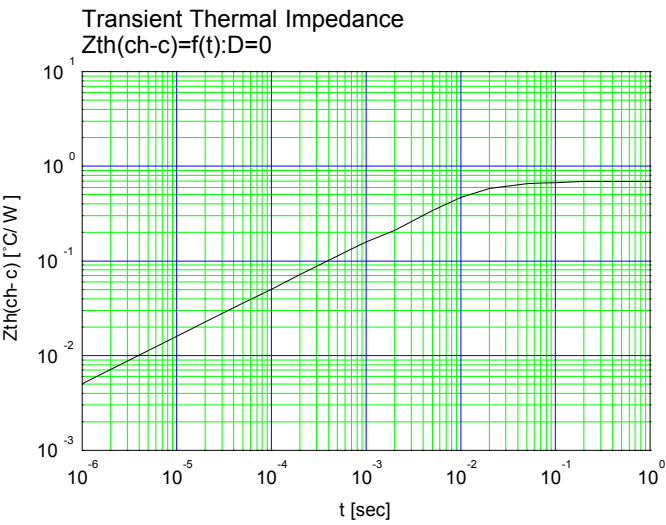
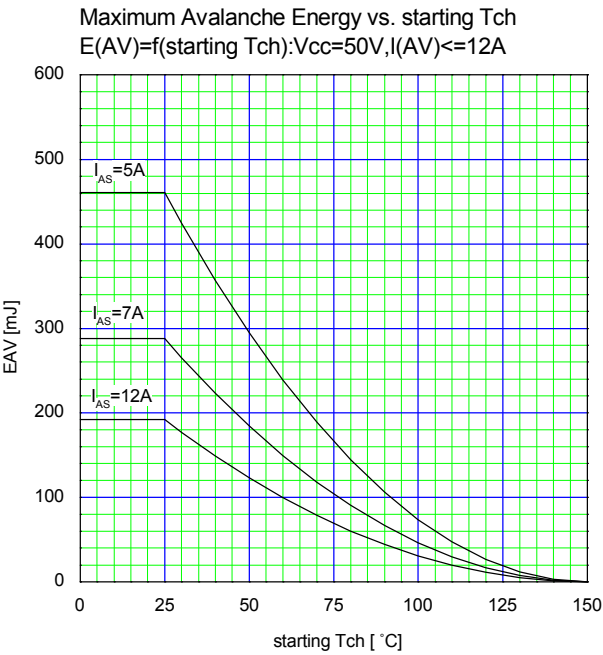


Typical Forward Characteristics of Reverse Diode
 $I_F = f(V_{SD})$: $80\mu s$ pulse test, $T_{ch} = 25^{\circ}C$



Typical Switching Characteristics vs. I_D
 $t = f(I_D)$: $V_{CC} = 300V$, $V_{GS} = 10V$, $R_G = 15\Omega$





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