

FML16N50ES

FUJI POWER MOSFET

Super FAP-E³ series

N-CHANNEL SILICON POWER MOSFET

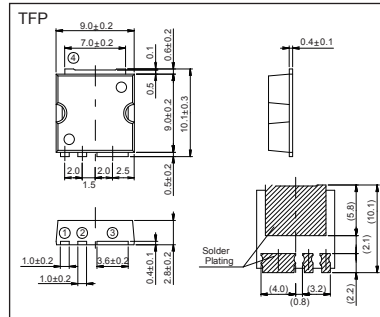
■ Features

Maintains both low power loss and low noise
Lower $R_{DS(on)}$ characteristic
More controllable switching dV/dt by gate resistance
Smaller V_{GS} ringing waveform during switching
Narrow band of the gate threshold voltage ($4.2 \pm 0.5V$)
High avalanche durability

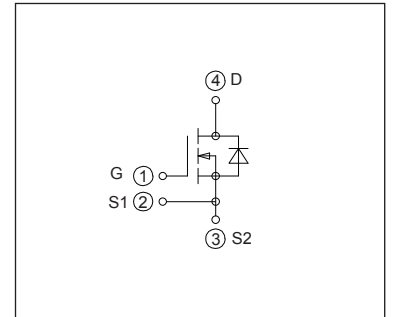
■ Applications

Switching regulators
UPS (Uninterruptible Power Supply)
DC-DC converters

■ Outline Drawings [mm]



■ Equivalent circuit schematic



■ Maximum Ratings and Characteristics

● Absolute Maximum Ratings at $T_c=25^\circ C$ (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	500	V	
	V_{DSX}	500	V	$V_{GS} = -30V$
Continuous Drain Current	I_D	± 16	A	
Pulsed Drain Current	I_{DP}	± 64	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	16	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E_{AS}	485	mJ	Note*2
Repetitive Maximum Avalanche Energy	E_{AR}	22.5	mJ	Note*3
Peak Diode Recovery dV/dt	dV/dt	4.8	kV/ μs	Note*4
Peak Diode Recovery $-di/dt$	$-di/dt$	100	A/ μs	Note*5
Maximum Power Dissipation	P_D	1.44	W	$T_a=25^\circ C$
		225		$T_c=25^\circ C$
Operating and Storage Temperature range	T_{ch}	150	$^\circ C$	
	T_{stg}	-55 to +150	$^\circ C$	

● Electrical Characteristics at $T_c=25^\circ C$ (unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	500	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=V_{GS}$	3.7	4.2	4.7	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=500V, V_{GS}=0V$	-	-	25	μA
		$V_{DS}=400V, V_{GS}=0V$	-	-	250	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D=8A, V_{GS}=10V$	-	0.33	0.38	Ω
Forward Transconductance	g_{fs}	$I_D=8A, V_{DS}=25V$	5.5	11	-	S
Input Capacitance	C_{iss}	$V_{DS}=25V$	-	1700	2550	pF
Output Capacitance	C_{oss}	$V_{GS}=0V$	-	210	315	
Reverse Transfer Capacitance	C_{rss}	$f=1MHz$	-	13	19.5	
Turn-On Time	$t_{d(on)}$	$V_{cc}=300V$	-	37	55.5	ns
	t_r	$V_{GS}=10V$	-	30	45	
Turn-Off Time	$t_{d(off)}$	$I_D=8A$	-	87	130.5	
	t_f	$R_G=18\Omega$	-	17	25.5	nC
Total Gate Charge	Q_G	$V_{cc}=250V$	-	48	72	
Gate-Source Charge	Q_{GS}	$I_D=16A$	-	17	25.5	
Drain-Source Crossover Charge	Q_{SW}	$V_{GS}=10V$	-	7	10.5	
Gate-Drain Charge	Q_{GD}		-	18	27	
Avalanche Capability	I_{AV}	$L=1.52mH, T_{ch}=25^\circ C$	16	-	-	A
Diode Forward On-Voltage	V_{SD}	$I_F=16A, V_{GS}=0V, T_{ch}=25^\circ C$	-	0.90	1.35	V
Reverse Recovery Time	t_{rr}	$I_F=16A, V_{GS}=0V$	-	0.46	-	μs
Reverse Recovery Charge	Q_{rr}	$-di/dt=100A/\mu s, T_{ch}=25^\circ C$	-	6.0	-	μC

● Thermal Characteristics

Description	Symbol	Test Conditions	min.	typ.	max.	Unit
Thermal resistance	$R_{th(ch-c)}$	Channel to case			0.56	$^\circ C/W$
	$R_{th(ch-a)}$	Channel to Ambient			87	$^\circ C/W$
	$R_{th(ch-a)}$	Channel to Ambient Note*6			52	$^\circ C/W$

Note *1 : $T_{ch} \leq 150^\circ C$

Note *2 : Stating $T_{ch}=25^\circ C, I_{AS}=5A, L=33.8mH, V_{cc}=50V, R_G=10\Omega,$

E_{AS} limited by maximum channel temperature and avalanche current.

Note *3 : Repetitive rating : Pulse width limited by maximum channel temperature.

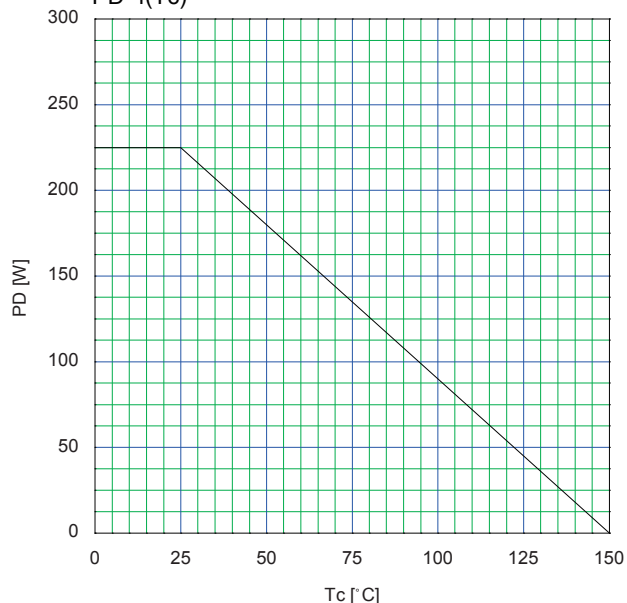
Note *4 : $I_F=I_D, -di/dt=100A/\mu s, V_{cc} \leq BV_{DSS}, T_{ch} \leq 150^\circ C.$

Note *5 : $I_F=I_D, dv/dt=6.3kV/\mu s, V_{cc} \leq BV_{DSS}, T_{ch} \leq 150^\circ C.$

Note *6 : Surface mounted on 1000mm², $t=1.6mm$ FR-4 PCB (Drain pad area : 500mm²)

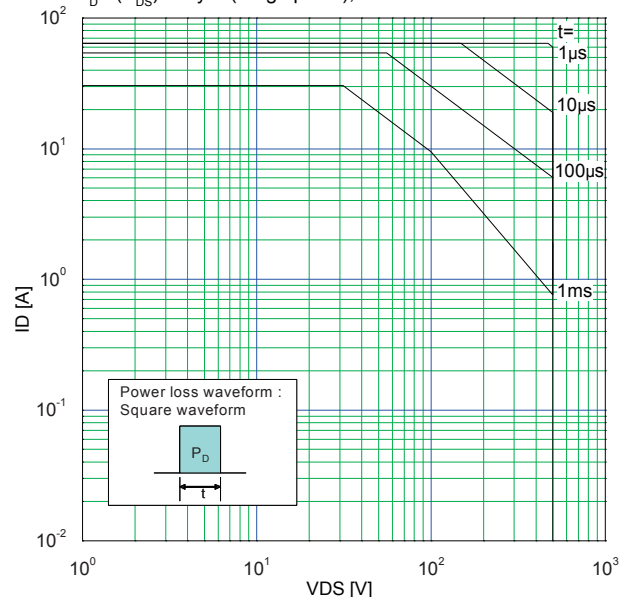
Allowable Power Dissipation

$P_D = f(T_c)$



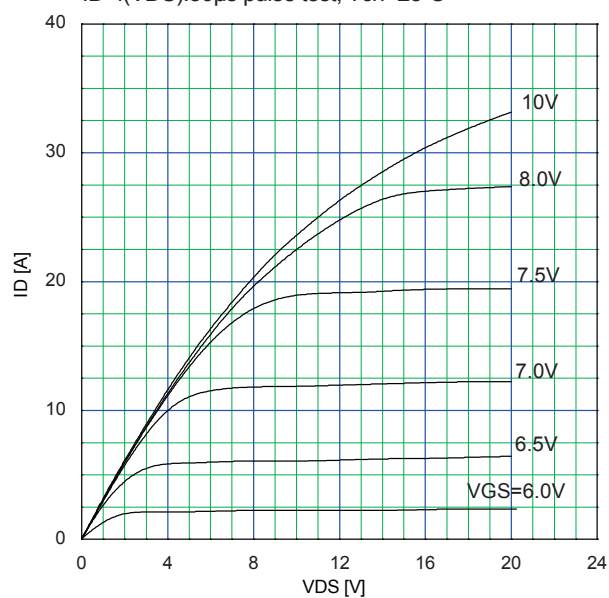
Safe Operating Area

$I_D = f(V_{DS}): \text{Duty}=0(\text{Single pulse}), T_c=25^\circ\text{C}$



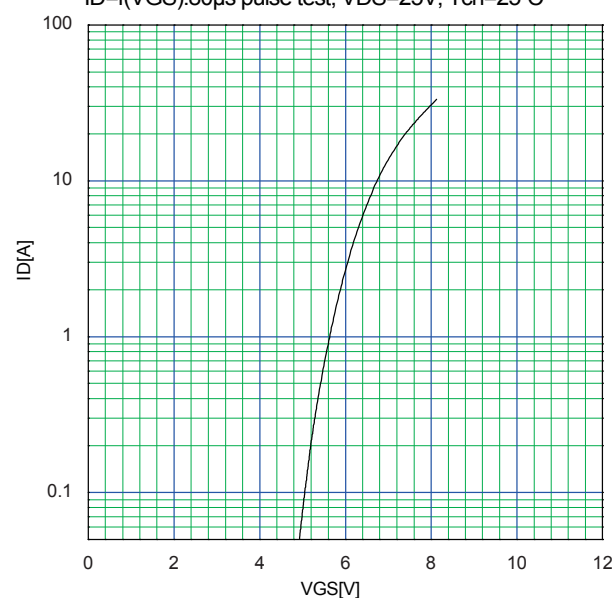
Typical Output Characteristics

$I_D = f(V_{DS}): 80\mu\text{s pulse test}, T_{ch}=25^\circ\text{C}$



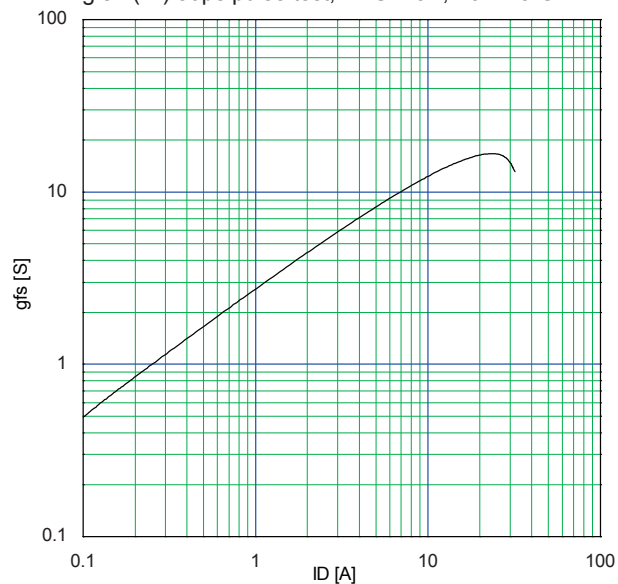
Typical Transfer Characteristic

$I_D = f(V_{GS}): 80\mu\text{s pulse test}, V_{DS}=25\text{V}, T_{ch}=25^\circ\text{C}$



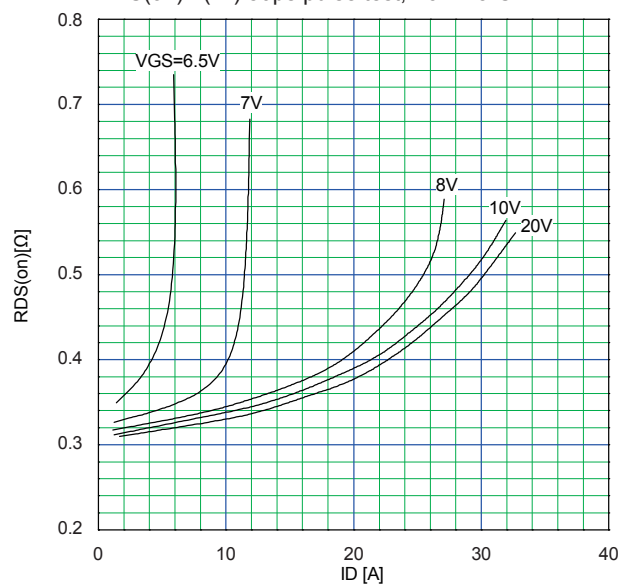
Typical Transconductance

$g_{fs} = f(I_D): 80\mu\text{s pulse test}, V_{DS}=25\text{V}, T_{ch}=25^\circ\text{C}$

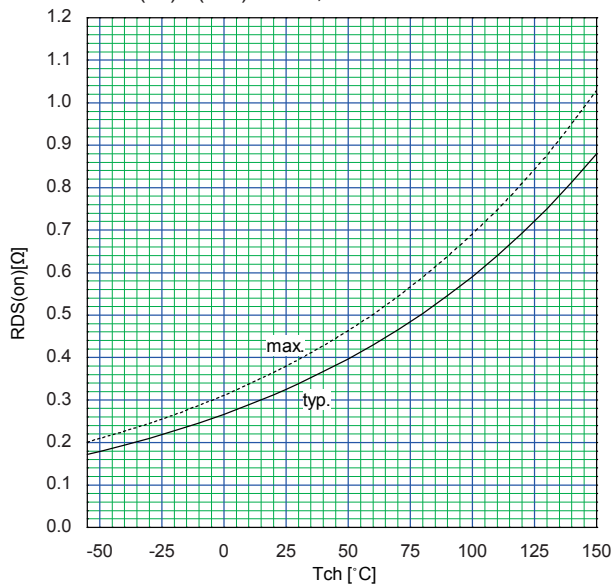


Typical Drain-Source on-state Resistance

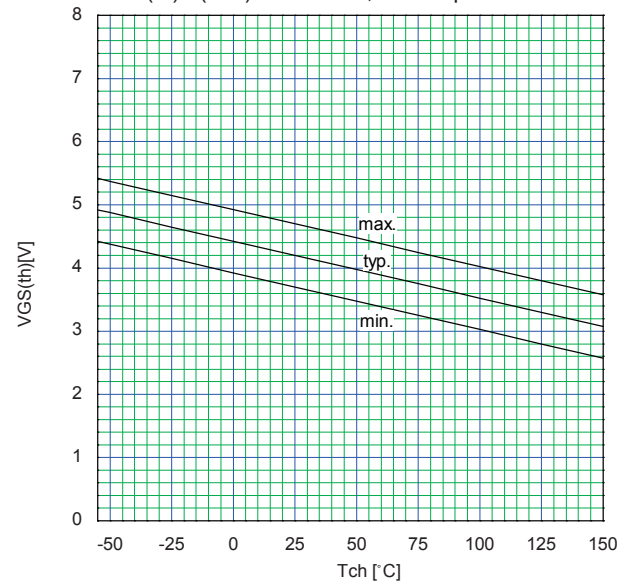
$R_{DS(on)} = f(I_D): 80\mu\text{s pulse test}, T_{ch}=25^\circ\text{C}$



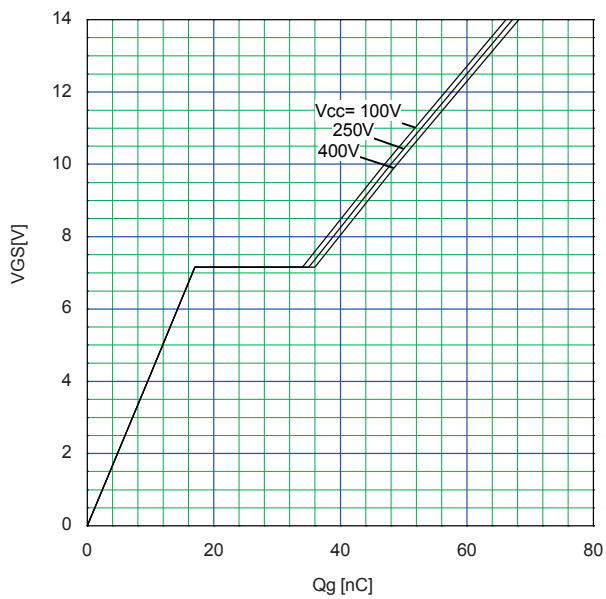
Drain-Source On-state Resistance
 $R_{DS(on)} = f(T_{ch}): I_D = 8A, V_{GS} = 10V$



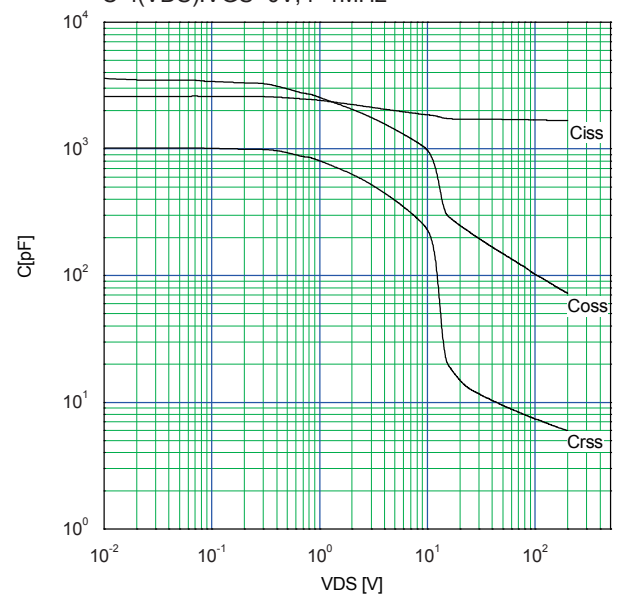
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)} = f(T_{ch}): V_{DS} = V_{GS}, I_D = 250\mu A$



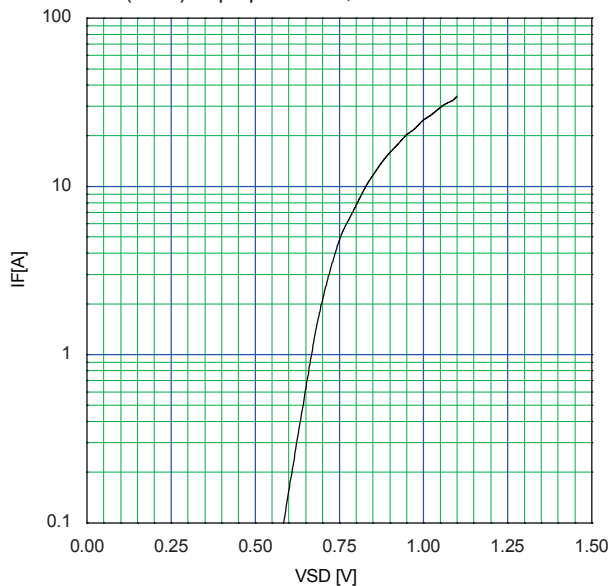
Typical Gate Charge Characteristics
 $V_{GS} = f(Q_g): I_D = 16A, T_{ch} = 25^\circ C$



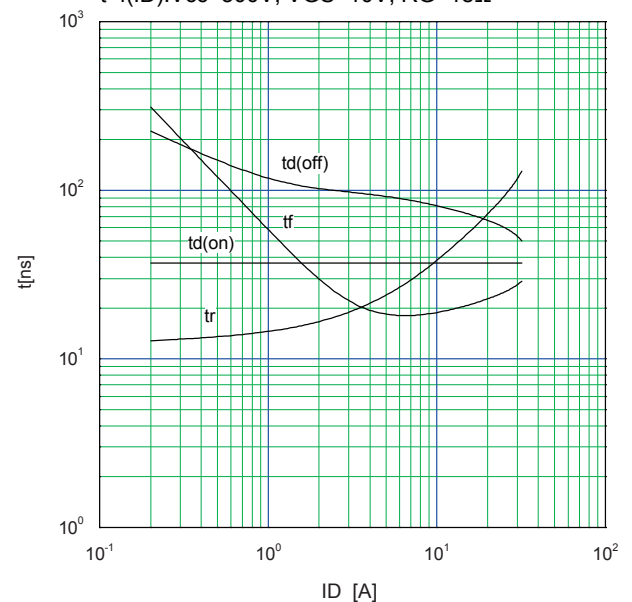
Typical Capacitance
 $C = f(V_{DS}): V_{GS} = 0V, f = 1MHz$

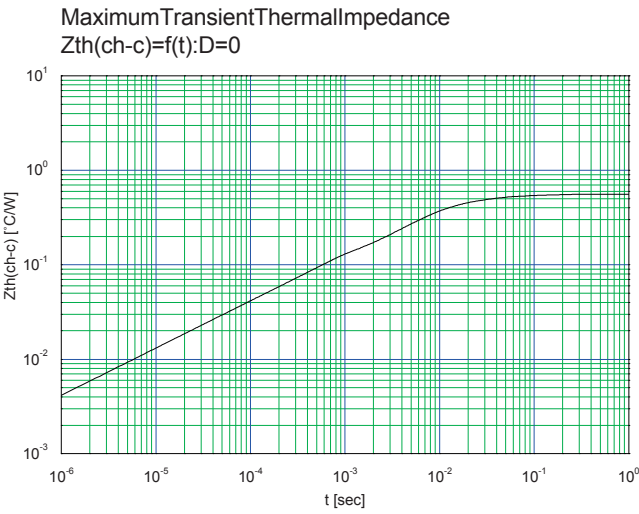
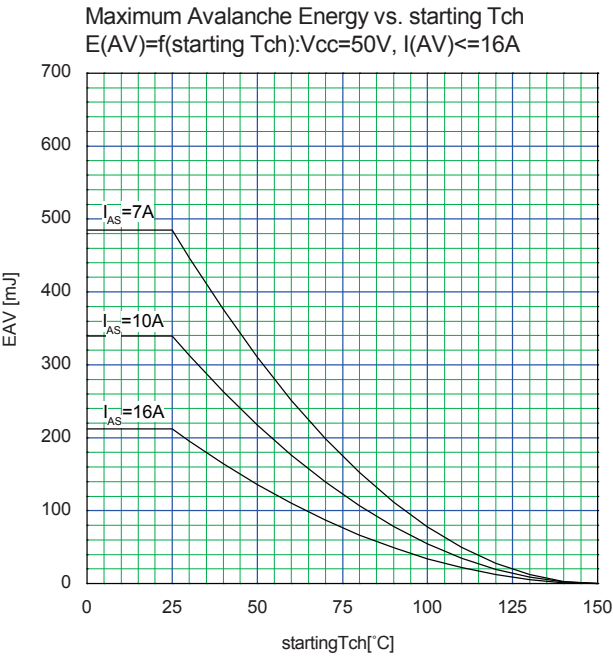


Typical Forward Characteristics of Reverse Diode
 $I_F = f(V_{SD}): 80\mu s$ pulse test, $T_{ch} = 25^\circ C$



Typical Switching Characteristics vs. I_D
 $t = f(I_D): V_{CC} = 300V, V_{GS} = 10V, R_G = 18\Omega$





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