

# FMP08N60S1

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FUJI POWER MOSFET

## Super J-MOS series

## N-Channel enhancement mode power MOSFET

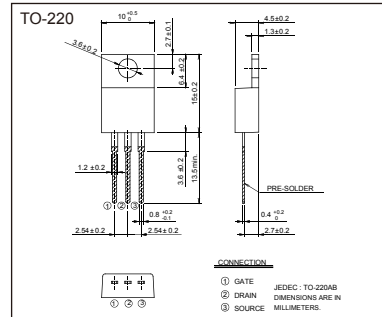
### Features

Pb-free lead terminal  
RoHS compliant

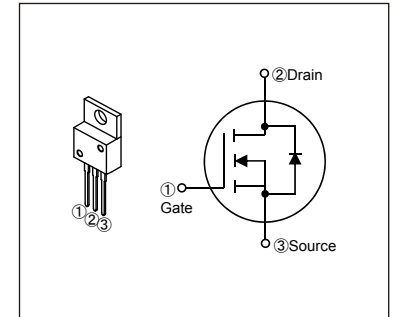
### Applications

For switching

### Outline Drawings [mm]



### Equivalent circuit schematic



### Absolute Maximum Ratings at TC=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	$V_{DS}$	600	V	
	$V_{DSX}$	600	V	$V_{GS} = -30V$
Continuous Drain Current	$I_D$	±8	A	$T_c = 25^\circ C$ Note*1
		±5.1	A	$T_c = 100^\circ C$ Note*1
Pulsed Drain Current	$I_{DP}$	±24	A	
Gate-Source Voltage	$V_{GS}$	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	$I_{AR}$	2.5	A	Note *2
Non-Repetitive Maximum Avalanche Energy	$E_{AS}$	249.6	mJ	Note *3
Maximum Drain-Source dV/dt	$dV_{DS}/dt$	50	kV/μs	$V_{DS} \leq 600V$
Peak Diode Recovery dV/dt	$dV/dt$	15	kV/μs	Note *4
Peak Diode Recovery -di/dt	$-di/dt$	100	A/μs	Note *5
Maximum Power Dissipation	$P_D$	2.02	W	$T_a = 25^\circ C$
		70		$T_c = 25^\circ C$
Operating and Storage Temperature range	$T_{ch}$	150	°C	
	$T_{slg}$	-55 to +150	°C	

Note \*1 : Limited by maximum channel temperature.

Note \*2 :  $T_{ch} \leq 150^\circ C$ , See Fig.1 and Fig.2

Note \*3 : Starting  $T_{ch} = 25^\circ C$ ,  $I_{AS} = 1.5A$ ,  $L = 203mH$ ,  $V_{DD} = 60V$ ,  $R_G = 50\Omega$ , See Fig.1 and Fig.2

$E_{AS}$  limited by maximum channel temperature and avalanche current.

Note \*4 :  $I_{FS} \leq I_D$ ,  $-di/dt = 100A/\mu s$ ,  $V_{DD} \leq 400V$ ,  $V_{peak} \leq BV_{DSS}$ ,  $T_{ch} \leq 150^\circ C$ .

Note \*5 :  $I_{FS} \leq I_D$ ,  $dV/dt = 15kV/\mu s$ ,  $V_{DD} \leq 400V$ ,  $V_{peak} \leq BV_{DSS}$ ,  $T_{ch} \leq 150^\circ C$ .

### Electrical Characteristics at TC=25°C (unless otherwise specified)

#### • Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu A$ $V_{GS} = 0V$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D = 250\mu A$ $V_{DS} = V_{GS}$	2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600V$ $V_{GS} = 0V$ $T_{ch} = 25^\circ C$	-	-	25	μA
		$V_{DS} = 480V$ $V_{GS} = 0V$ $T_{ch} = 125^\circ C$	-	-	250	
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 30V$ $V_{DS} = 0V$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D = 4A$ $V_{GS} = 10V$	-	0.399	0.47	Ω
Gate resistance	$R_G$	$f = 1MHz$ , open drain	-	2.9	-	Ω

## • Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	$g_{fs}$	$I_D=4A$ $V_{DS}=25V$	3.5	7.5	-	S
Input Capacitance	$C_{iss}$	$V_{DS}=10V$	-	620	-	pF
Output Capacitance	$C_{oss}$	$V_{GS}=0V$ $f=1MHz$	-	1340	-	
Reverse Transfer Capacitance	$C_{rss}$		-	120	-	
Effective output capacitance, energy related (Note *6)	$C_{o(er)}$	$V_{GS}=0V$ $V_{DS}=0...480V$	-	48	-	
Effective output capacitance, time related (Note *7)	$C_{o(tr)}$	$V_{GS}=0V$ $V_{DS}=0...480V$ $I_D=constant$	-	140	-	
Turn-On Time	$t_{d(on)}$	$V_{DD}=400V, V_{GS}=10V/0V$ $I_D=4A, R_G=30\Omega$ See Fig.3 and Fig.4	-	9.5	-	ns
	$t_r$		-	29	-	
Turn-Off Time	$t_{d(off)}$		-	75	-	
	$t_f$		-	16	-	
Total Gate Charge	$Q_G$	$V_{DD}=480V, I_D=8A$ $V_{GS}=10V$ See Fig.5	-	25	-	nC
Gate-Source Charge	$Q_{GS}$		-	7.5	-	
Gate-Drain Charge	$Q_{GD}$		-	6	-	
Drain-Source crossover Charge	$Q_{SW}$		-	5	-	

Note \*6 :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $BV_{DSS}$ .

Note \*7 :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $BV_{DSS}$ .

## • Reverse Diode

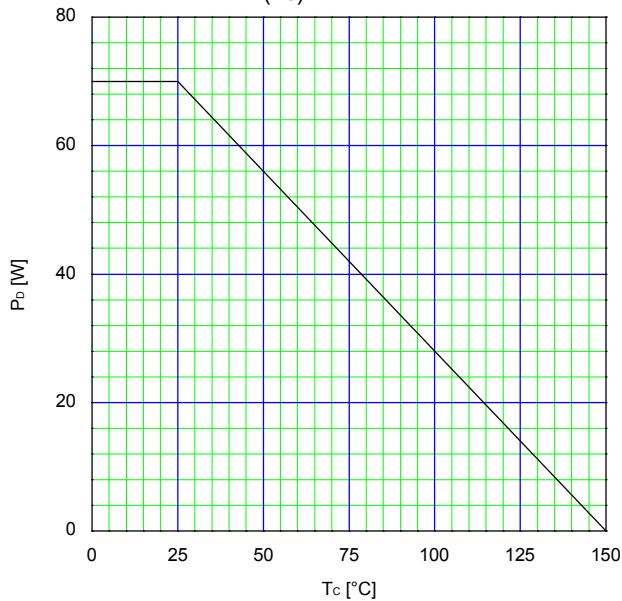
Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	$I_{AV}$	$L=43.9mH, T_{ch}=25^\circ C$ See Fig.1 and Fig.2	2.5	-	-	A
Diode Forward On-Voltage	$V_{SD}$	$I_F=8A, V_{GS}=0V$ $T_{ch}=25^\circ C$	-	0.9	1.35	V
Reverse Recovery Time	$t_{rr}$	$I_F=8A, V_{DD}=400V$ $-di/dt=100A/\mu s$ $V_{GS(Q1)}=short, V_{GS(Q2)}=10V/0V$ $R_G=330\Omega$ $T_{ch}=25^\circ C$		285	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	3.2	-	$\mu C$
Peak Reverse Recovery Current	$I_{rp}$	See Fig.6 and Fig.7	-	20	-	A

## ■ Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	1.79	$^\circ C/W$
Channel to Ambient	$R_{th(ch-a)}$	-	-	62	$^\circ C/W$

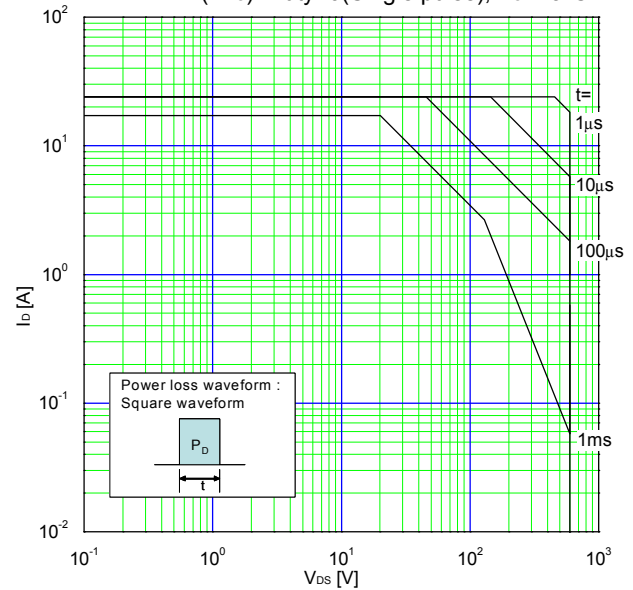
Allowable Power Dissipation

$P_D = f(T_C)$



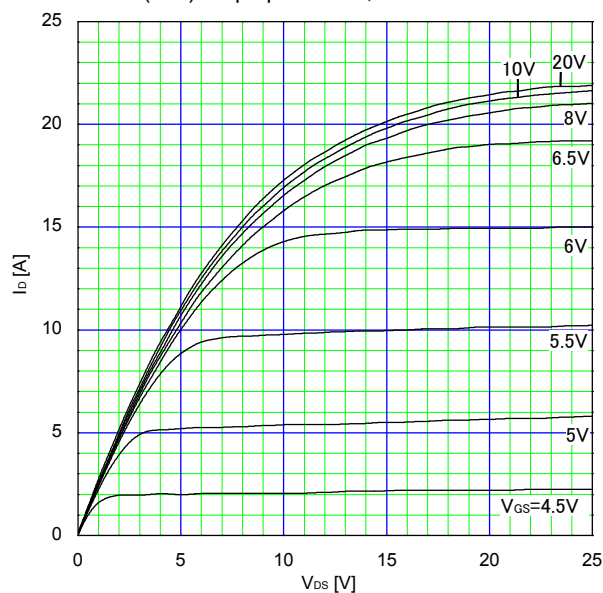
Safe Operating Area

$I_D = f(V_{DS})$ ; Duty=0 (Single pulse),  $T_C = 25^\circ\text{C}$



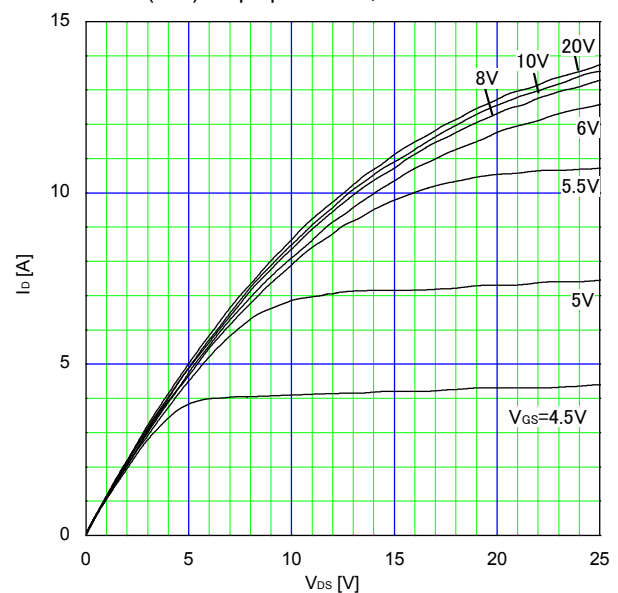
Typical Output Characteristics

$I_D = f(V_{DS})$ ; 80  $\mu\text{s}$  pulse test,  $T_{ch} = 25^\circ\text{C}$



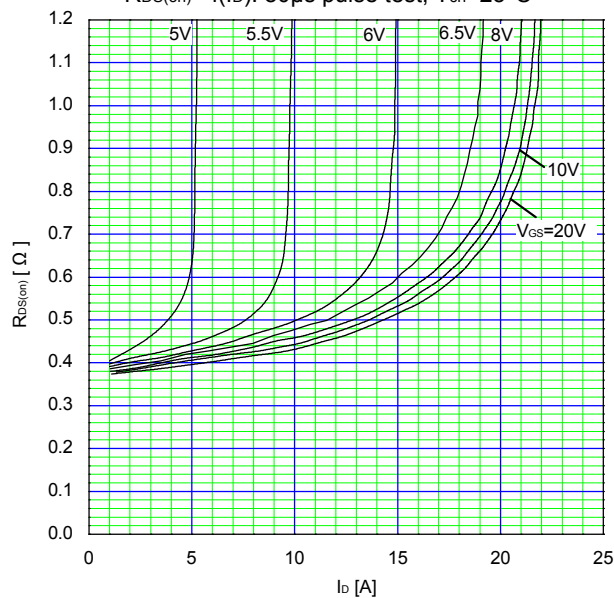
Typical Output Characteristics

$I_D = f(V_{DS})$ ; 80  $\mu\text{s}$  pulse test,  $T_{ch} = 150^\circ\text{C}$



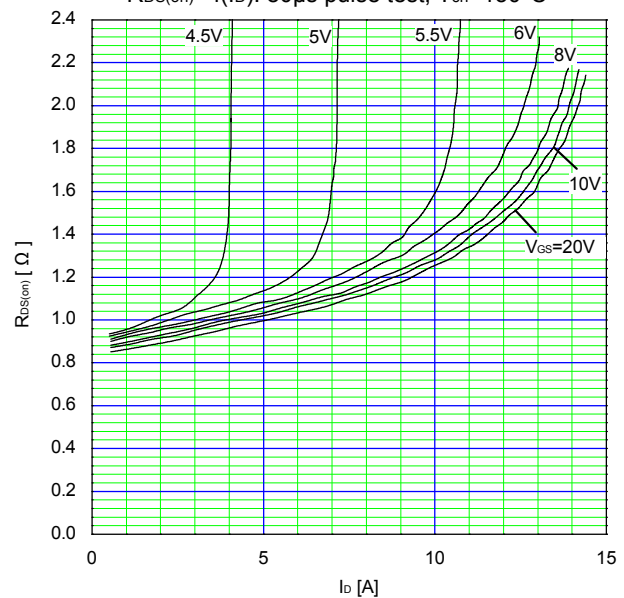
Typical Drain-Source on-state Resistance

$R_{DS(on)} = f(I_D)$ ; 80  $\mu\text{s}$  pulse test,  $T_{ch} = 25^\circ\text{C}$



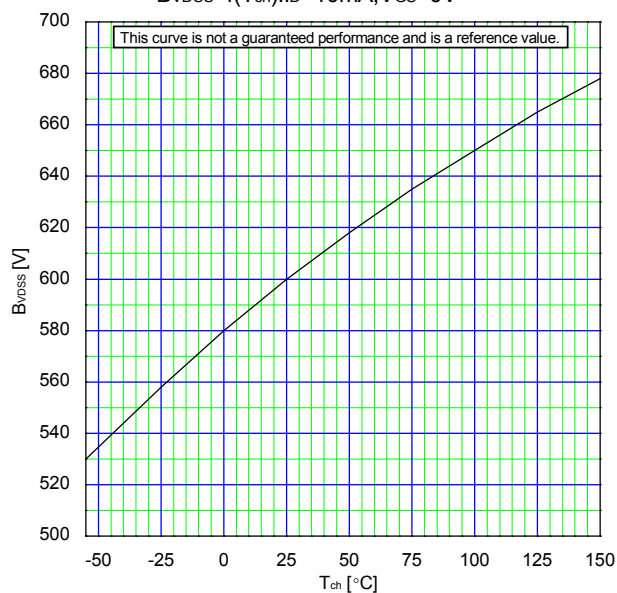
Typical Drain-Source on-state Resistance

$R_{DS(on)} = f(I_D)$ ; 80  $\mu\text{s}$  pulse test,  $T_{ch} = 150^\circ\text{C}$



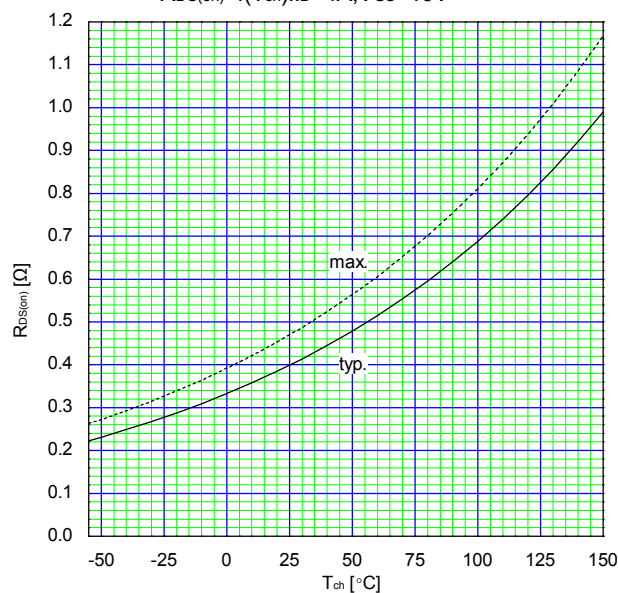
Drain-Source Breakdown Voltage

$$B_{VDS} = f(T_{ch}): I_D = 10\text{mA}, V_{GS} = 0\text{V}$$

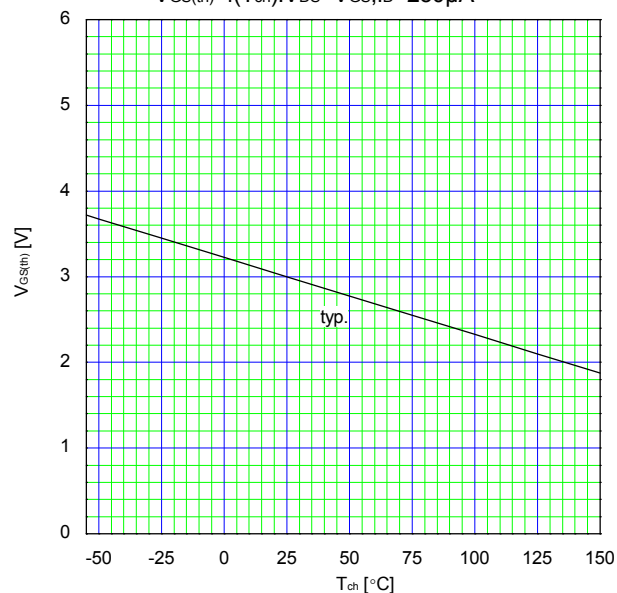


Drain-Source On-state Resistance

$$R_{DS(on)} = f(T_{ch}): I_D = 4\text{A}, V_{GS} = 10\text{V}$$

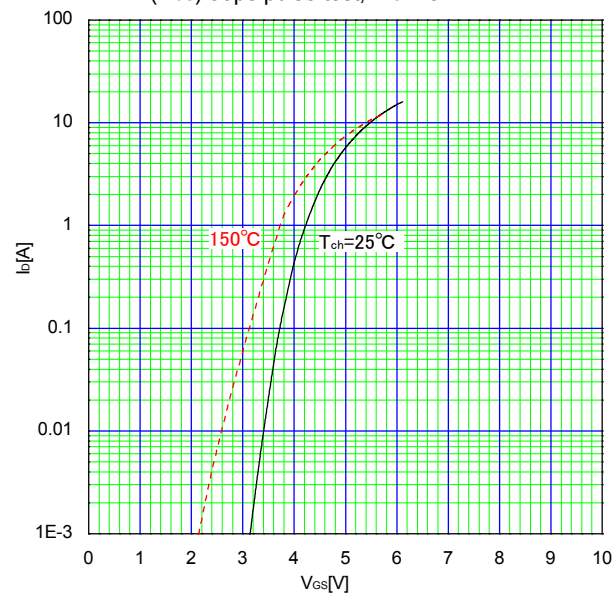
Gate Threshold Voltage vs.  $T_{ch}$ 

$$V_{GS(th)} = f(T_{ch}): V_{DS} = V_{GS}, I_D = 250\mu\text{A}$$



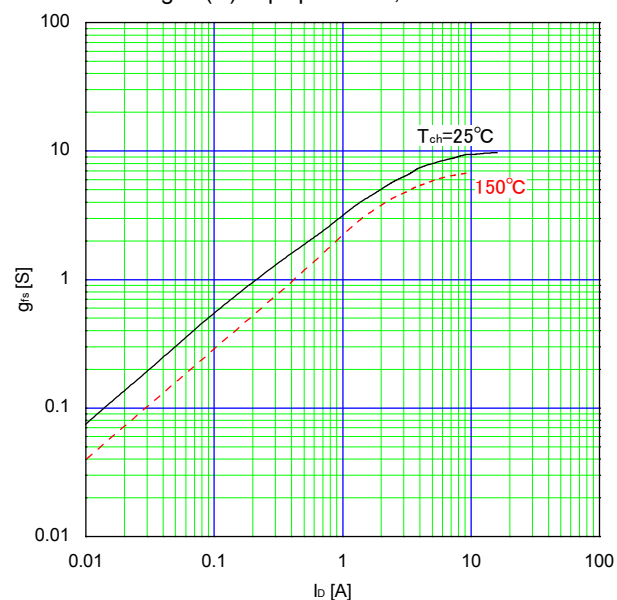
Typical Transfer Characteristic

$$I_D = f(V_{GS}): 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



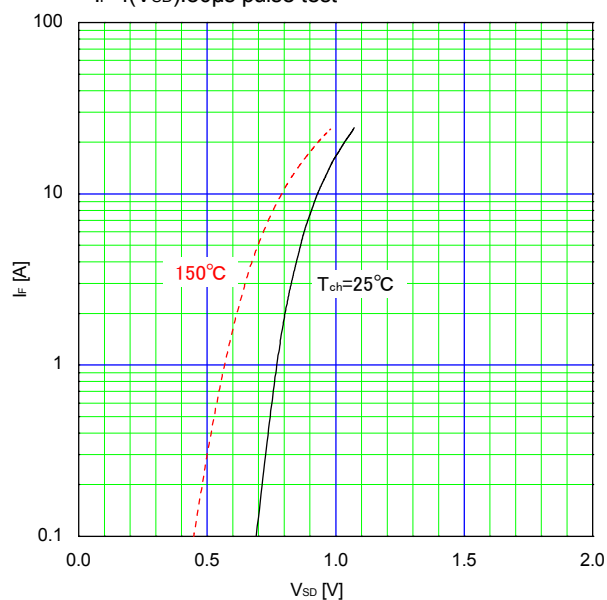
Typical Transconductance

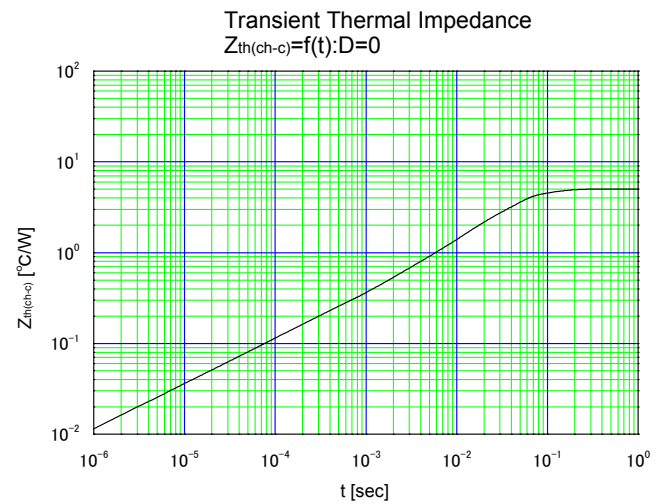
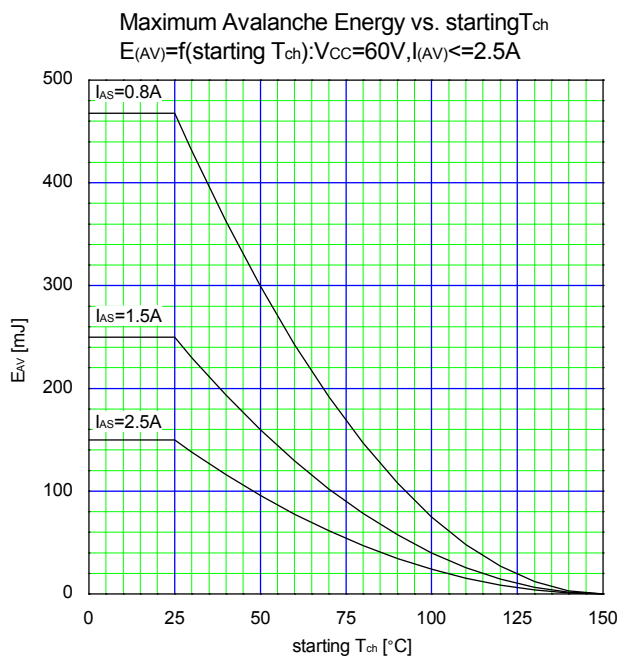
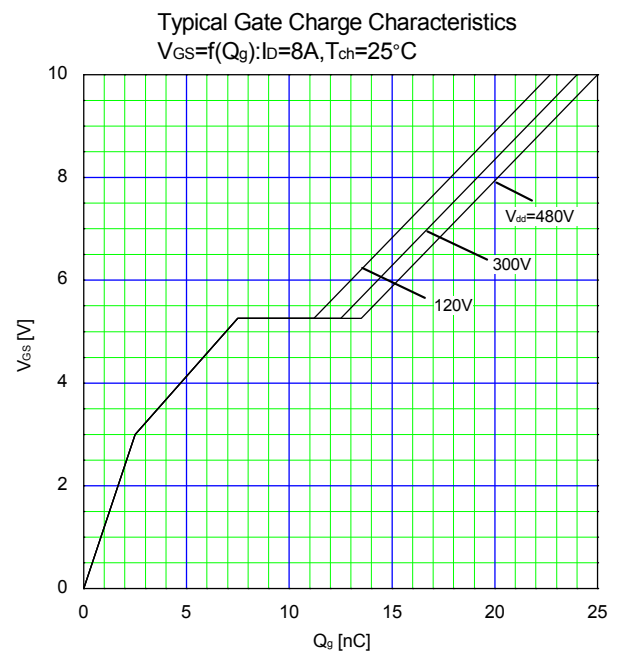
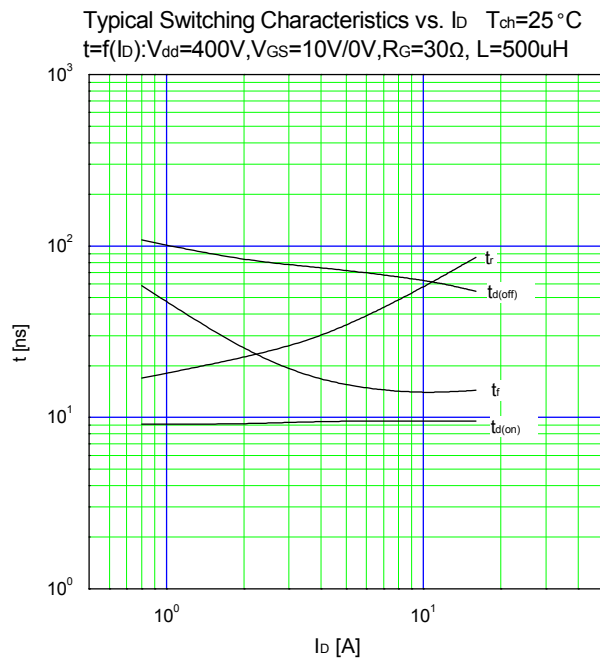
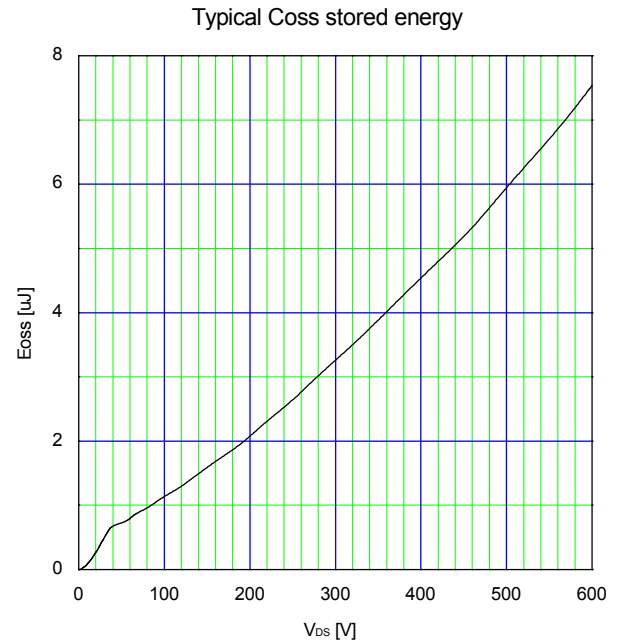
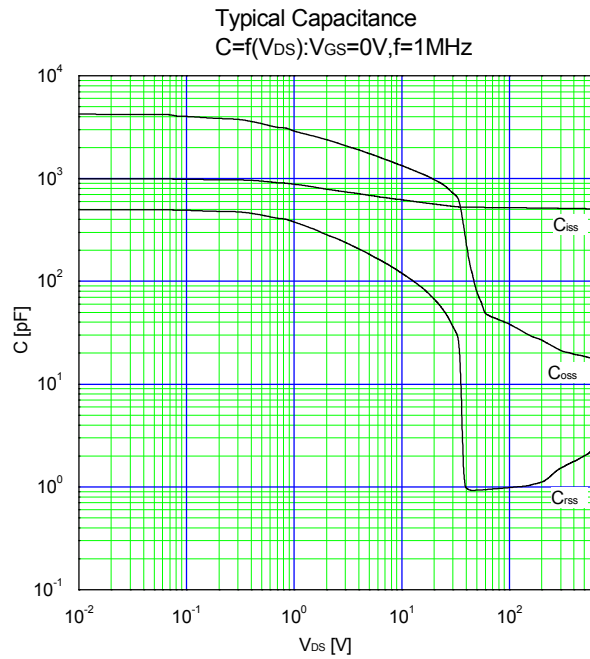
$$g_{fs} = f(I_D): 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



Typical Forward Characteristics of Reverse Diode

$$I_F = f(V_{SD}): 80\mu\text{s pulse test}$$





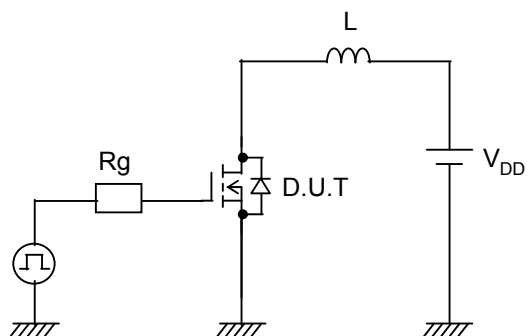


Fig.1 Avalanche Test circuit

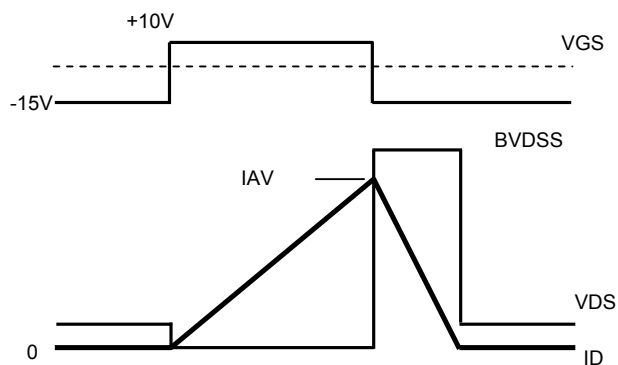


Fig.2 Operating waveforms of Avalanche Test

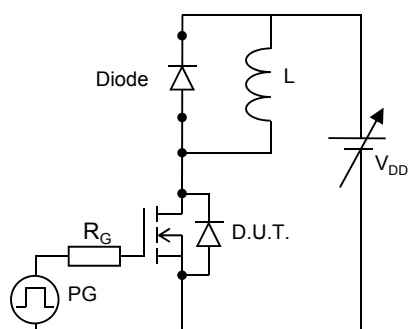


Fig.3 Switching Test circuit

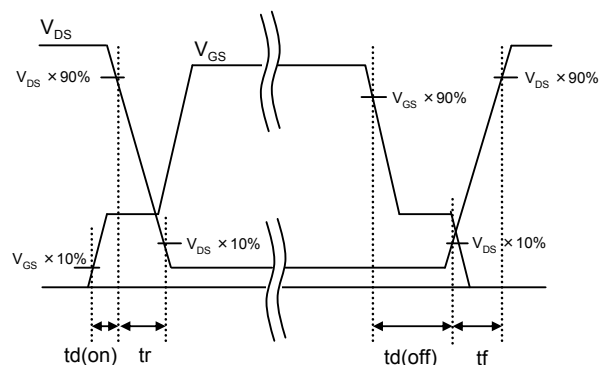


Fig.4 Operating waveform of Switching Test

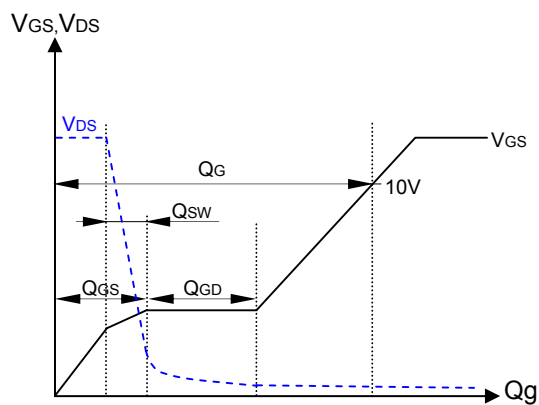


Fig.5 Operating waveform of Gate charge Test

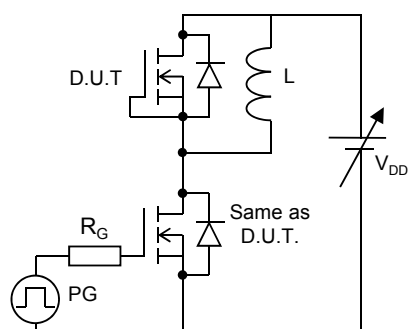


Fig.6 Reverse recovery Test circuit

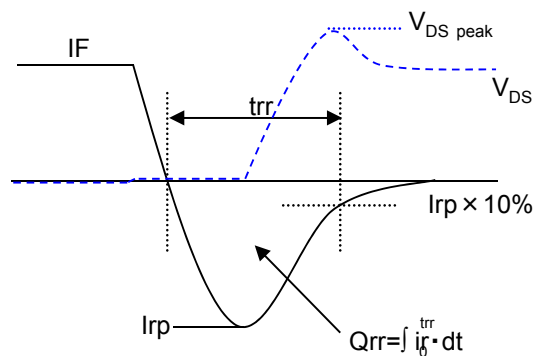
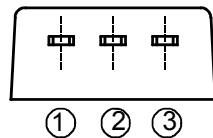
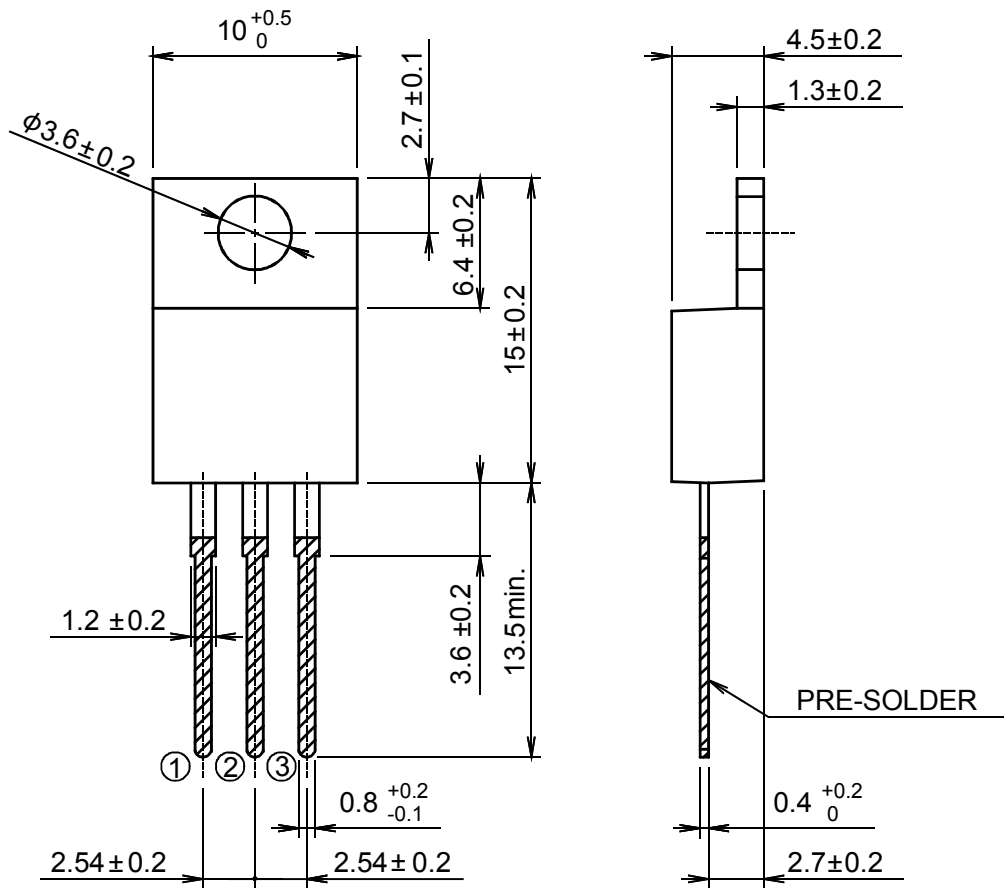


Fig.7 Operating waveform of Reverse recovery Test

## ■ Outview: TO-220 Package

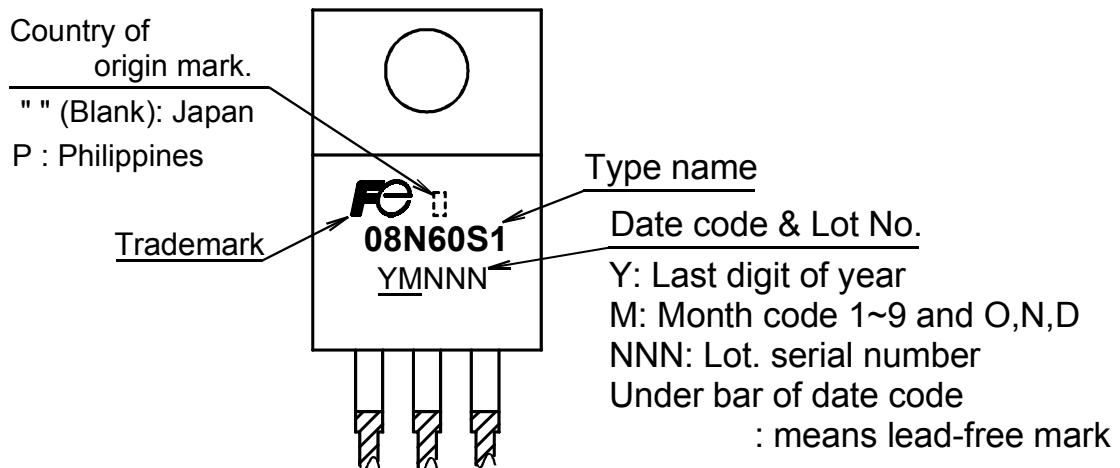
CONNECTION

- ① GATE
- ② DRAIN
- ③ SOURCE

JEDEC : TO-220AB

DIMENSIONS ARE IN MILLIMETERS.

## ■ Marking



\* The font (font type,size) and the trademark-size might be actually different.

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