

Super J-MOS series

N-Channel enhancement mode power MOSFET

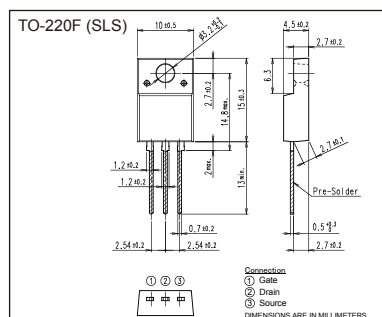
■ Features

Pb-free lead terminal
RoHS compliant

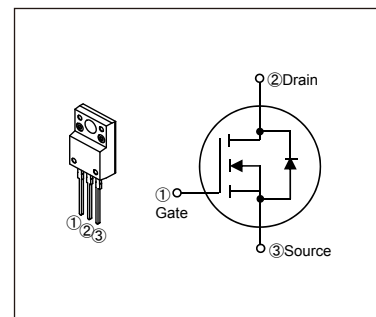
■ Applications

For switching

■ Outline Drawings [mm]



■ Equivalent circuit schematic



■ Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30V$
Continuous Drain Current	I_D	± 13	A	$T_c=25^{\circ}C$ Note*1
		± 8.2	A	$T_c=100^{\circ}C$ Note*1
Pulsed Drain Current	I_{DP}	± 39	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	3.4	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E_{AS}	452.1	mJ	Note *3
Maximum Drain-Source dV/dt	d V_{DS} /dt	50	kV/ μ s	$V_{DS} \leq 600V$
Peak Diode Recovery dV/dt	dV/dt	15	kV/ μ s	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/ μ s	Note *5
Maximum Power Dissipation	P_D	2.16	W	$T_a=25^{\circ}C$
		43		$T_c=25^{\circ}C$
Operating and Storage Temperature range	T_{ch}	150	$^{\circ}C$	
	T_{stg}	-55 to +150	$^{\circ}C$	
Isolation Voltage	V_{iso}	2	kVrms	t=60sec, f=60Hz

Note *1 : Limited by maximum channel temperature.

Note *2 : $T_{ch} \leq 150^{\circ}\text{C}$, See Fig.1 and Fig.2

Note *3 : Starting $T_{ch}=25^{\circ}\text{C}$, $I_{AS}=2.1\text{A}$, $L=188\text{mH}$, $V_{DD}=60\text{V}$, $R_G=50\Omega$, See Fig.1 and Fig.2
EAS limited by maximum channel temperature and avalanche current.

Note *4: $|V_{DS}| \leq |V_{DD}|$, $-di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 400 \text{ V}$, $V_{peak} \leq BV_{DSS}$, $T_{ch} \leq 150^\circ\text{C}$.

Note *5: $|I_F| \leq |I_D$, $dV/dt=15kV/\mu s$, $V_{DD} \leq 400V$, $V_{peak} \leq BV_{DSS}$, $T_{ch} \leq 150^\circ C$.

■ Electrical Characteristics at T_c=25°C (unless otherwise specified)

- Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A$ $V_{GS}=0V$		600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D=250\mu A$ $V_{DS}=V_{GS}$		2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=600V$ $V_{GS}=0V$	$T_{ch}=25^{\circ}C$	-	-	25	μA
		$V_{DS}=480V$ $V_{GS}=0V$	$T_{ch}=125^{\circ}C$	-	-	250	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}= \pm 30V$ $V_{DS}=0V$		-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D=6.5A$ $V_{GS}=10V$		-	0.237	0.28	Ω
Gate resistance	R_G	f=1MHz, open drain		-	3.5	-	Ω

• Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g_{fs}	$I_D=6.5A$ $V_{DS}=25V$	6	12.5	-	S
Input Capacitance	C_{iss}	$V_{DS}=10V$	-	1010	-	pF
Output Capacitance	C_{oss}	$V_{GS}=0V$	-	2160	-	
Reverse Transfer Capacitance	C_{rss}	$f=1MHz$	-	200	-	
Effective output capacitance, energy related (Note *6)	$C_{o(er)}$	$V_{GS}=0V$ $V_{DS}=0\ldots 480V$	-	70	-	
Effective output capacitance, time related (Note *7)	$C_{o(tr)}$	$V_{GS}=0V$ $V_{DS}=0\ldots 480V$ $I_D=constant$	-	220	-	
Turn-On Time	$t_{d(on)}$	$V_{DD}=400V, V_{GS}=10V/0V$ $I_D=6.5A, R_G=24\Omega$ See Fig.3 and Fig.4	-	13	-	ns
	t_r		-	38	-	
Turn-Off Time	$t_{d(off)}$		-	104	-	
	t_f		-	16	-	
Total Gate Charge	Q_G	$V_{DD}=480V, I_D=13A$ $V_{GS}=10V$ See Fig.5	-	35	-	nC
Gate-Source Charge	Q_{GS}		-	10	-	
Gate-Drain Charge	Q_{GD}		-	10.5	-	
Drain-Source crossover Charge	Q_{SW}		-	6.5	-	

Note *6 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS} .

Note *7 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS} .

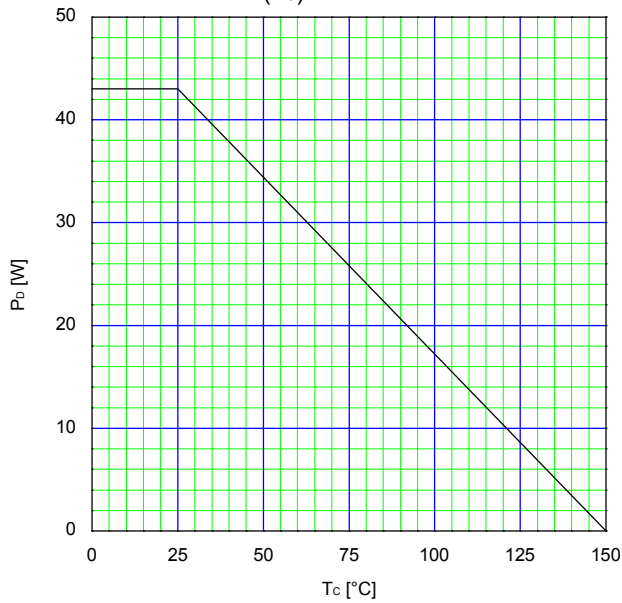
• Reverse Diode

Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	I_{AV}	$L=44.3mH, T_{ch}=25^\circ C$ See Fig.1 and Fig.2	3.4	-	-	A
Diode Forward On-Voltage	V_{SD}	$I_F=13A, V_{GS}=0V$ $T_{ch}=25^\circ C$	-	0.9	1.35	V
Reverse Recovery Time	t_{rr}	$I_F=13A, V_{DD}=400V$ $-di/dt=100A/\mu s$		330	-	ns
Reverse Recovery Charge	Q_{rr}	$V_{GS(Q1)}=short, V_{GS(Q2)}=10V/0V$ $R_G=330\Omega$ $T_{ch}=25^\circ C$	-	4.5	-	μC
Peak Reverse Recovery Current	I_{rp}	See Fig.6 and Fig.7	-	25	-	A

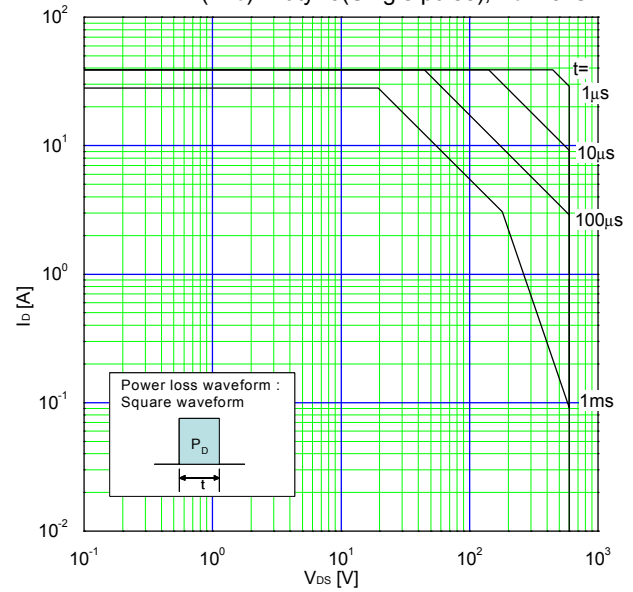
■ Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	2.9	$^\circ C/W$
Channel to Ambient	$R_{th(ch-a)}$	-	-	58	$^\circ C/W$

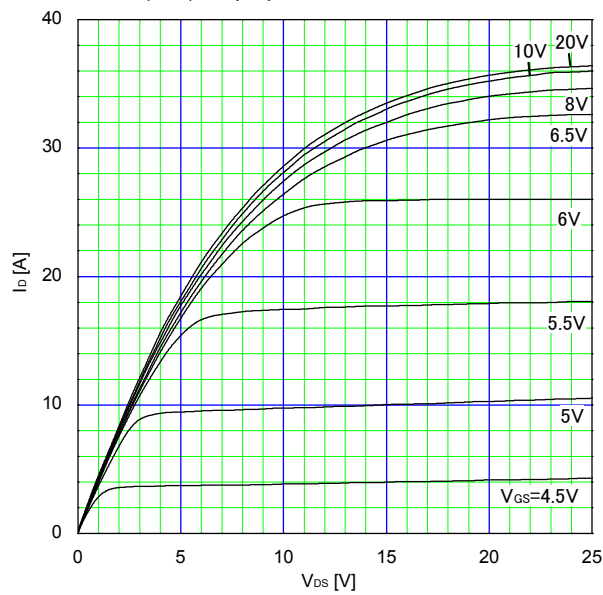
Allowable Power Dissipation
 $P_D = f(T_C)$



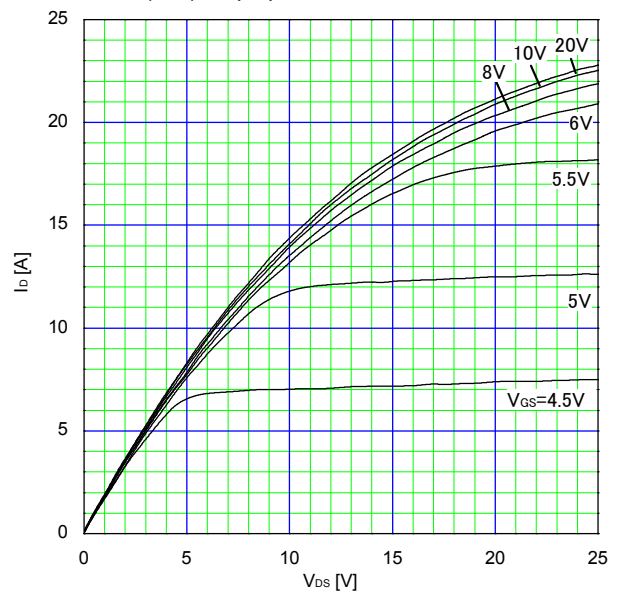
Safe Operating Area
 $I_D = f(V_{DS})$: Duty=0 (Single pulse), $T_C = 25^\circ\text{C}$



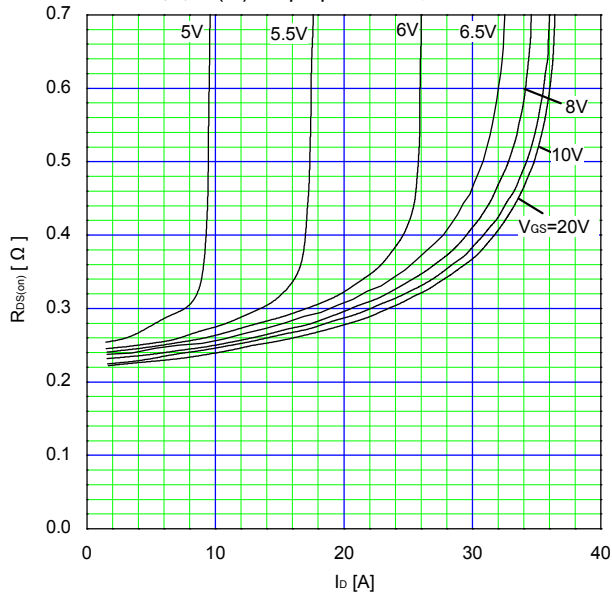
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80 μs pulse test, $T_{ch} = 25^\circ\text{C}$



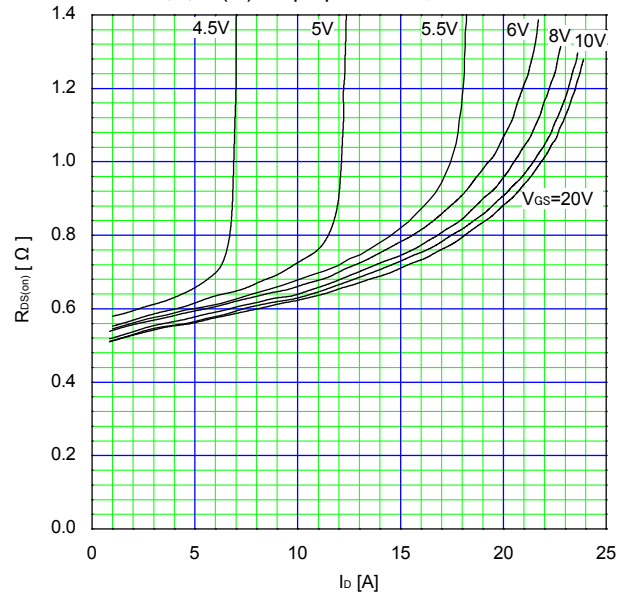
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80 μs pulse test, $T_{ch} = 150^\circ\text{C}$



Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80 μs pulse test, $T_{ch} = 25^\circ\text{C}$

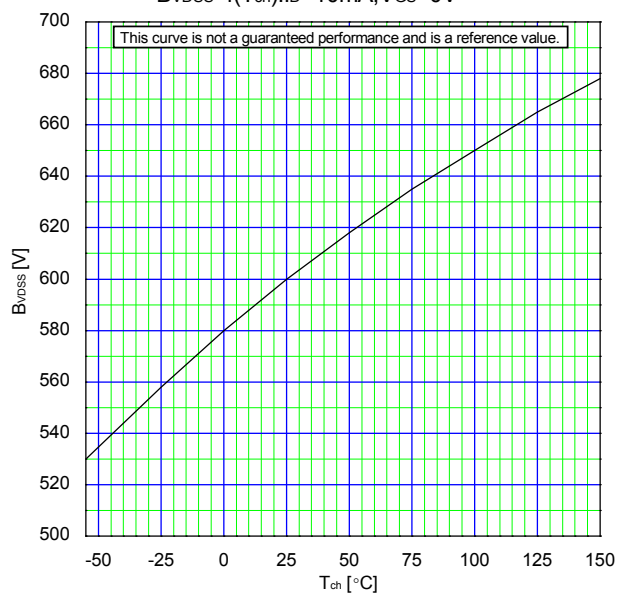


Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80 μs pulse test, $T_{ch} = 150^\circ\text{C}$



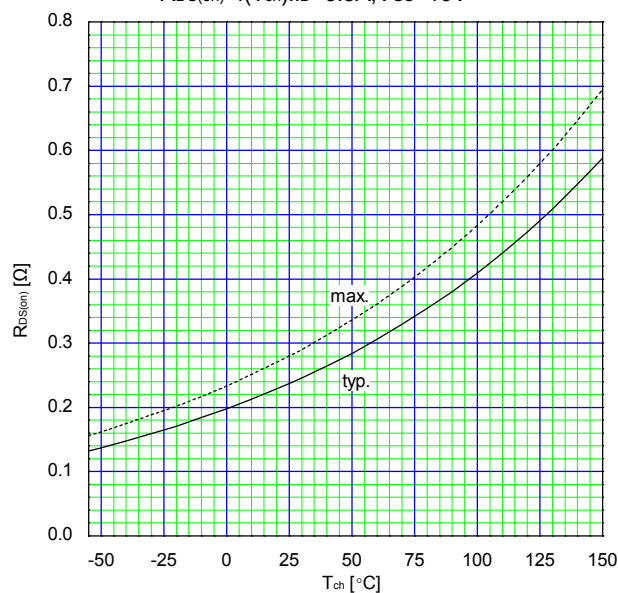
Drain-Source Breakdown Voltage

$$B_{VDS} = f(T_{ch}): I_D = 10\text{mA}, V_{GS} = 0\text{V}$$

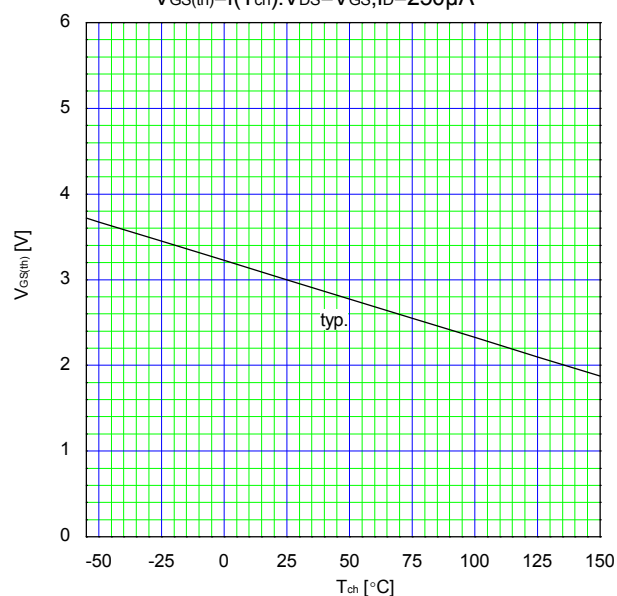


Drain-Source On-state Resistance

$$R_{DS(on)} = f(T_{ch}): I_D = 6.5\text{A}, V_{GS} = 10\text{V}$$

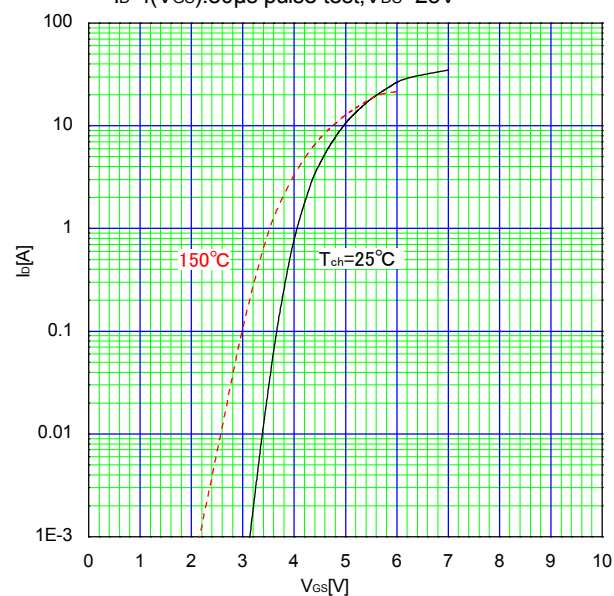
Gate Threshold Voltage vs. T_{ch}

$$V_{GS(th)} = f(T_{ch}): V_{DS} = V_{GS}, I_D = 250\mu\text{A}$$



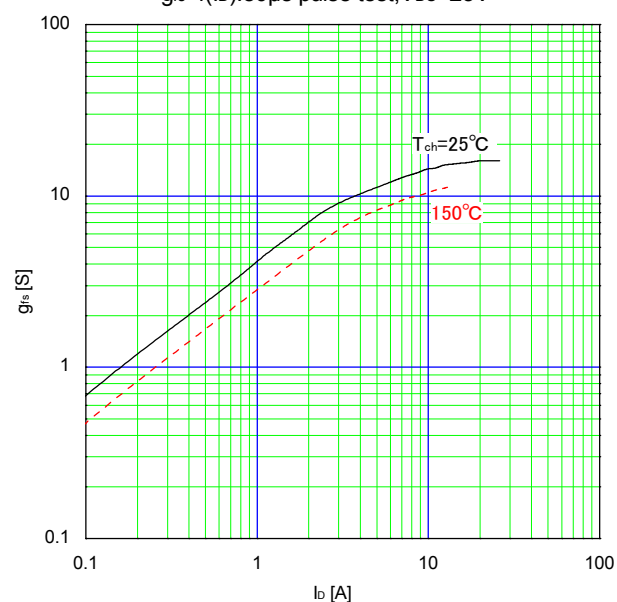
Typical Transfer Characteristic

$$I_D = f(V_{GS}): 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



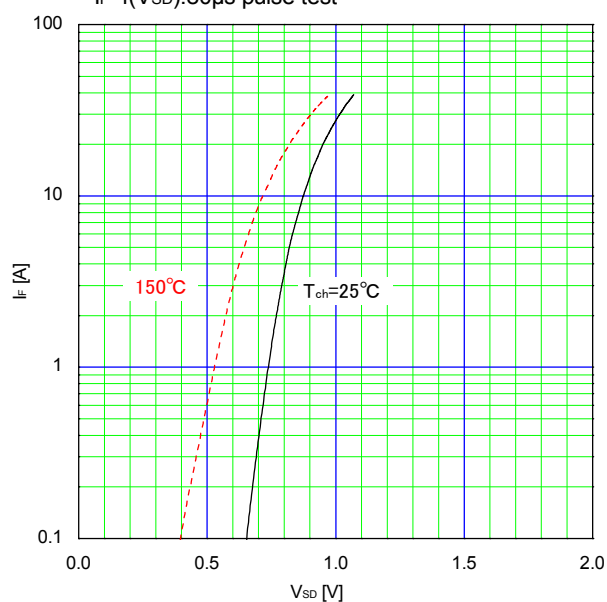
Typical Transconductance

$$g_{fs} = f(I_D): 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$

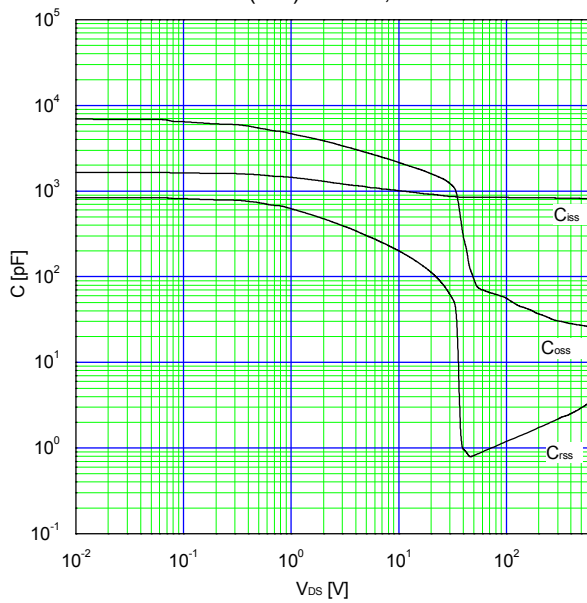


Typical Forward Characteristics of Reverse Diode

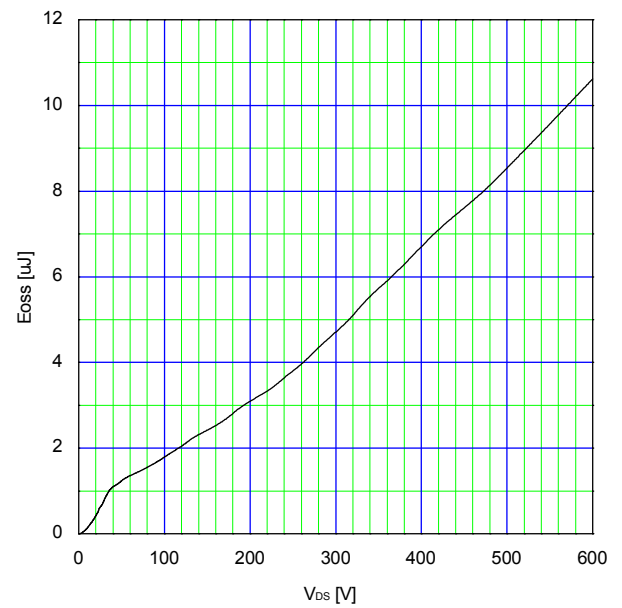
$$I_F = f(V_{SD}): 80\mu\text{s pulse test}$$



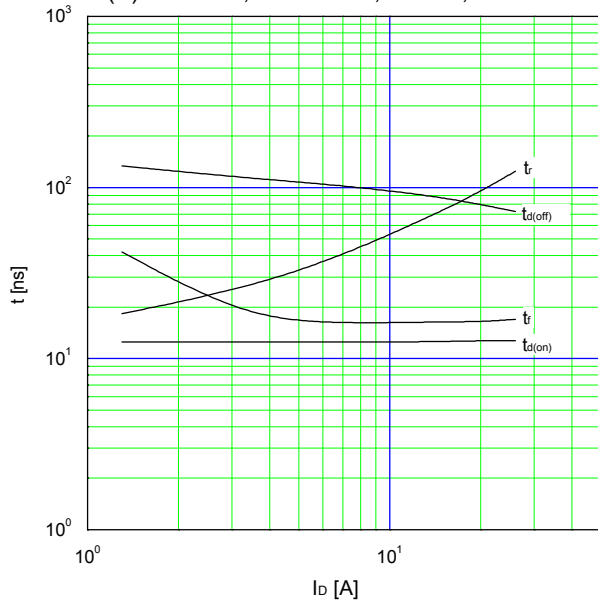
Typical Capacitance
 $C=f(V_{DS}):V_{GS}=0V, f=1MHz$



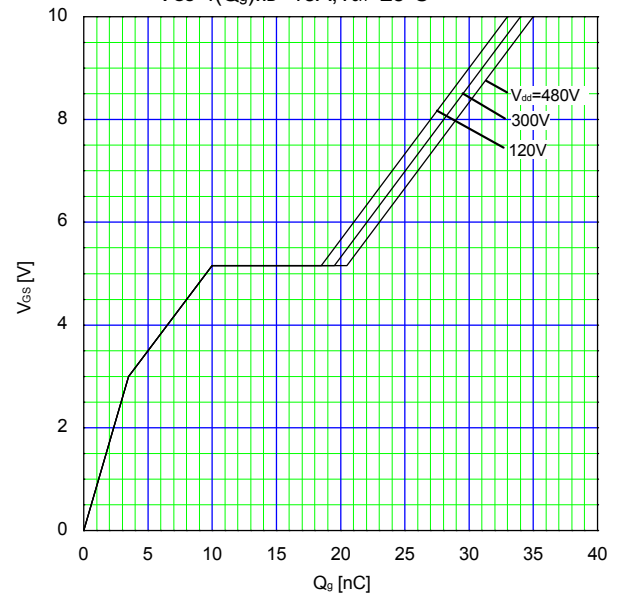
Typical Coss stored energy



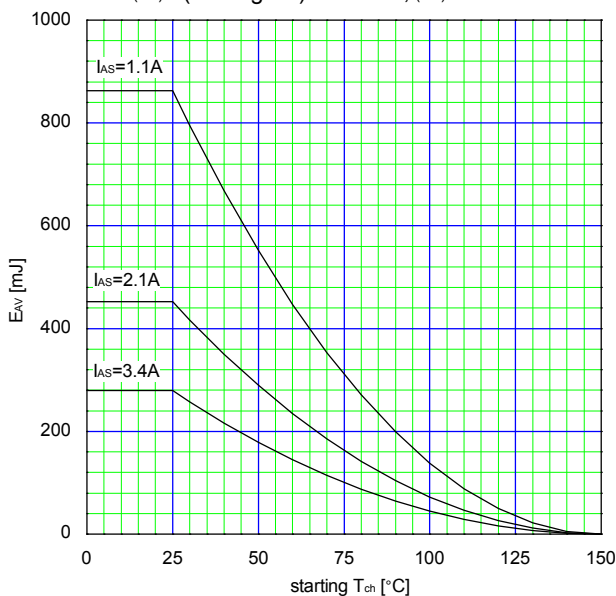
Typical Switching Characteristics vs. I_D $T_{ch}=25^\circ C$
 $t=f(I_D):V_{dd}=400V, V_{GS}=10V/0V, R_G=24\Omega, L=500\mu H$



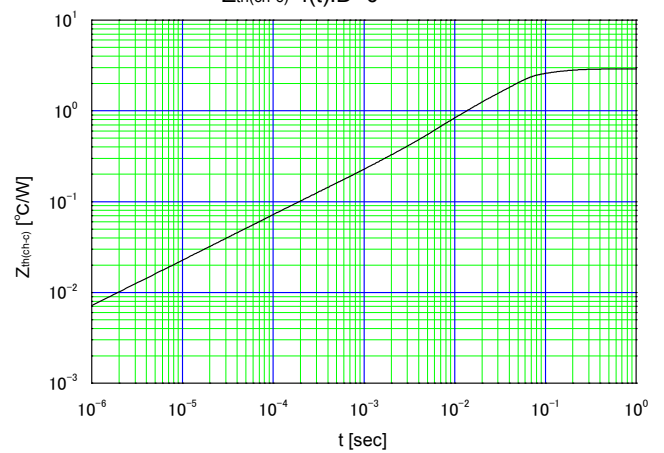
Typical Gate Charge Characteristics
 $V_{GS}=f(Q_g):I_D=13A, T_{ch}=25^\circ C$



Maximum Avalanche Energy vs. starting T_{ch}
 $E_{(AV)}=f(\text{starting } T_{ch}):V_{CC}=60V, I_{(AV)} \leq 3.4A$



Transient Thermal Impedance
 $Z_{th(ch-c)}=f(t):D=0$



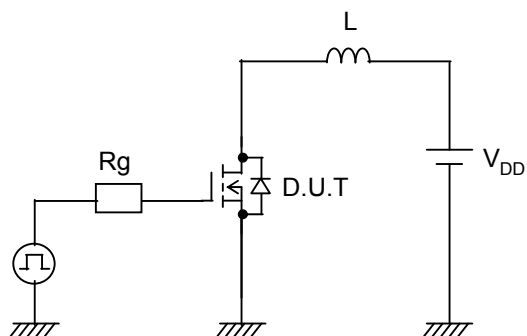


Fig.1 Avalanche Test circuit

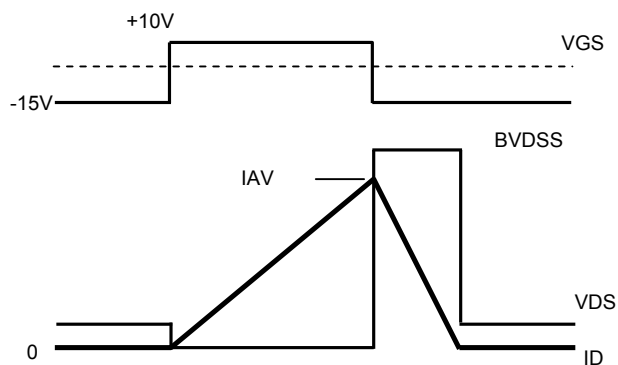


Fig.2 Operating waveforms of Avalanche Test

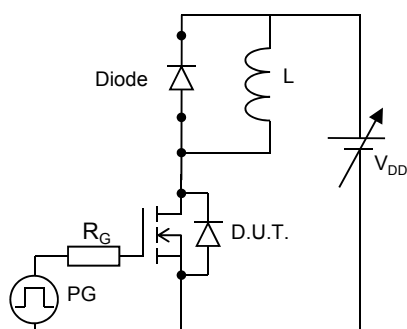


Fig.3 Switching Test circuit

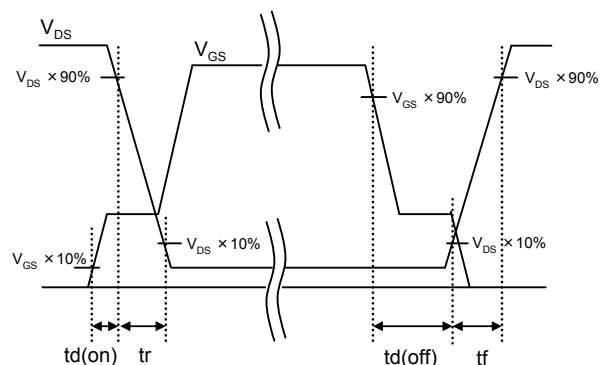


Fig.4 Operating waveform of Switching Test

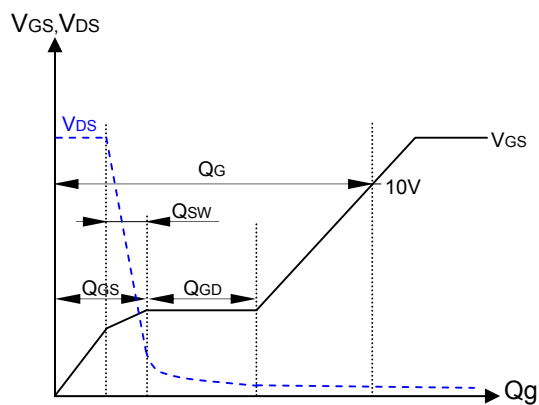


Fig.5 Operating waveform of Gate charge Test

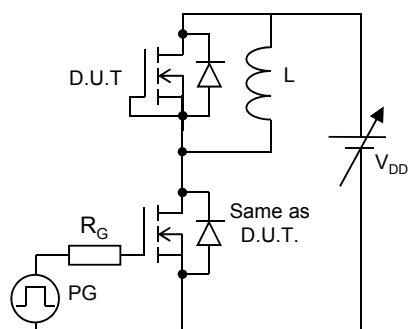


Fig.6 Reverse recovery Test circuit

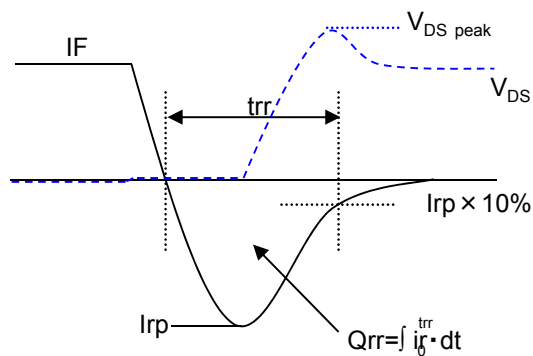
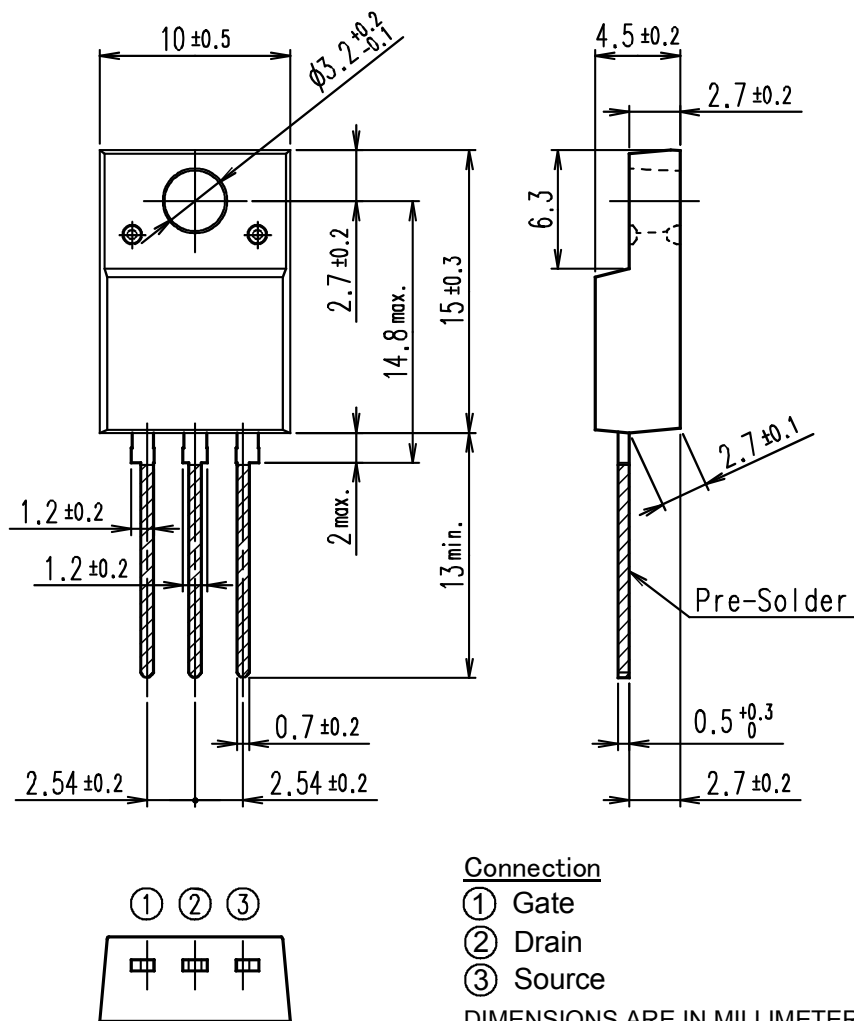
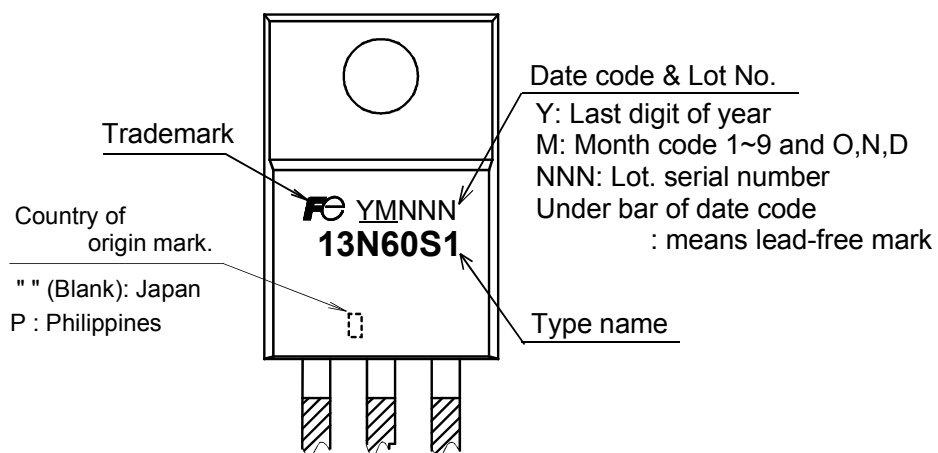


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-220F (SLS) Package



■ Marking



* The font (font type,size) and the trademark-size might be actually different.

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