

FMV35N60S1FD

FUJI POWER MOSFET

Super J-MOS series

N-Channel enhancement mode power MOSFET

■ Features

Low on-state resistance Low switching loss easy to use (more controllabe switching dV/dt by Rg)

Applications

UPS

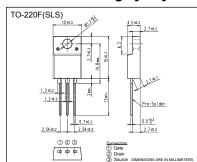
Server

Telecom

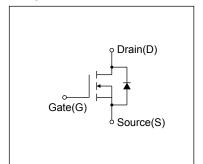
Power conditioner system

Power supply

Outline Drawings [mm]



■ Equivalent circuit schematic



■ Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain Sauras Valtara	V _{DS}	600	V	
Drain-Source Voltage	V _{DSX}	600	V	V _{GS} =-30V
Continuous Drain Current		±35	Α	Tc=25°C Note*1
Continuous Drain Current	lo lo	±22	Α	Tc=100°C Note*1
Pulsed Drain Current	IDP	±105	Α	Note*1
Gate-Source Voltage	Vgs	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	lar	6.6	А	Note *2
Non-Repetitive Maximum Avalanche Energy	Eas	1239.6	mJ	Note *3
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	kV/μs	V _{DS} ≤ 600V
Peak Diode Recovery dV/dt	dV/dt	30	kV/µs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *5
Marrian Davida Dispination	Po	2.16	W	Ta=25°C
Maximum Power Dissipation		110	VV	Tc=25°C
One matter a send Ottomore Towns and the many	Tch	150	°C	
Operating and Storage Temperature range	T _{stg}	-55 to +150	°C	

■ Electrical Characteristics at T_c=25°C (unless otherwise specified)

Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V		600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I _D =1.3mA V _{DS} =V _{GS}		3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	loss	V _{DS} =600V V _{GS} =0V	T _{ch} =25°C	-	-	25	- μΑ
		V _{DS} =480V V _{GS} =0V	T _{ch} =125°C	-	190	-	
Gate-Source Leakage Current	Igss	V _{GS} = ± 30V V _{DS} =0V		-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =17.5A V _{GS} =10V		-	0.089	0.105	Ω
Gate resistance	R _G	f=1MHz, open drain		-	1.1	-	Ω

Note *1 : Limited by maximum channel temperature.

Note *2 : T_{ch≤1}50°C, See Fig.1 and Fig.2

Note *3 : Starting T_{ch=2}5°C, I_{AS=4}A, L=142mH, V_{DD=6}0V, R_G=50Ω, See Fig.1 and Fig.2

E_{AS} limited by maximum channel temperature and avalanche current.

Note *4 : I_{F≤-}I_D, -di/dt=100A/µs, V_{DS} p_{eak}≤600V, T_{ch}≤150°C.

Note *5 : I_{F≤-}I_D, dV/dt=30kV/µs, V_{DS} p_{eak}≤600V, T_{ch}≤150°C.

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Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g _{fs}	I _D =17.5A V _{DS} =25V	13.5	27	-	S
Input Capacitance	Ciss	V _{DS} =400V	-	2530	-	
Output Capacitance	Coss	V _{GS} =0V	-	75	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	5.5	-	
Effective output capacitance, energy related (Note *6)	C _{o(er)}	V _{SS} =0V V _{DS} =0400V	-	195	-	pF
Effective output capacitance, time related (Note *7)	Co(tr)	V _{GS} =0V V _{DS} =0400V ID=constant	-	- 670	-	
Turn-On Time	t _{d(on)}	V_{DD} =400V, V_{GS} =10V I_D =17.5A, R_G =18 Ω See Fig.3 and Fig.4	-	116	-	ns
	tr		-	28	-	
Turn-Off Time	t _{d(off)}		-	163	-	
	tf		-	18	-	
Total Gate Charge	Q _G	V _{DD} =400V, I _D =35A V _{GS} =10V See Fig.5	-	92	-	
Gate-Source Charge	Q _{GS}		-	24.5	-	nC
Gate-Drain Charge	Q _{GD}		-	38	-	IIC
Drain-Source crossover Charge	Qsw		-	13	-	

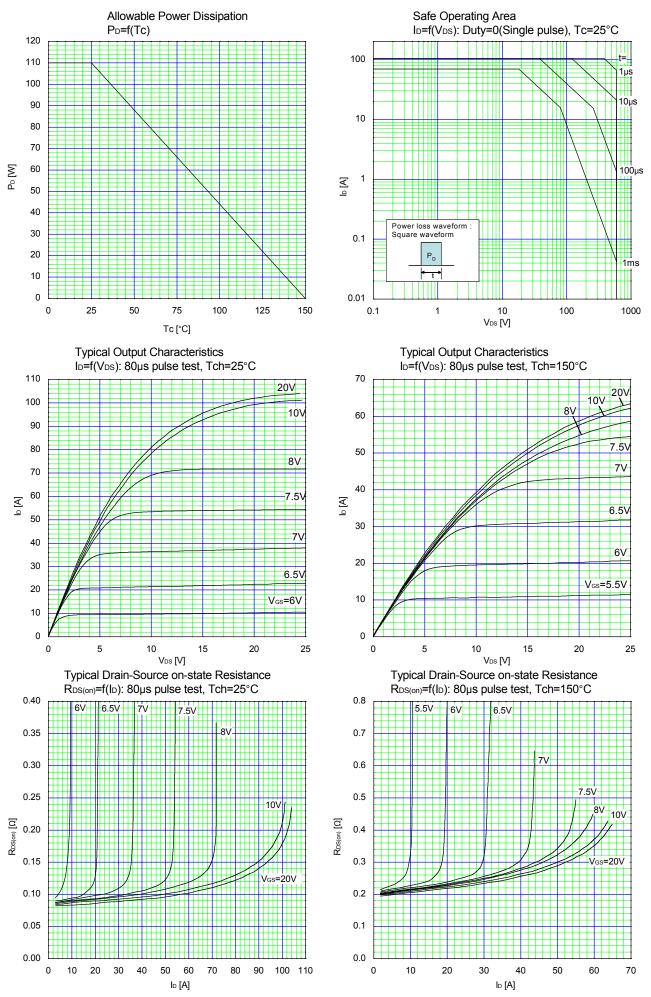
Note *6 : $C_{\text{o(er)}}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V. Note *7 : $C_{\text{o(er)}}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

• Reverse Diode

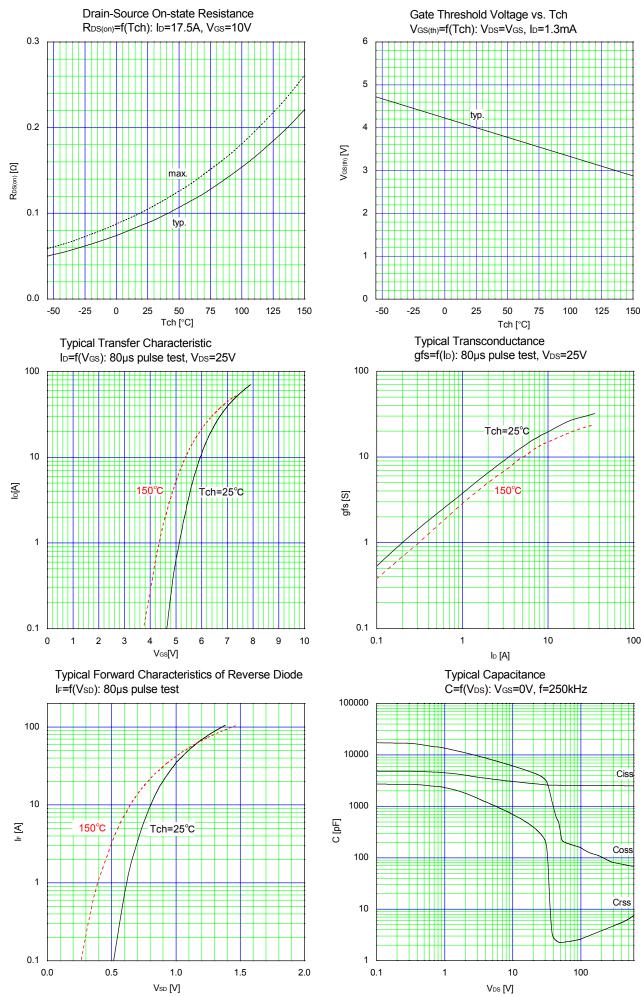
Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	lav	L=31.6mH,Tch=25°C See Fig.1 and Fig.2	6.6	-	-	А
Diode Forward On-Voltage	VsD	I _F =35A,V _{GS} =0V T _{Ch} =25°C	-	1	1.35	V
Reverse Recovery Time	trr	I _F =35A, V _{DD} =400V -di/dt=100A/μs R _G =150Ω, T _{ch} =25°C See Fig.6 and Fig.7	-	185	-	ns
Reverse Recovery Charge	Qrr		-	1.3	-	μC
Peak Reverse Recovery Current	Irp		-	14	-	А

■ Thermal Resistance

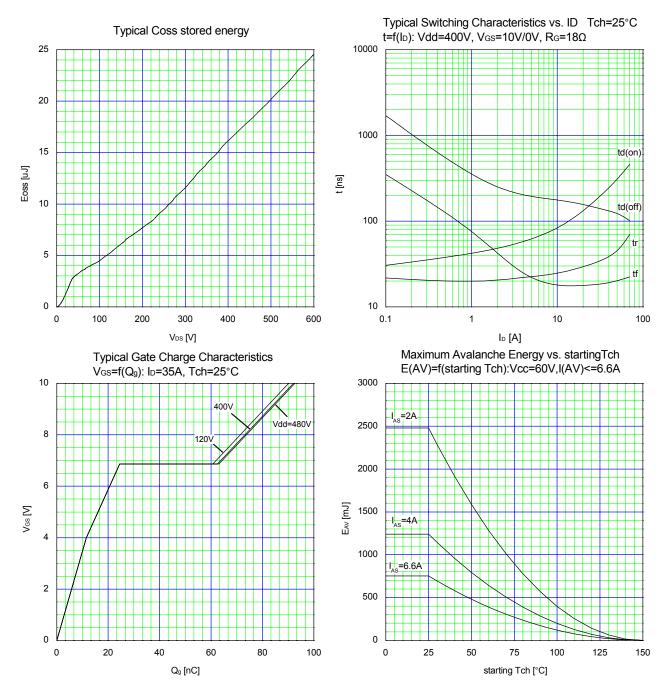
Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	R _{th(ch-c)}	-	-	1.14	°C/W
Channel to Ambient	R _{th(ch-a)}	-	-	58	°C/W

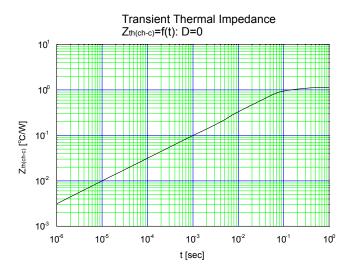


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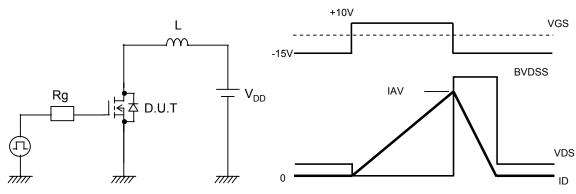


Fig.1 Avalanche Test circuit

Fig.2 Operating waveforms of Avalanche Test

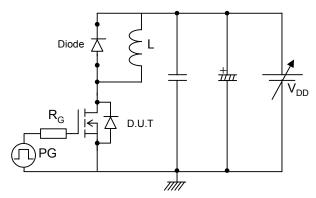


Fig.3 Switching Test circuit

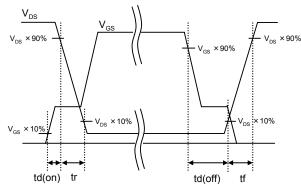


Fig.4 Operating waveform of Switching Test

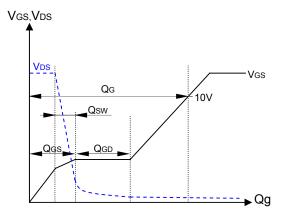


Fig.5 Operating waveform of Gate charge Test

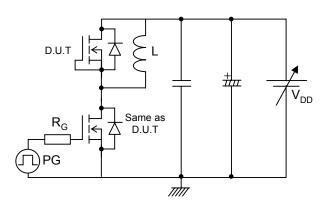


Fig.6 Reverse recovery Test circuit

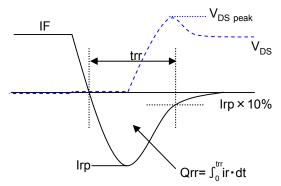
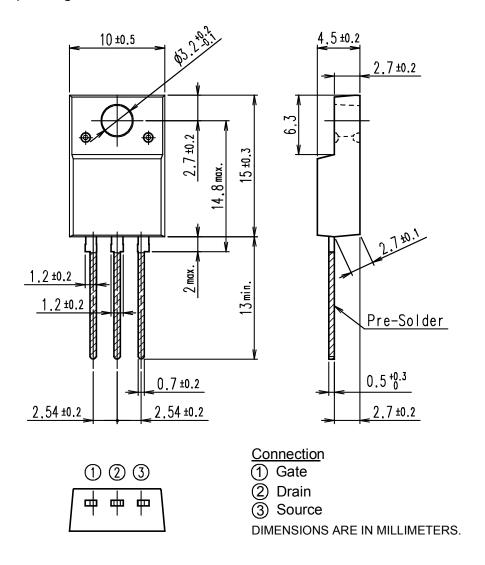
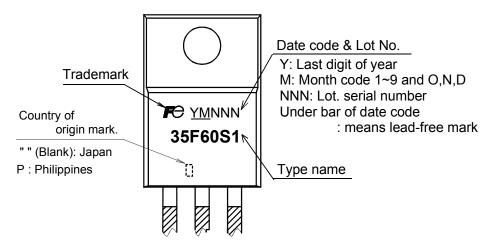


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-220F(SLS) Package



■ Marking



* The font (font type,size) and the trademark-size might be actually different.

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