

Super FAP-E^{3S} Low Qg Built-in FRED series

N-Channel enhancement mode power MOSFET

■ Features

Low on-state resistance
Low switching loss
easy to use
(more controllable switching dV/dt by R_g)
The reliability trial conforms to AEC Q101.
100% avalanche tested

■ Applications

Automotive switching applications

■ Absolute Maximum Ratings at $T_c=25^\circ\text{C}$ (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30\text{V}$
Continuous Drain Current	I_D	± 35	A	
Pulsed Drain Current	I_{DP}	± 140	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Non-Repetitive Maximum Avalanche current	I_{AS}	35	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E_{AS}	850	mJ	Note*2
Peak Diode Recovery dV/dt	dV/dt	4.7	kV/ μs	Note*3
Peak Diode Recovery di/dt	$-di/dt$	100	A/ μs	Note*4
Maximum Power Dissipation	P_D	570	W	
Operating and Storage Temperature range	T_{ch}	150	$^\circ\text{C}$	
	T_{stg}	-55 to +150	$^\circ\text{C}$	

Note*1 : $T_{ch} \leq 150^\circ\text{C}$, See Fig.1 and Fig.2

Note*2 : Starting $T_{ch}=25^\circ\text{C}$, $L=1330\mu\text{H}$, $V_{CC}=60\text{V}$, $R_G=50\Omega$, See Fig.1 and Fig.2

E_{AS} limited by maximum channel temperature and avalanche current.

See to Avalanche Energy graph of page 5

Note*3 : $IF \leq -I_D$, $-di/dt=100\text{A}/\mu\text{s}$, $V_{CC} \leq BV_{DSS}$, $T_{ch} \leq 150^\circ\text{C}$

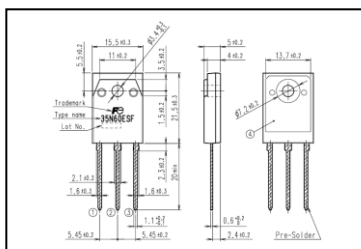
Note*4 : $IF \leq -I_D$, $dV/dt=4.7\text{kV}/\mu\text{s}$, $V_{CC} \leq BV_{DSS}$, $T_{ch} \leq 150^\circ\text{C}$

■ Electrical Characteristics at $T_c=25^\circ\text{C}$ (unless otherwise specified)

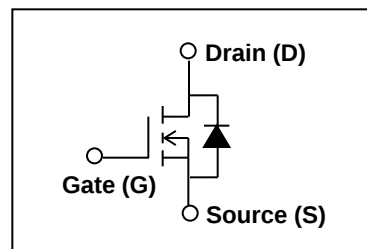
Static Ratings

Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=1\text{mA}$ $V_{GS}=0\text{V}$	600	—	—	V
	BV_{DSX}	$I_D=1\text{mA}$ $V_{GS}=-30\text{V}$	600	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ $V_{DS}=V_{GS}$	3.2	4.2	5.2	V
Zero Gate Voltage Drain current	I_{DSS}	$V_{DS}=600\text{V}$ $V_{GS}=0\text{V}$ $T_a=25^\circ\text{C}$	—	2	10	μA
		$V_{DS}=480\text{V}$ $V_{GS}=0\text{V}$ $T_a=125^\circ\text{C}$	—	0.7	2	mA
Gate-Source Leakage current	I_{GSS}	$V_{GS}=30\text{V}$ $V_{DS}=0\text{V}$	—	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D=17.5\text{A}$ $V_{GS}=10\text{V}$	—	145	170	$\text{m}\Omega$

■ Outline Drawings [mm]



■ Equivalent circuit schematic



Dynamic Ratings

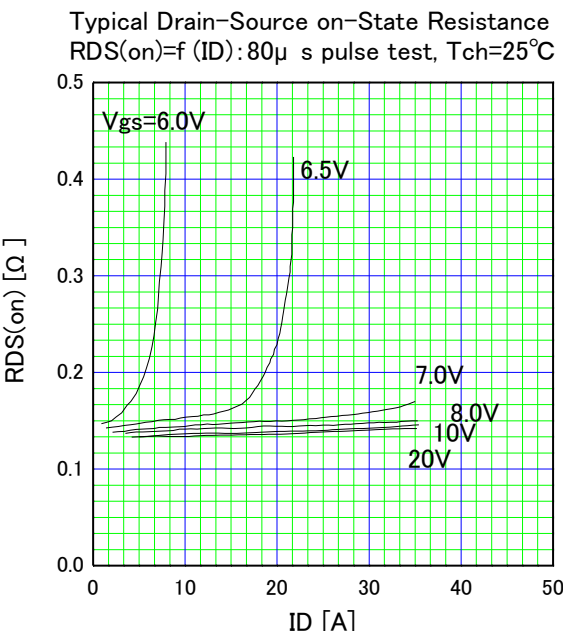
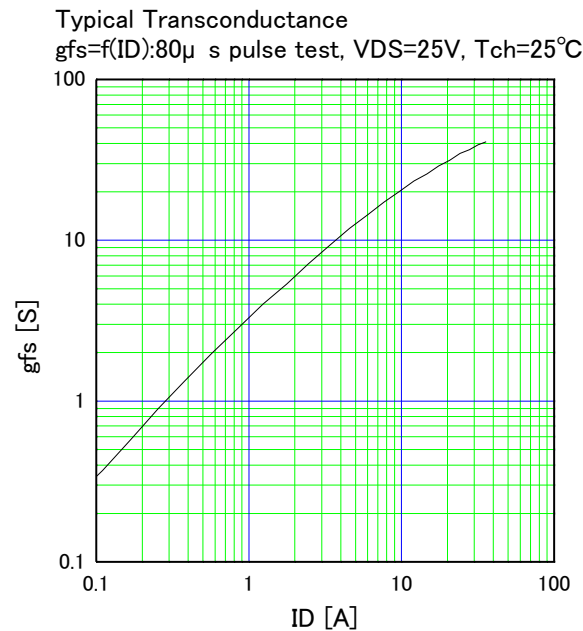
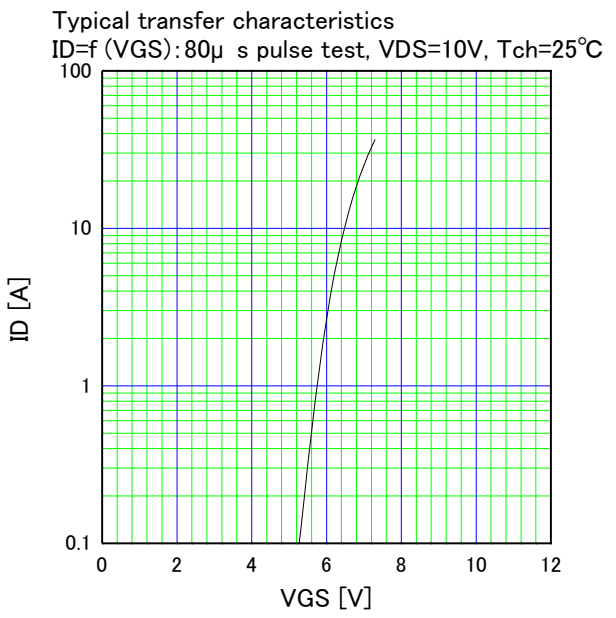
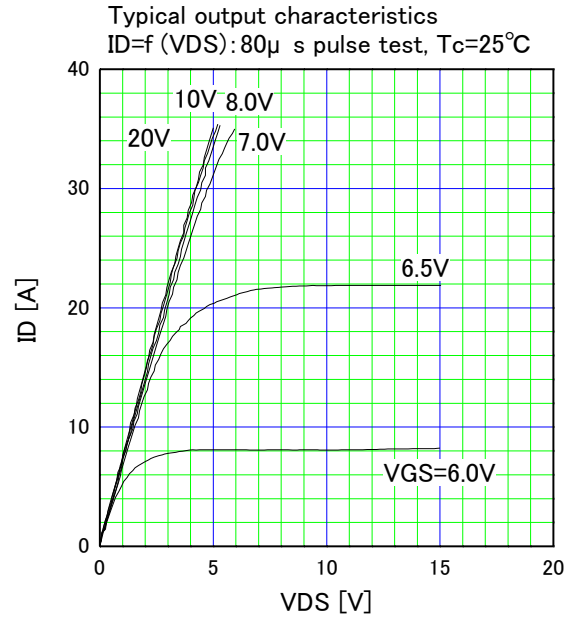
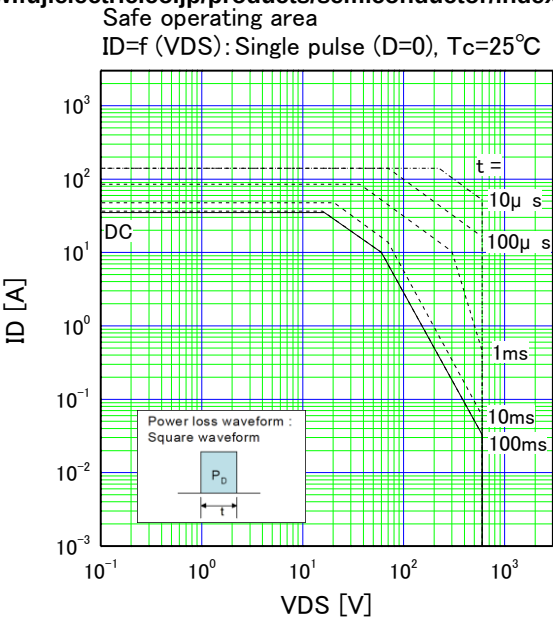
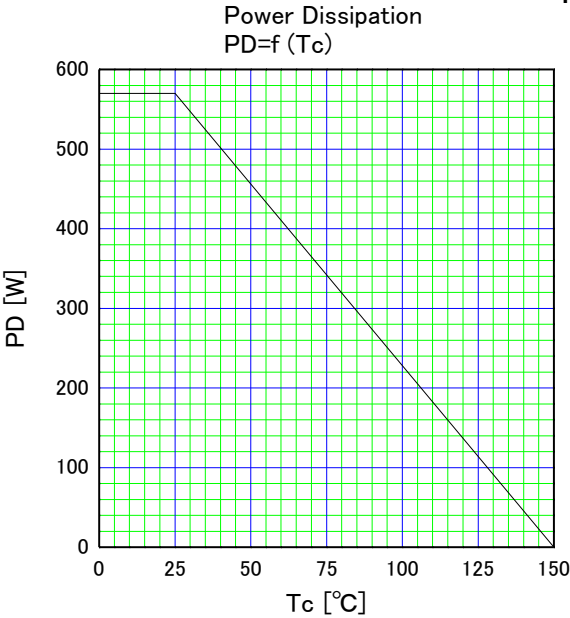
Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g_{fs}	$I_D=17.5A$ $V_{DS}=25V$	13	—	—	S
Input Capacitance	C_{iss}	$V_{DS}=25V$ $V_{GS}=0V$ $f=1MHz$	—	5900	—	pF
Output Capacitance	C_{oss}		—	660	—	
Reverse Transfer Capacitance	C_{rss}		—	39	—	
Turn-On Time	$t_{d(on)}$	$V_{CC}=300V, V_{GS}=10V$ $I_D=17.5A, R_G=10\Omega$ See Fig.3 and Fig.4	—	65	—	ns
	t_r		—	165	—	
Turn-Off Time	$t_{d(off)}$		—	160	—	
	t_f		—	35	—	
Total Gate Charge	Q_G	$V_{DD}=300V, I_D=35A$ $V_{GS}=10V$ See Fig.5	—	155	—	nC
Gate-Source Charge	Q_{GS}		—	53	—	
Gate-Drain Charge	Q_{GD}		—	72	—	

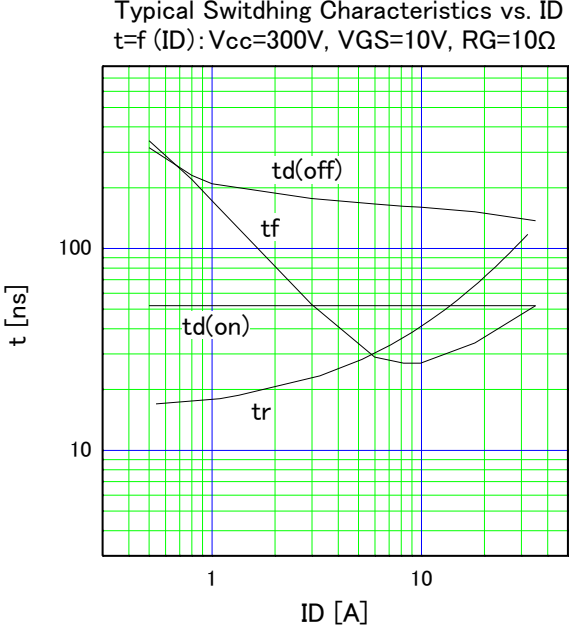
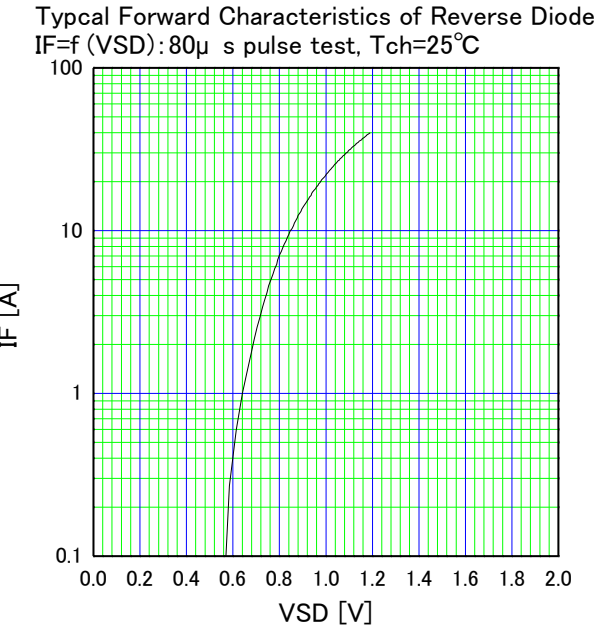
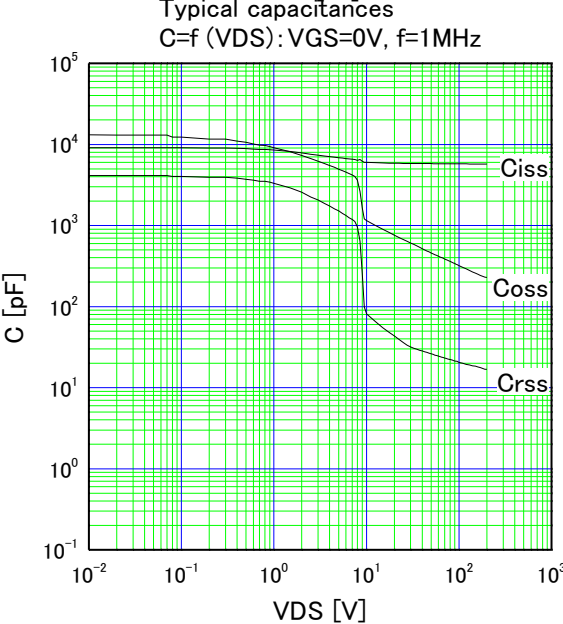
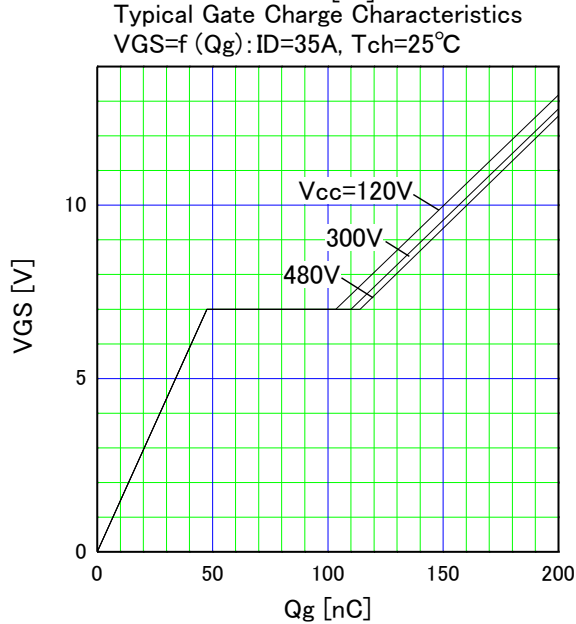
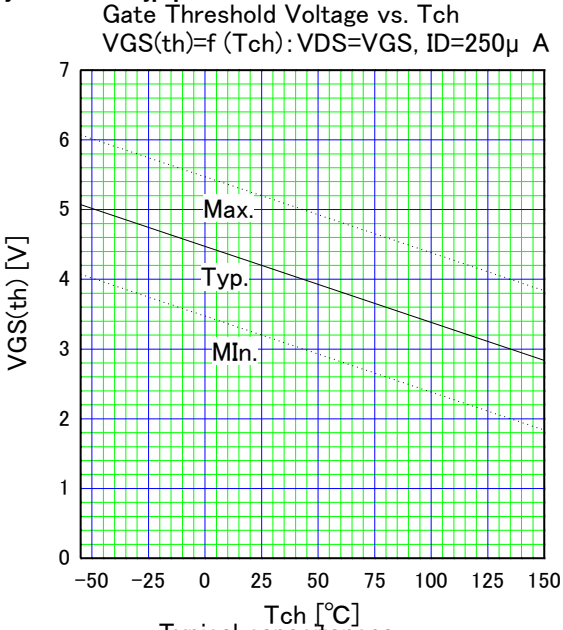
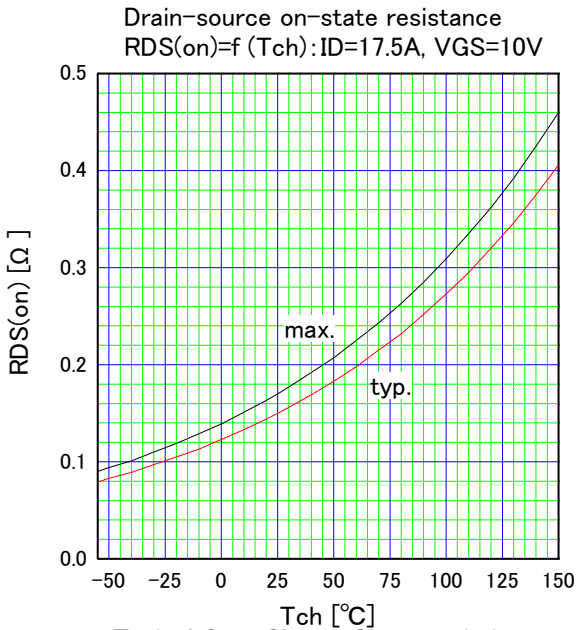
Reverse Ratings

Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Avalanche Capability	I_{AV}	$L=1330\mu H, T_{ch}=25^\circ C$ See Fig.1 and Fig.2	35	—	—	A
Diode Forward On- Voltage	V_{SD}	$I_F=35A, V_{GS}=0V$ $T_{ch}=25^\circ C$	—	1.10	1.5	V
Reverse Recovery Time	t_{rr}	$I_F=35A, V_{GS}=0V$ $-di/dt=100A/\mu s$ $T_{ch}=25^\circ C$	—	160	—	ns
Reverse Recovery Charge	Q_{rr}		—	1.0	—	μC

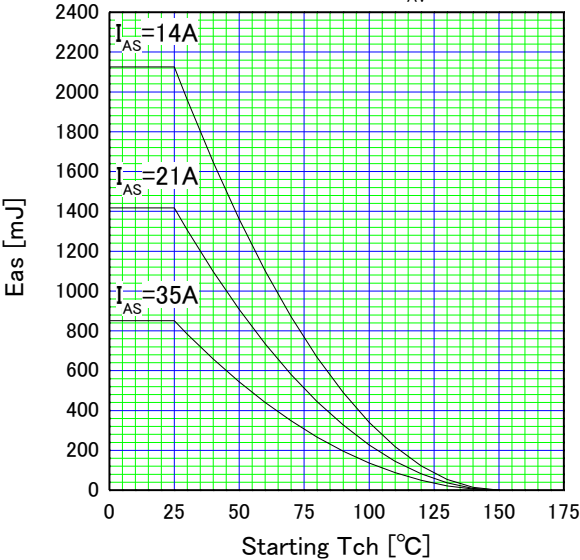
■ Thermal Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Cannel to Case	$R_{th(ch-c)}$	—	—	0.219	$^\circ C/W$
Cannel to Ambient	$R_{th(ch-a)}$	—	—	50.0	$^\circ C/W$





Maximum Avalanche energy vs. starting T_{ch}
E_{as}=f (starting T_{ch}): V_{cc}=60V, I_{AS}≤35A, single pulse



Maximum Avalanche Current vs. starting T_{ch}
I (AV) =f (starting T_{ch}), single pulse

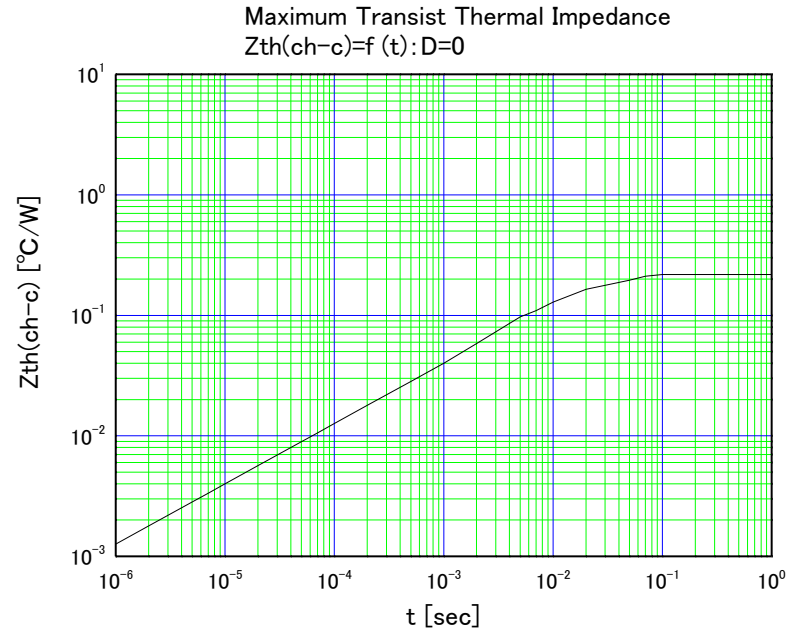
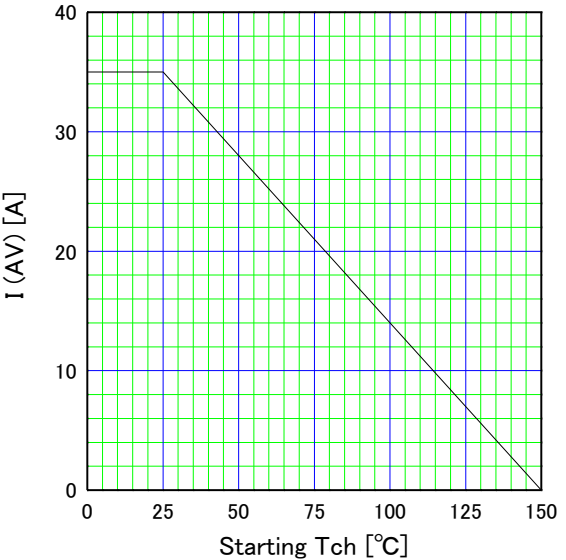


Fig.1 Avalanche Test circuit

Fig.2 Operating waveforms of Avalanche Test

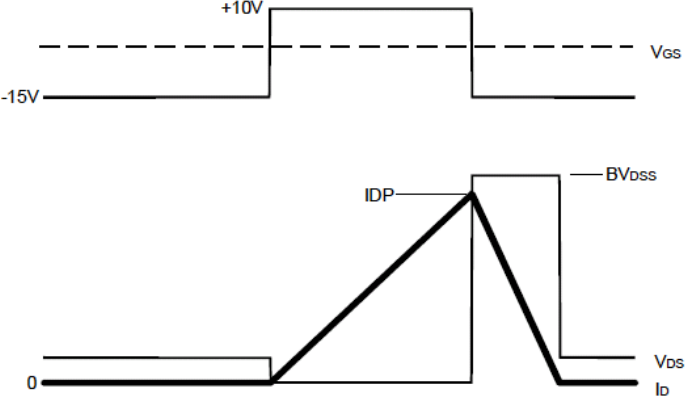
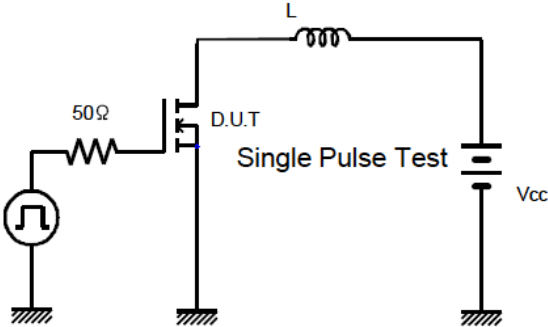


Fig.3 Switching Test circuit

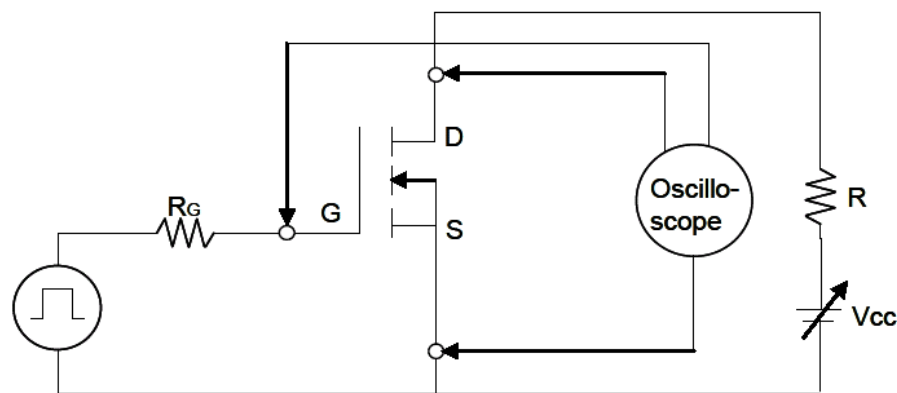


Fig.4 Operating waveform of Switching Test

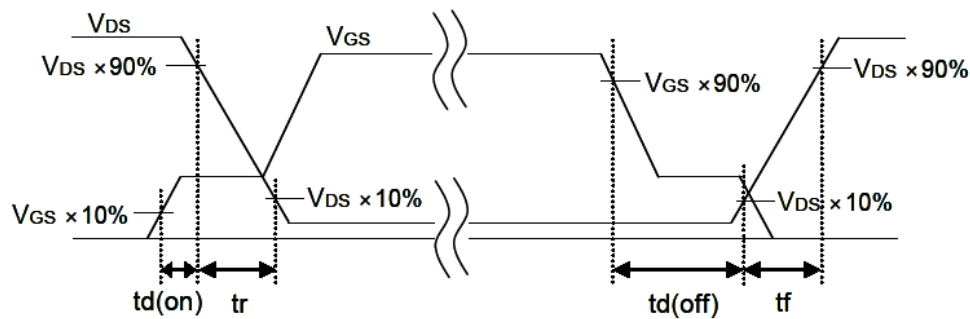


Fig.5 Operating waveform of Gate charge Test

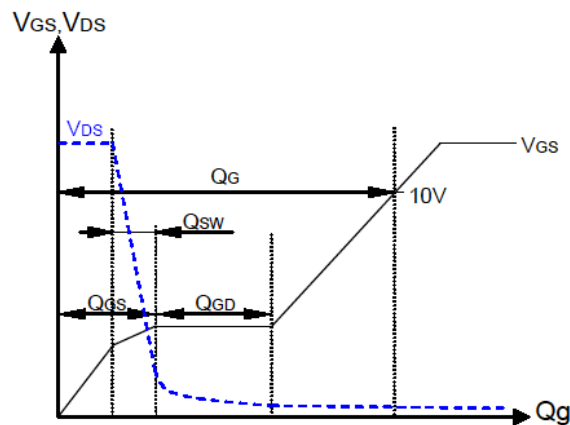
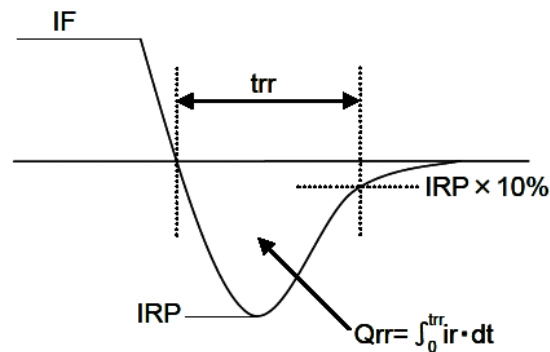


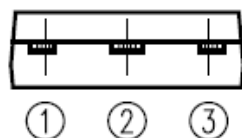
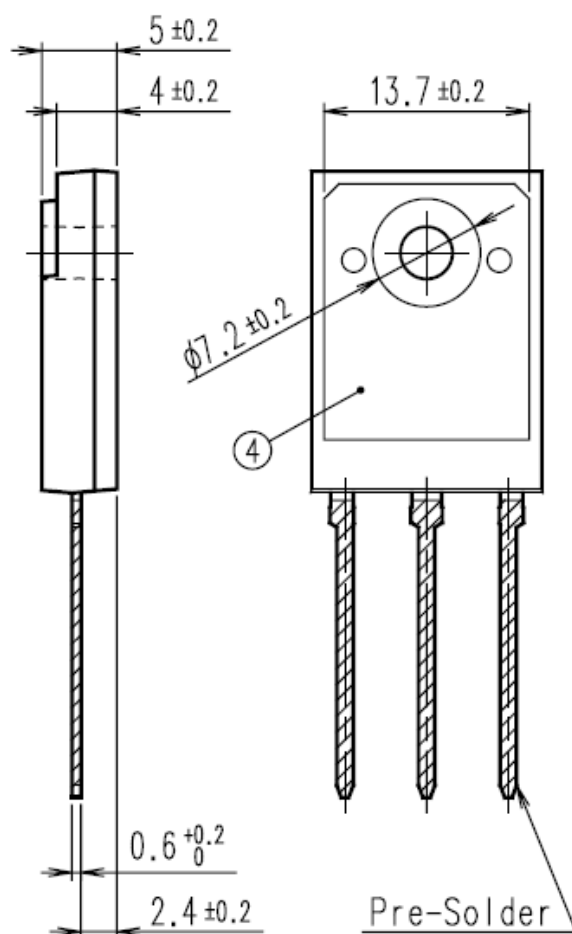
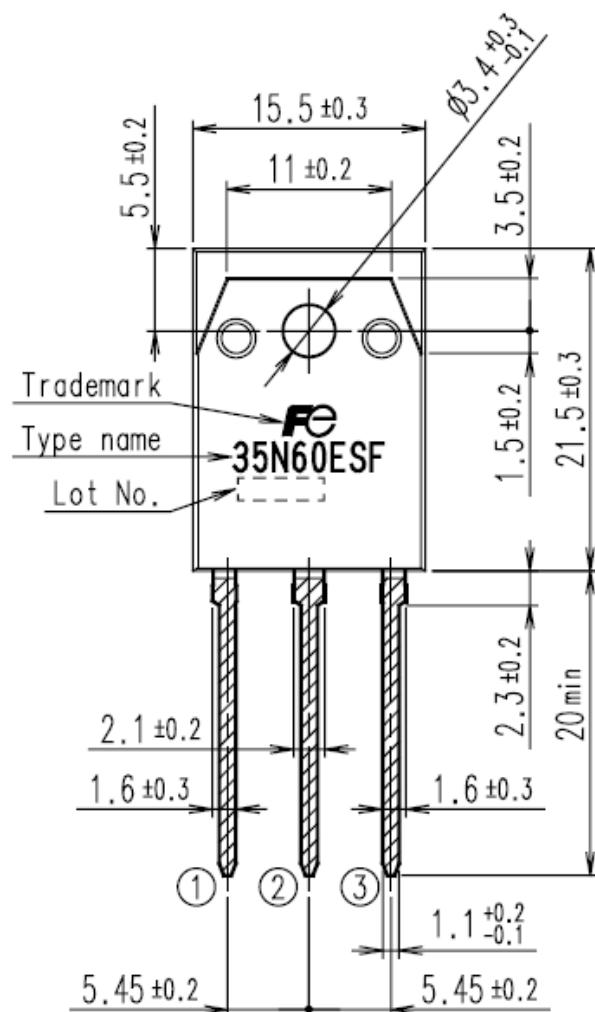
Fig.6 Operating waveform of Body diode Recovery Test



■ Out view

FUJI POWER MOSFET

TYPE : FMY35N60ESF



CONNECTION

- ① GATE
- ② ④ DRAIN
- ③ SOURCE

JEDEC: TO-247

DIMENSIONS ARE IN MILLIMETERS.

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