

Super J-MOS™ series

N-Channel enhancement mode power MOSFET

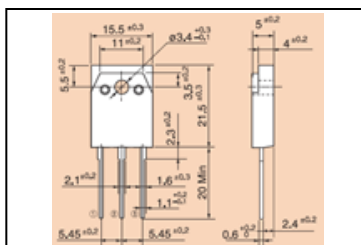
■ Features

Low on-state resistance
Low switching loss
Easy to use
(more controllable switching dV/dt by R_g)
The reliability trial conforms to AEC Q101.
100% avalanche tested

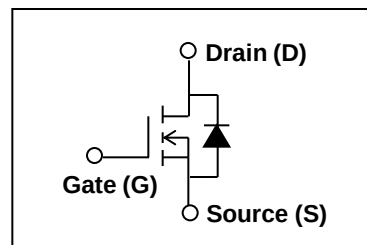
■ Applications

Automotive switching applications

■ Outline Drawings [mm]



■ Equivalent circuit schematic



■ Absolute Maximum Ratings at Tc=25°C(unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30V$
Continuous Drain Current	I_D	± 68	A	$T_c=25^{\circ}C$ Note*1
Pulsed Drain Current	I_{DP}	± 204	A	
Gate-Source Voltage	V_{GS}	30	V	
		± 30	V	AC
Non-Repetitive Maximum Avalanche current	I_{AS}	13.5	A	Note*2
Non-Repetitive Maximum Avalanche Energy	E_{AS}	3194.4	mJ	Note*3
Peak Diode Recovery dV/dt	dV/dt	15	kV/ μs	Note*4
Peak Diode Recovery di/dt	-di/dt	50	A/ μs	Note*5
Maximum Power Dissipation	P_D	545	W	$T_c=25^{\circ}C$
Operating and Storage Temperature range	T_{ch}	150	$^{\circ}C$	
	T_{stg}	-55 to +150	$^{\circ}C$	

Note*1 : Limited by maximum channel temperature

Note*2 : $T_{ch} \leq 150^{\circ}\text{C}$. See Fig.1 and Fig.2

Note*3 : Starting Tch=25°C, IAS=11A, L=19.3mH, VDD=60V, RG=50Ω, See Fig.1 and Fig.2

EAS limited by maximum channel temperature and avalanche current.

Note*4 : $IF \leq -34A$, $-di/dt = 50A/\mu s$, $V_{DD} \leq 300V$, $T_{ch} \leq 150^{\circ}C$

Note*5: $I_F \leq -34A$, $dV/dt = 15kV/\mu s$, $V_{DD} \leq 300V$, $T_{ch} \leq 150^{\circ}C$

■ **Electrical Characteristics at Tc=25°C(unless otherwise specified)**

Static Ratings

Description	Symbol	Conditions		Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A$ $V_{GS}=0V$		600	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D=250\mu A$ $V_{DS} = V_{GS}$		2.5	3.0	3.5	V
Zero Gate Voltage Drain current	I_{DSS}	$V_{DS}= 600V$ $V_{GS}=0V$	$T_a=25^{\circ}C$	—	2	10	μA
		$V_{DS}= 480V$ $V_{GS}=0V$	$T_a=150^{\circ}C$	—	1	10	
Gate-Source Leakage current	I_{GSS}	$V_{GS}=\pm 30V$ $V_{DS}= 0V$		—	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D=34A$ $V_{GS}=10V$		—	0.034	0.040	Ω

Dynamic Ratings

Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g_{fs}	$I_D=34A$ $V_{DS}=10V$	27.5	—	—	S
Input Capacitance	C_{iss}	$V_{DS}=10V$ $V_{GS}=0V$ $f=1MHz$	—	7000	—	pF
Output Capacitance	C_{oss}		—	14500	—	
Reverse Transfer Capacitance	C_{rss}		—	1300	—	
Turn-On Time	$t_{d(on)}$	$V_{DD}=400V, V_{GS}=10V$ $I_D=34A, R_G=6.2\Omega$ See Fig.3 and Fig.4	—	40	—	ns
	t_r		—	107	—	
Turn-Off Time	$t_{d(off)}$		—	199	—	
	t_f		—	20	—	
Total Gate Charge	Q_G	$V_{DD}=400V, I_D=68A$ $V_{GS}=10V$ See Fig.5	—	203	—	nC
Gate-Source Charge	Q_{GS}		—	44	—	
Gate-Drain Charge	Q_{GD}		—	76	—	

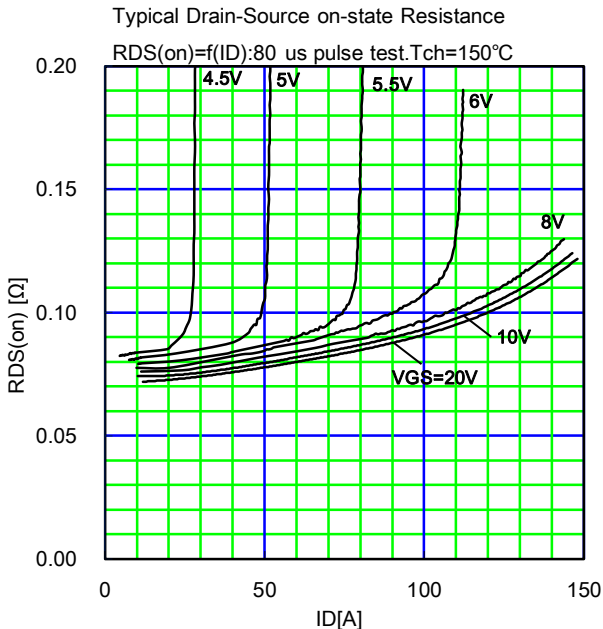
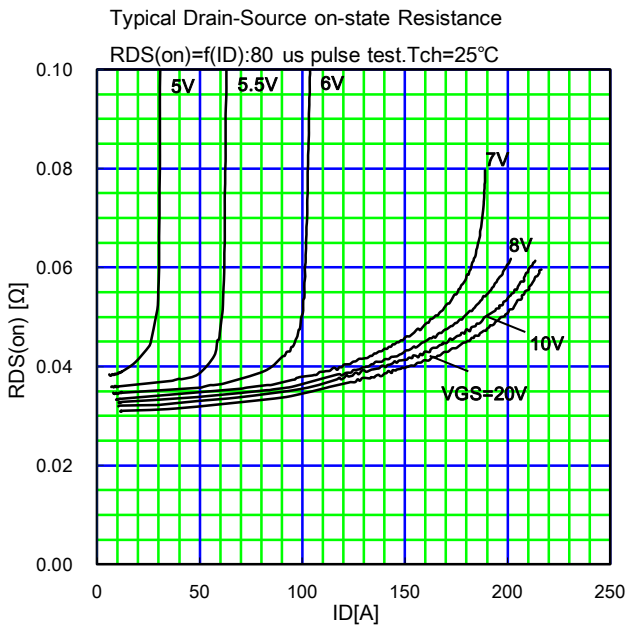
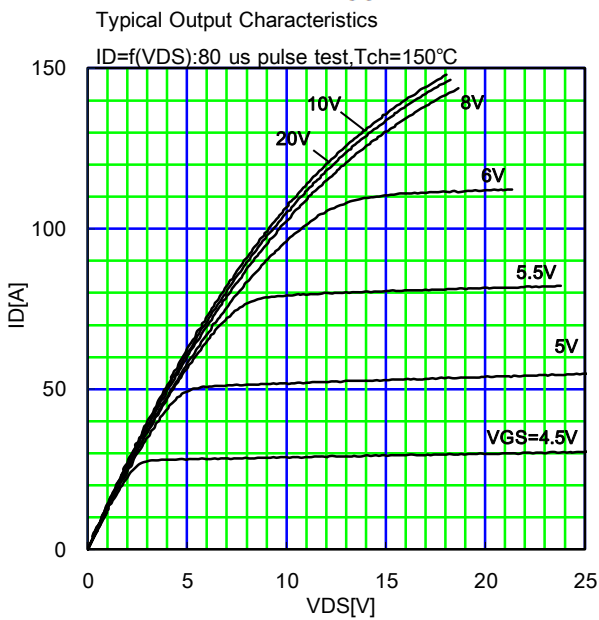
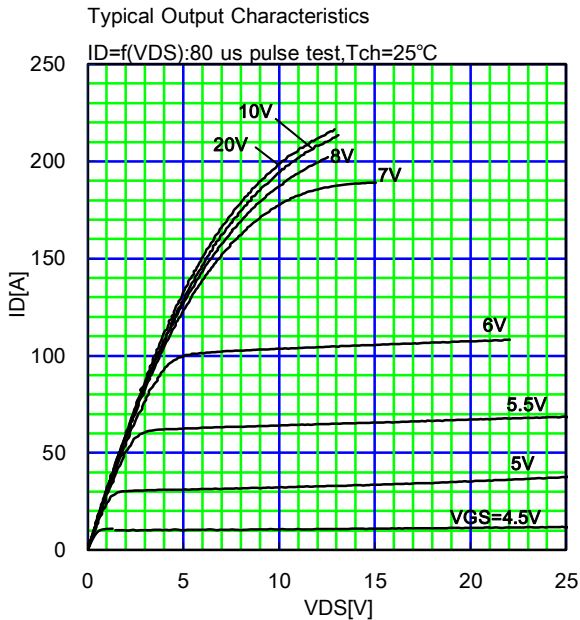
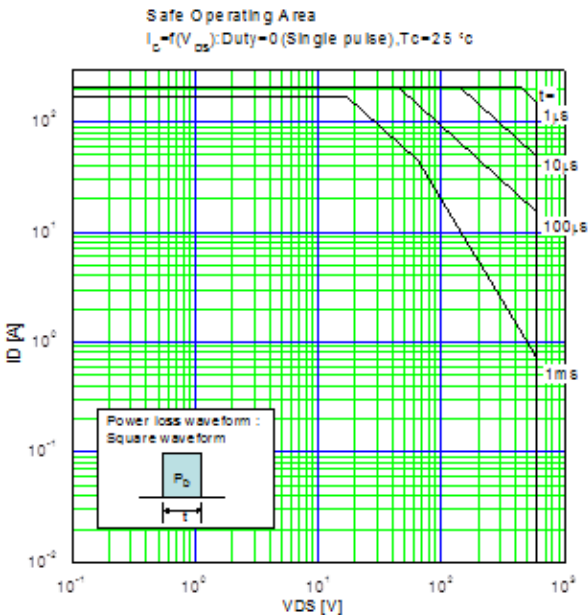
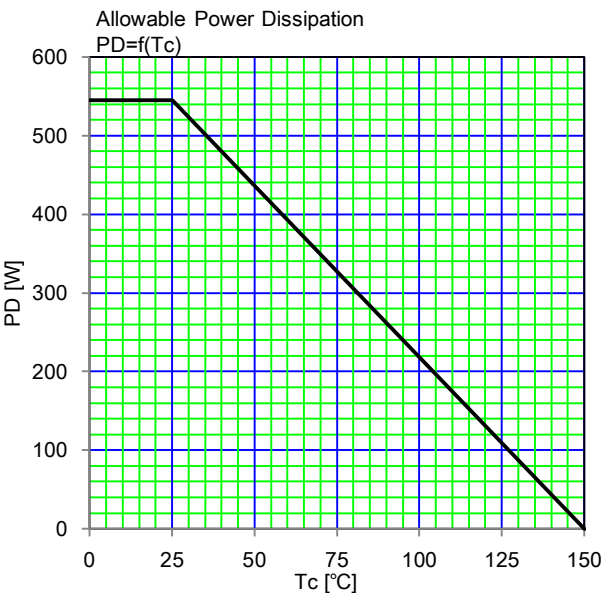
Note*6 : Co(er) is a fixed capacitance that gives the same stored energy as Coss while VDS is rising from 0 to 80% BVDSS.
 Note*7 : Co(tr) is a fixed capacitance that gives the same charging times as Coss while VDS is rising from 0 to 80% BVDSS.

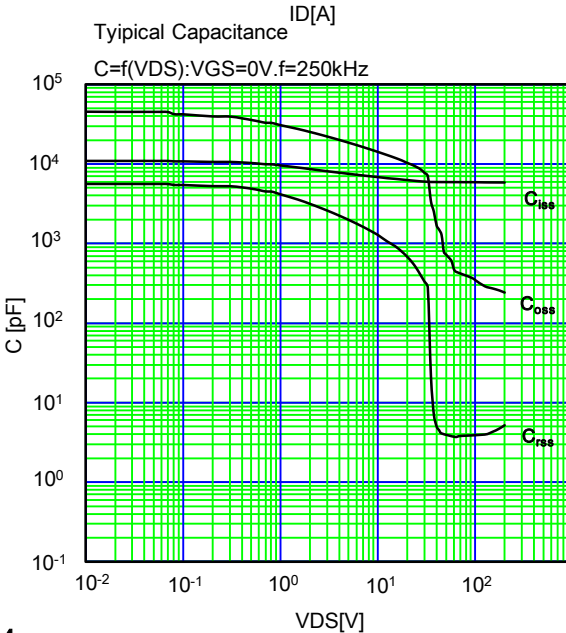
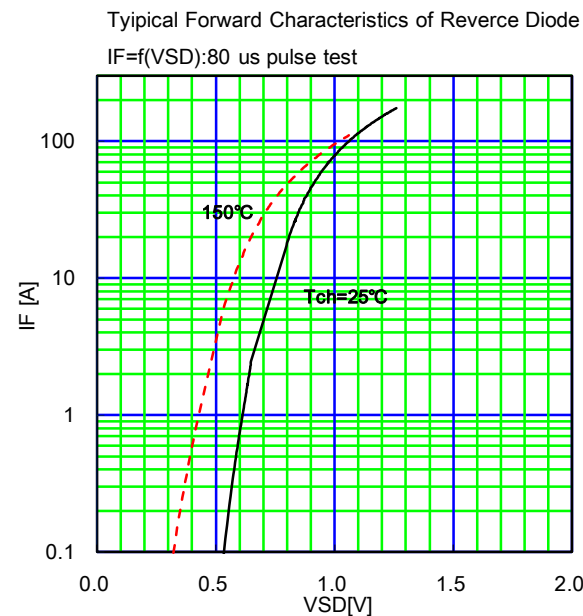
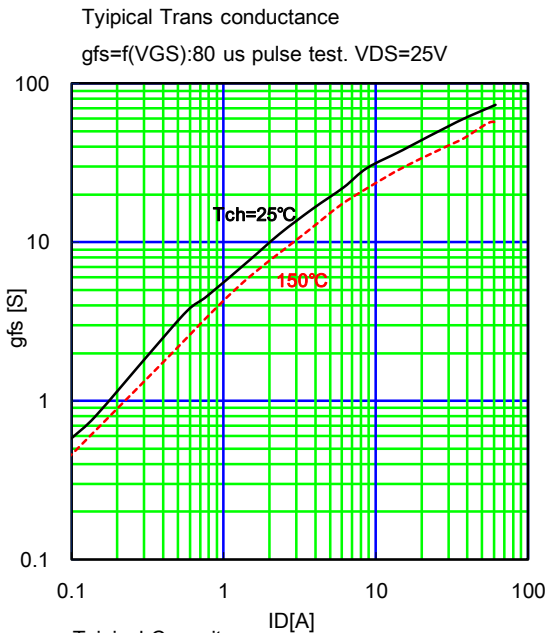
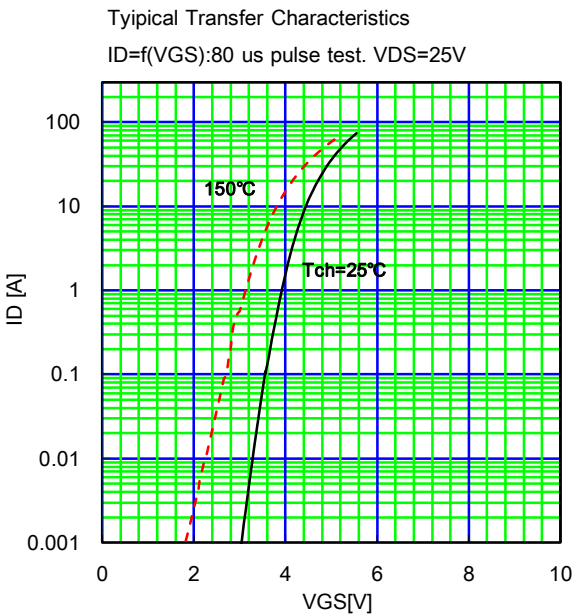
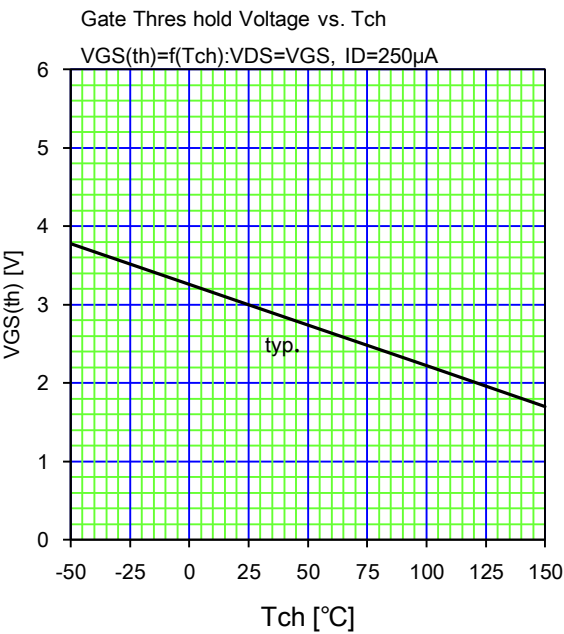
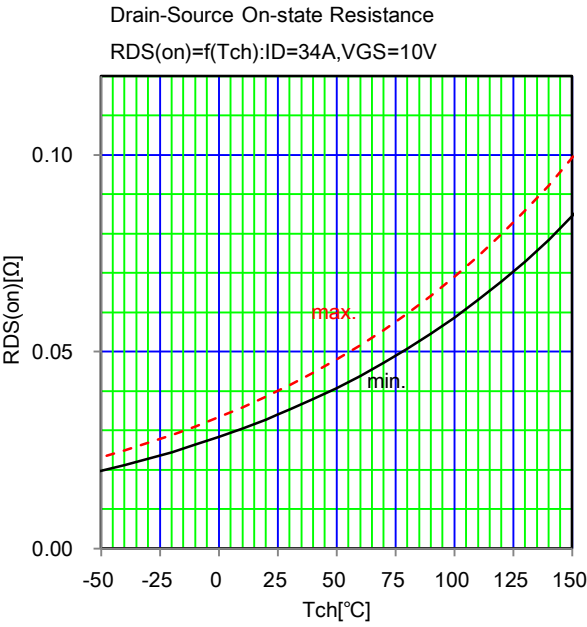
Reverse Ratings

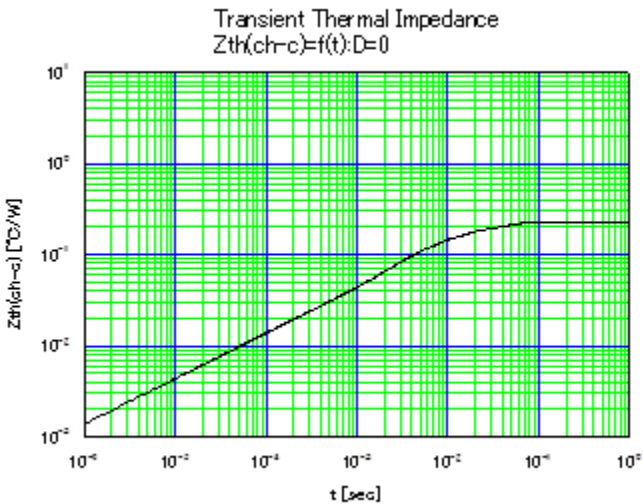
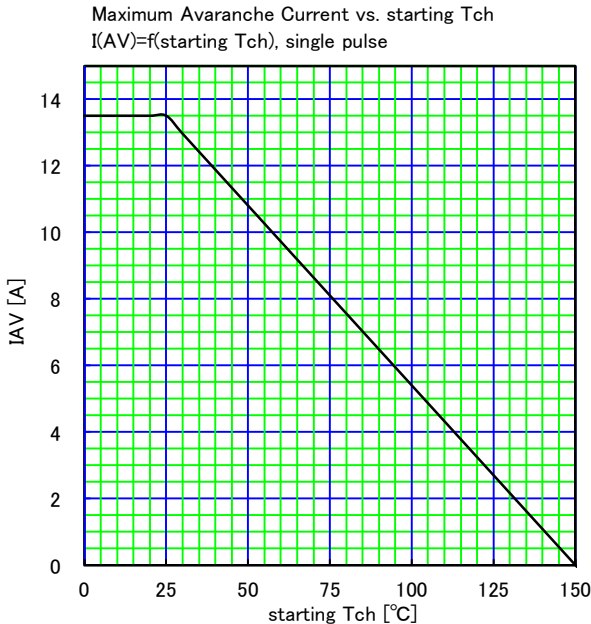
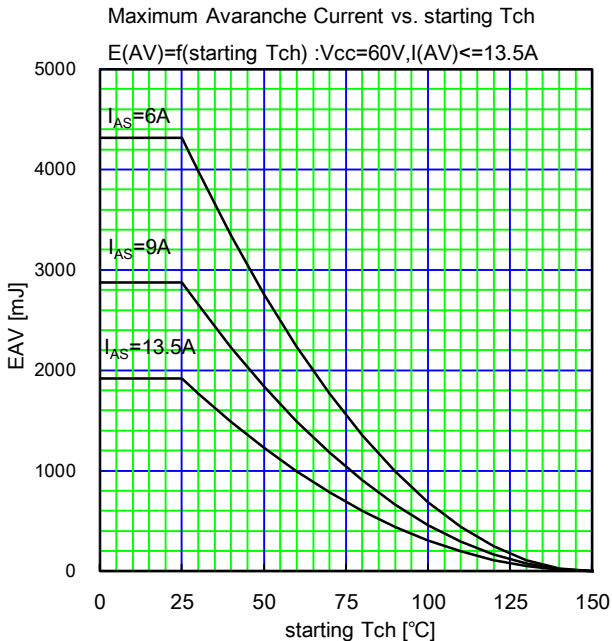
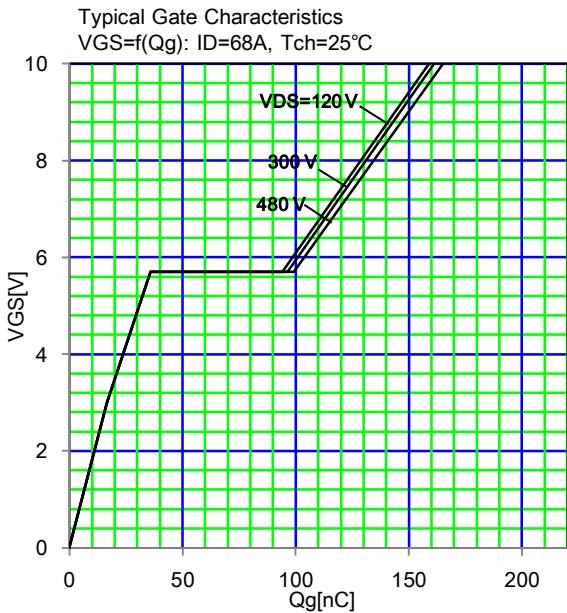
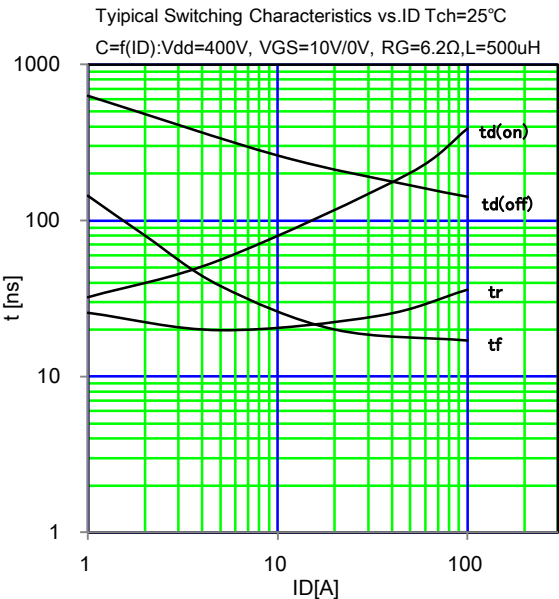
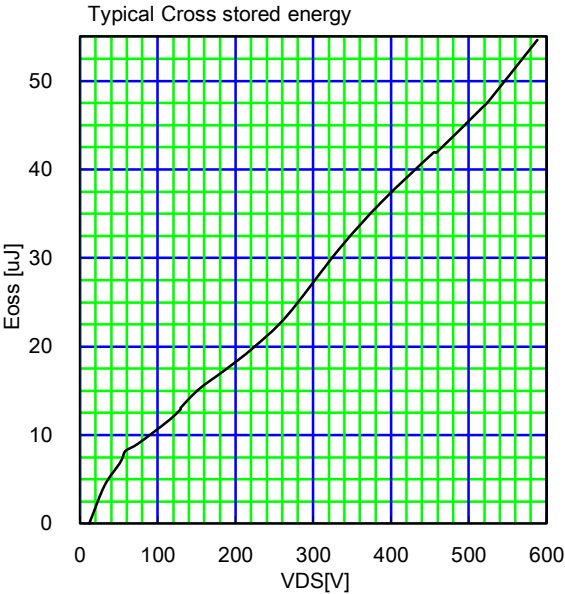
Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Avalanche Capability	I_{AV}	$L=19.3mH, T_{ch}=25^\circ C$ See Fig.1 and Fig.2	13.5	—	—	A
Diode Forward On- Voltage	V_{SD}	$I_F=68A, V_{GS}=0V$ $T_{ch}=25^\circ C$	—	1.0	1.35	V
Reverse Recovery Time	t_{rr}	$I_F=34A, V_{GS}=0V$ $V_{DD}=300V$ $-di/dt=50A/\mu s$ See Fig.6	—	600	—	ns
Reverse Recovery Charge	Q_{rr}		—	8.7	—	μC

■ Thermal Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Cannel to Case	$R_{th(ch-c)}$	—	—	0.23	$^\circ C/W$
Cannel to Ambient	$R_{th(ch-a)}$	—	—	50	$^\circ C/W$







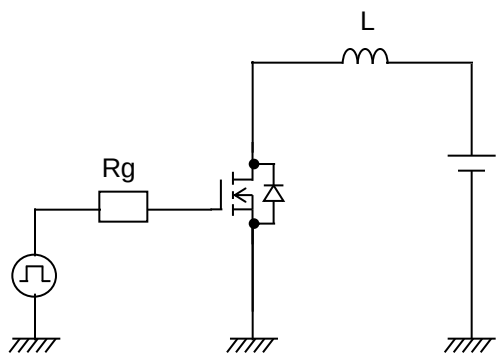


Fig.1 Avalanche Test circuit

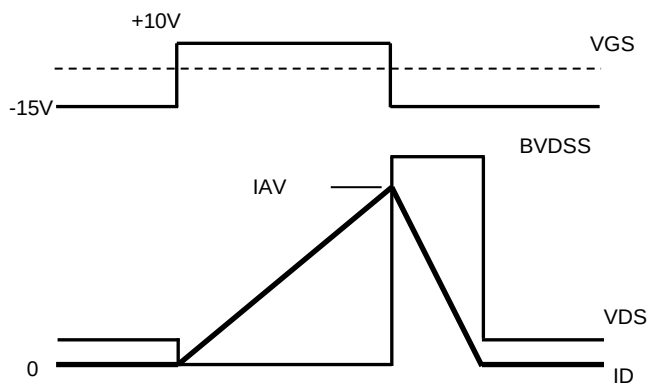


Fig.2 Operating waveforms of Avalanche Test

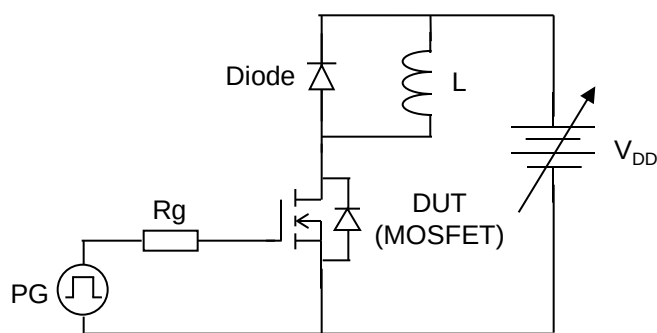


Fig.3 Switching Test circuit

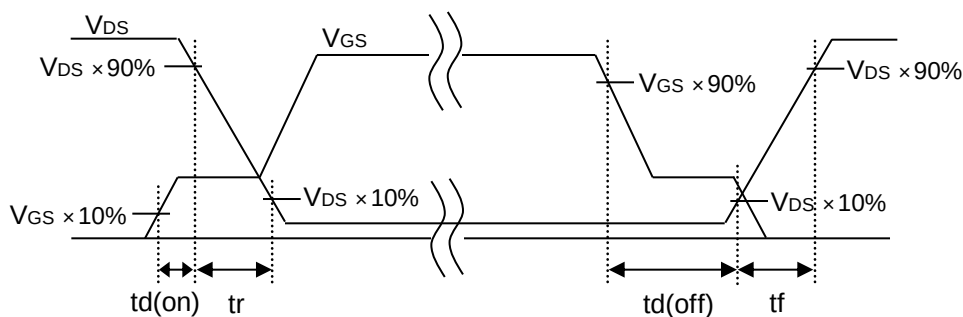


Fig.4 Operating waveform of Switching Test

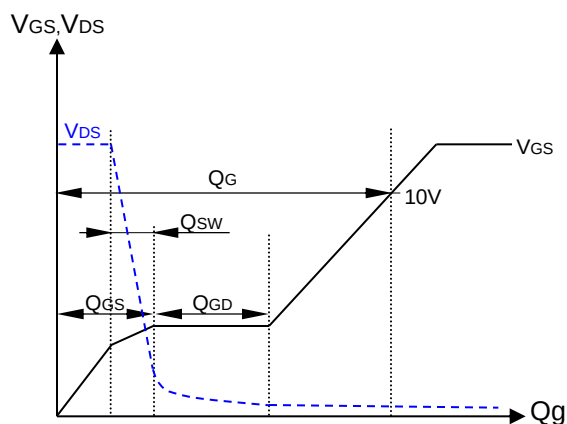


Fig.5 Operating waveform of Gate charge Test

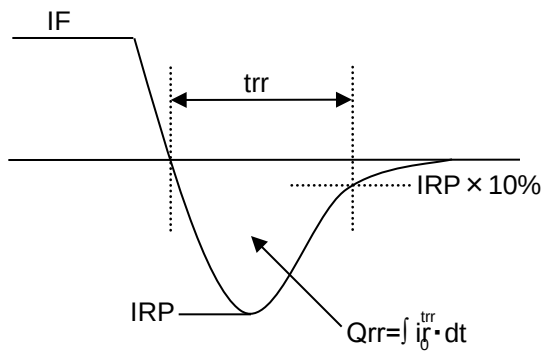


Fig.6 Operating waveform of Body diode Recovery Test

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