PDP Scan Driver IC

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1. Introduction

A shift in consumer electronics from analog to digital technology is underway, and the television industry is transitioning from CRT to flat panel display (FPD) technology. With the increasing popularity of FPDs, the market for plasma display panels (PDPs) has also grown rapidly. The FPD market is divided according to screen size: sizes of 30 inches and smaller use liquid crystal display (LCD) technology, sizes from 40 to 50 inches use PDP technology, and larger sizes use projector technology. However, competition among the different FPD technologies is intensifying and the market division according to screen size is becoming less prevalent. Within this context, PDP technology is being required to provide such performance improvements as lower power consumption and higher luminous efficient, as well as lower cost.

There are two types of PDP driver ICs, a scan driver IC that selects scan lines and an address driver (or data driver IC) that selects data lines. The characteristics of the driver ICs affect the quality of the image display, and because many IC devices are used in a single panel, these driver ICs are required to provide high performance at a low cost.

Fuji Electric develops both scan driver ICs and address driver ICs and this paper describes the technology used in Fuji Electric's FD3284F PDP scan driver IC which features high current and low on-state resistance.

2. Features of the PDP Scan Driver IC

Figure 1 shows the drive circuit of a PDP module. The scan driver IC has 64-bit output lines, and 12 of these scan driver ICs are used in an extended graphics array (XGA) panel. The basic operation of the scan driver IC is shown in Fig. 2.

(1) Scan period

During the scan period, the scan driver IC selects a scan line, and according to signal from an address driver IC, outputs a 100 V address discharge to the cell to be displayed.

(2) Sustain period

Fig.1 PDP module drive circuit

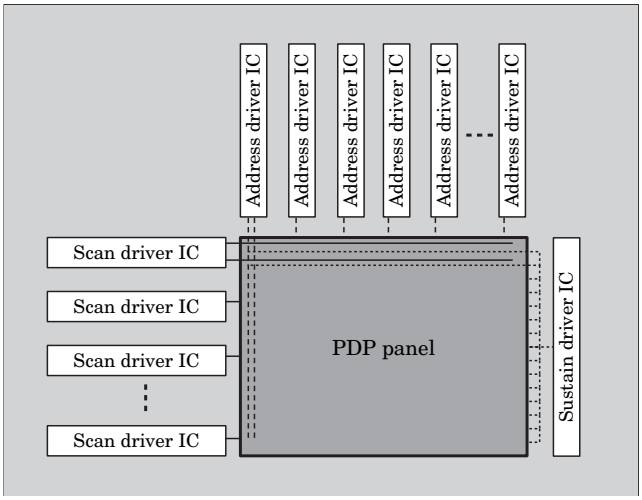
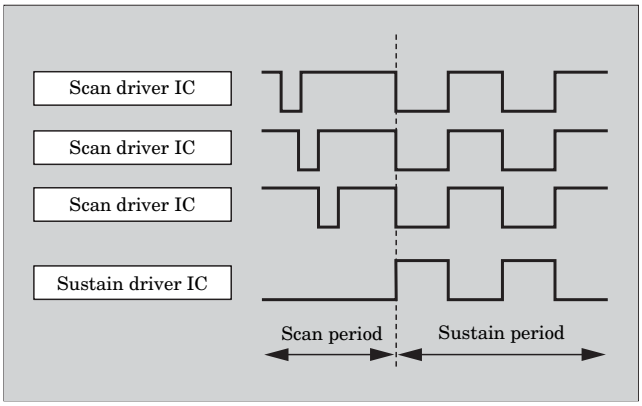


Fig.2 Scan driver IC operation



During the scan period, the scan driver IC alternates operation with the sustain driver IC, and outputs a 160 V sustain discharge to the cell that received an address discharge during the scan period.

This sustain discharge operation is repeated to implement a grayscale display.

The scan driver IC must be able to supply a large current at a high voltage during address and sustain discharges.

3. PDP Scan Driver IC Technology

3.1 Process and device technology

Fuji Electric has been using a silicon-on-insulator (SOI) method of dielectric isolation technology. Although the SOI process has the disadvantage of an expensive wafer cost, it features small device isolated areas and latch-up free operation, and therefore SOI process technology is well suited for scan driver ICs that require high voltage and high current.

The output device uses insulated gate bipolar transistors (IGBTs) connected in a totem pole configuration. The output circuit of a scan driver IC occupies 60 % of the IC area and therefore the output device size has a large impact on cost. The IGBT, which is able to output a large current from a small area, is optimally suited as an output device for a scan driver IC. As shown in Fig. 3 and Table 1, the newly developed third-generation SOI-IGBT device is smaller and achieves greater drive capability than a conventional IGBT.

Fig.3 IGBT device comparison

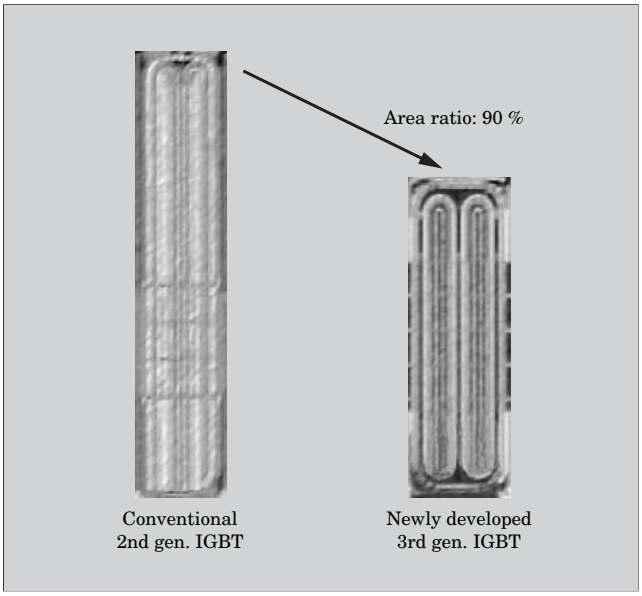


Table 1 FD3284F characteristics

Parameter	Conventional IGBT	FD3284F
Absolute maximum voltage (logic circuit)	7.0 V	7.0 V
Absolute maximum voltage (output circuit)	165 V	165 V
Operating voltage (logic)	5.0 V	5.0 V
Operating voltage (output)	30 to 130 V	30 to 130 V
High output source or sink current	– 200 mA/ +1,000 mA	– 200 mA/ +1,500 mA
High output diode current	– 1,000 mA/ +1,000 mA	– 1,200 mA/ +1,500 mA

3.2 Circuit technology

Figure 4 shows the output stage circuit of a scan driver IC. N-channel IGBTs are connected in a totem pole output configuration. The high-side IGBT (N2 in the figure) is controlled by a level shifter, and because the IGBT gate is driven at 5.5 V, a 5.5 V zener diode is inserted between the gate and source for protection.

The operation of the output stage circuit is summarized below.

(1) Scan period

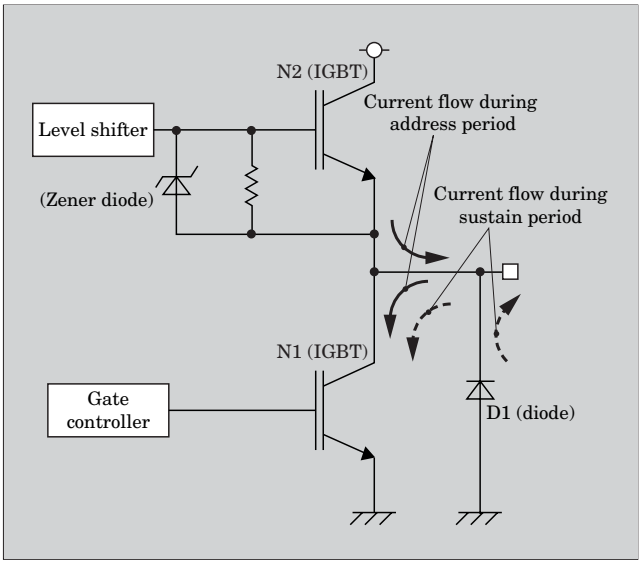
IGBTs N1 and N2 operate to output selected waveforms and unselected waveforms. During an address discharge, the N1 IGBT supplies a large current.

(2) Sustain period

The N1 IGBT and the D1 diode operate to provide a sustain discharge current supplied from both the N1 and D1 devices.

As the size of the display panel increases, a larger discharge current is required for address discharge and sustain discharge, and the on-state resistance of the device becomes an issue. If the device has a large on-state resistance, it will emit a large quantity of heat and the resulting temperature rise will lead to degradation of the device characteristics and a corresponding degradation of display quality. Comparing the on-state resistance of the N1 IGBT and the D1 diode reveals that when the on-state resistance of the D1 diode is 1.4 V/400 mA, the N1 IGBT will have a large on-state resistance of 6.0 V/400 mA. Because the N1 IGBT operates during both the scan period and the sustain period, its on-state resistance has a dominant effect on the amount of heat generated. Accordingly, the key to the development of a successful scan driver IC is to provide an N1 IGBT device with high drive capability.

Fig.4 Output circuit



3.3 IGBT gate control technology

If the current density of an IGBT device is increased so that large current can be obtained in a small area, the safe operating area (SOA) will become smaller and if an unusual discharge occurs during address or sustain discharge operations and causes an overload or short-circuit state, the device will exceed its SOA and be damaged.

Similarly, if waste metal adheres between the output terminals and the device unexpectedly enters an overload state, the device will exceed its SOA and become damaged.

On the other hand, in an attempt to expand the SOA, if the current density is decreased, the device area will increase due to the tradeoff relation that exists between current density and cost will also increase. In order to resolve this tradeoff between current density and SOA, Fuji Electric has developed technology for controlling the gate voltage of the N1 IGBT in accordance with the output timing. This operation is shown in Fig. 5.

During the scan period, in the case of a 5 V supply voltage VDL, so as to supply sufficient current for the output to drop, a voltage of approximately 4.5 V is applied to the gate of the N1 IGBT, causing the output voltage to drop from 100 V to 0 V and a scan line to be selected.

Fig.5 Address discharge operation

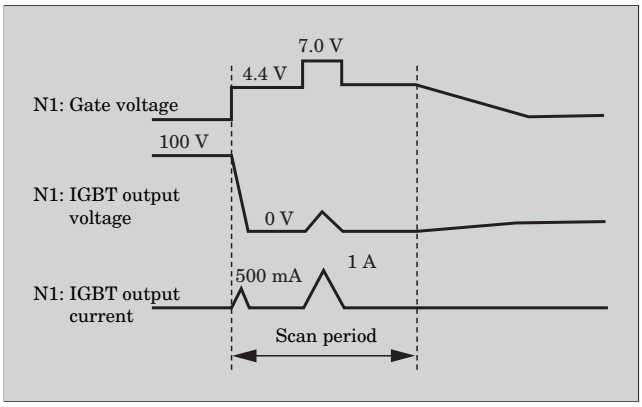
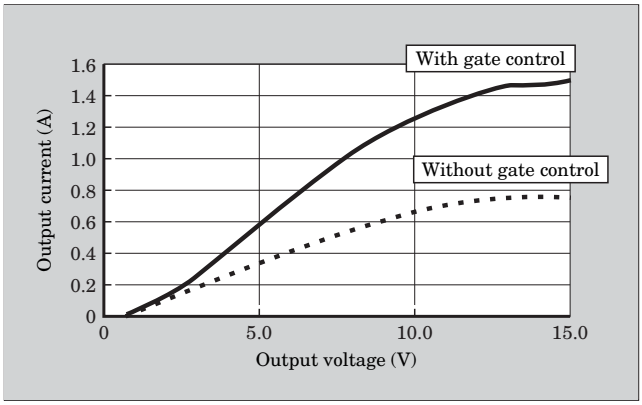


Fig.6 FD3284F's low-level R_{ON} (N1)



The address discharge begins, and when a larger current is required, the gate voltage of the N1 IGBT is increased to 7 V to boost the current drive capability of the N1 IGBT.

After the address discharge, the gate voltage is again lowered to 4.5 V to reduce the drive capability. Then, 1.5 μs after the scan period, the voltage of the N1 IGBT gate is gradually decreased until the IGBT turns off. This control prevents the N1 IGBT from operating outside its normal operating period, thereby prevent possible damage due to an unexpected overload condition caused by an unusual discharge, short circuit or the like.

Figure 6 shows the characteristics of an N1 IGBT that incorporates this gate control technology. Even if the device area is 10 % smaller than a conventional IGBT, implementation of this gate control enables twice the output current capacity compared to the case without gate control.

4. Application to a PDP Scan Driver IC

Fuji Electric's FD3284F PDP scan driver IC, which uses this newly developed third-generation SOI-IGBT device and gate control circuit technology, is described below.

4.1 Features

(1) 64-bit bidirectional shift register (15 MHz, with CLR function)
(2) Absolute maximum voltage: 165 V (output circuit), 7 V (logic circuit)
(3) Output operating voltage: 32 to 130 V
(4) Logic operating voltage: 5 V
(5) High output current: −0.2 A/+1.5 A (source/sink)
(6) High output diode current: −1.2 A/+1.5 A (source/

Fig.7 FD3284F block diagram

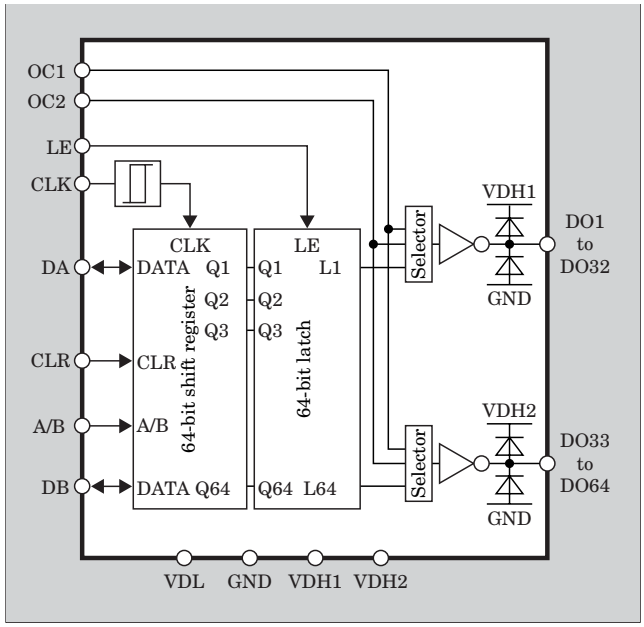
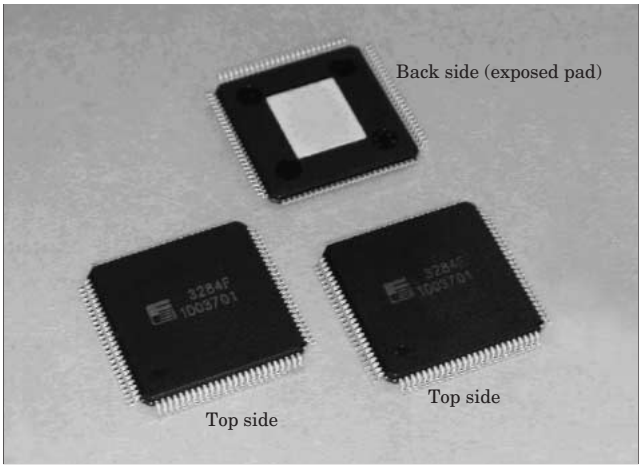


Fig.8 FD3284F package



sink)

(7) Package: TQFP 100-pin (exposed pad)

4.2 Circuit configuration

Figure 7 shows a block diagram of the circuit configuration. The circuit is configured from a 64-bit bidirectional shift register, a 64-bit latch, data selector circuits, and a totem pole output drive circuit.

4.3 Characteristics compared to those of a conventional IC

Table 1 lists the main differences in characteristics between the conventional scan driver IC and the FD3284F. The FD3284F, which has been designed to be capable of driving large PDP panels, features dramatically improved driver output current and diode output current capabilities. Figure 8 shows external views of the FD3284F which uses a heat-radiating exposed pad TQFP 100-pin package.

5. Conclusion

This paper has described characteristics of PDP scan driver IC technology and of Fuji Electric's FD3284F PDP scan driver IC. Competition among FPD technologies will intensify in the future and Fuji Electric plans to continue to advance device, circuit and process technologies in order to satisfy market requirements for higher performance and lower cost PDPs.

References

(1) Kobayashi, H. et al. IDW'04. PDP3-3.