6MBP50XTA065-50

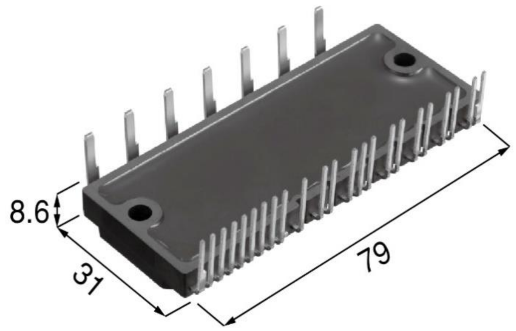
IGBT Modules

IGBT Module(X series)
650V / 50A / IPM

■ Features

Low-side IGBTs are separate emitter type
Short circuit protection
Temperature sensor output function
Under voltage protection
Fault signal output function
Input interface:TTL(3.3V/5V)Active high logic

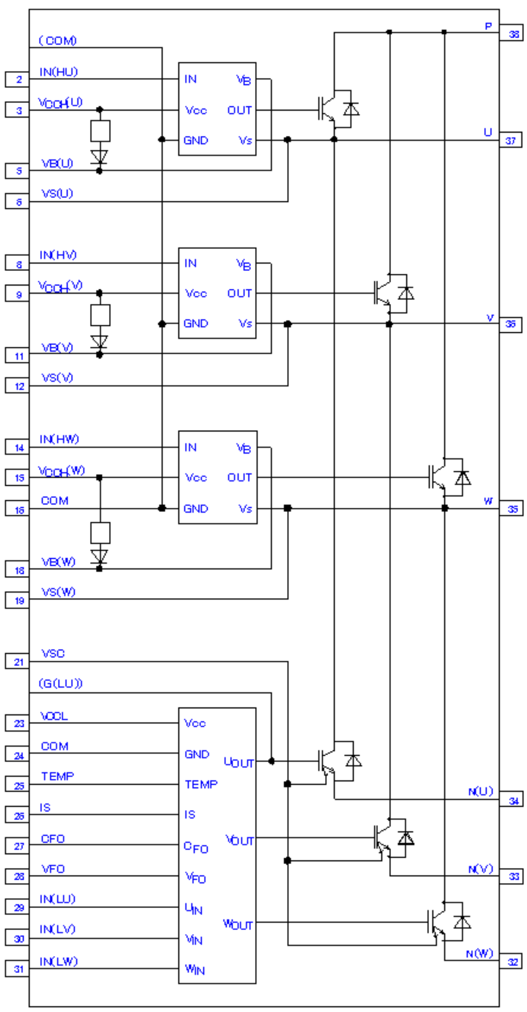
■ Typical appearance



■Applications

AC 100~240V three phase inverter drive for small power AC motor drives(such as compressor motor drive for air conditioner,compressor motor drive for heat pump applications,ventilator mortor drive)

■ Terminal assign and Internal circuit



Pin No.	Pin Name	Pin Description
2	IN(HU)	Signal input for high side U-phase
3	VCCH(U)	Control supply for high side U-phase
5	VB(U)	High-side bias voltage for U-phase IGBT driving
6	VS(U)	High-side U-phase drive supply GND
8	IN(HV)	Signal input for high side V-phase
9	VCCH(V)	Control supply for high side V-phase
11	VB(V)	High-side bias voltage for V-phase IGBT driving
12	VS(V)	High-side V-phase drive supply GND
14	IN(HW)	Signal input for high side W-phase
15	VCCH(W)	Control supply for high side W-phase
16	COM	Common supply ground
18	VB(W)	High-side bias voltage for W-phase IGBT driving
19	VS(W)	High-side W-phase drive supply GND
21	VSC	Sense current detecting for low side
23	VCCL	Low-side control supply
24	COM	Common supply ground
25	TEMP	Temperature sensor output
26	IS	Over current sensing voltage input
27	CFO	Capacitor for fault output width selection
28	VFO	Fault output
29	IN(LU)	Signal input for low side U-phase
30	IN(LV)	Signal input for low side V-phase
31	IN(LW)	Signal input for low side W-phase
32	N(W)	Negative bus voltage input for W-phase
33	N(V)	Negative bus voltage input for V-phase
34	N(U)	Negative bus voltage input for U-phase
35	W	Motor W-phase output
36	V	Motor V-phase output
37	U	Motor U-phase output
38	P	Positive bus voltage input

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■ **Absolute Maximum Ratings(T_{vj}=25°C,T_C=25°C,V_{CC}=15V,$V_{B(*)}$=15V unless otherwise specified)**

Items		Symbol	Characteristics	Unit	Remarks
Inverter block	DC Bus Voltage	$V_{DC (terminal)}$	450	V	Note *1, See Fig.2-2
	Bus Voltage (Surge)	$V_{DC(Surge,terminal)}$	500	V	Note *1, See Fig.2-2
	Collector-Emitter Voltage	$V_{CE(chip)}$	650	V	Note *1, See Fig.2-2
	Collector Current	I_C	50	A	Note *2
	Peak Collector Current	I_{CP}	100	A	V_{CC}≧15V, $V_{B(*)}$≧15V Note *2, *3, *4
	Forward current	I_F	50	A	Note *2
	Peak Forward current	I_{FP}	100	A	Note *2
	Collector Power Dissipation	P_{D_IGBT}	132	W	per single IGBT T_c=25°C
	FWD power Dissipation	P_{D_FWD}	89	W	per single FWD T_c=25°C
	Self operation "DC Bus voltage" of circuit protection between upper-arm and lower-arm	$V_{DC(sc)}$	400	V	V_{CC}=$V_{B(*)}$=13.5~16.5V T_{vj}=125°C, non-repetitive less than 3us See Fig.2-2
	Virtual Junction Temperature	T_{vj}	175	°C	Note *8
	Operating Virtual Junction Temperature	T_{vjop}	-40 ~ +150	°C	
Control circuit block	High-side Supply Voltage	$V_{CCH(U)}$ $V_{CCH(V)}$ $V_{CCH(W)}$	-0.5 ~ 20	V	Applied between VCCH(U)-COM, VCCH(V)-COM, VCCH(W)-COM
	Low-side Supply Voltage	V_{CCL}	-0.5 ~ 20	V	Applied between VCCL-COM
	High-side Bias Absolute Voltage	$V_{VB(U)-COM}$ $V_{VB(V)-COM}$ $V_{VB(W)-COM}$	-0.5 ~ 670	V	Applied between VB(U)-COM, VB(V)-COM, VB(W)-COM
	High-side Bias Voltage for IGBT gate driving	$V_{B(U)}$ $V_{B(V)}$ $V_{B(W)}$	-0.5 ~ 20	V	Note *4
	High-side Bias offset Voltage	V_U V_V V_W	-5 ~ 650	V	Applied between U-COM, V-COM, W-COM Note *5
	Input Signal Voltage	V_{IN}	-0.5 ~ V_{CCH}+0.5 -0.5 ~ V_{CCL}+0.5	V	Note *6
	Input Signal Current	I_{IN}	3	mA	sink current
	Fault Signal Voltage	V_{FO}	-0.5 ~ V_{CCL}+0.5	V	Applied between VFO-COM
	Fault Signal Current	I_{FO}	1	mA	sink current
	CFO Signal Voltage	V_{CFO}	-0.5 ~ 5.0	V	Between CFO-COM Note *9
	CFO Signal Current	I_{CFO}	-0.05 / 3	mA	source / sink current
	Over Current sensing Input Voltage	V_{IS}	-0.5 ~ V_{CCL}+0.5	V	Applied between IS-COM
	TEMP Signal Voltage	V_{TEMP}	-0.5 ~ 5.0	V	Between TEMP-COM Note *9
	TEMP Signal Current	I_{TEMP}	-0.05 / 3	mA	source / sink current
	VSC Signal Voltage	V_{VSC}	-0.5 ~ V_{CCL}+0.5	V	Between VSC-COM Note *9
	VSC Signal Current	I_{VSC}	-20	mA	Source current
	Virtual Junction Temperature	T_{vj}	150	°C	
Operating Case Temperature		T_c	-40 ~ +125	°C	See Fig.1-2
Storage Temperature		T_{stg}	-40 ~ +125	°C	
Isolation Voltage		V_{isol}	AC 2500	Vrms	Sine wave,60Hz t=1min , Note *7

Note

*1 : V_{DC} is applied between P-N(U),P-N(V),P-N(W).
V_{CE} is Collector-Emitter voltage of internal IGBT chip.

*2 : Pulse width and duty were limited by T_{vj}max.

*3 : V_{CC} is applied between VCCH-COM,VCCL-COM.

*4 : $V_{B(*)}$ is applied between VB(U)-VS(U),VB(V)-VS(V), VB(W)-VS(W).

*5 : Over 13.0V applied between VB(U)-VS(U),VB(V)-VS(V), VB(W)-VS(W). This IPM module might make incorrect response if the high-side bias offset voltage is less than -5V.

*6 : Applied between IN(HU)-COM,IN(HV)-COM,IN(HW)-COM,IN(LU)-COM,IN(LV)-COM,IN(LW)-COM.

*7 : Applied between shorted all terminal and IMS (Insulated Metal Substrate).

*8 : The maximum temperature during continuous operation is T_{vj}=150°C.
The operating conditions have to be decided so that the temperature is below T_{vj}=150°C.
Continuous operation at over T_{vj}=150°C may result in degradation of product lifetime such as power cycling capability.

*9 : CFO, TEMP, VSC are output terminals. Never applied power source.

Electrical Characteristics

Inverter block

(T_{vj}=25°C, T_c=25°C, V_{CC}=15V, $V_{B(*)}$=15V, V_{IN}=0V, V_{IS}=0V, $V_{N(*)-COM}$=0V unless otherwise specified)

Description	Symbol	Conditions		min.	typ.	max.	Unit
Zero gate Voltage Collector current	I_{CE}	V_{CE} = 650V	T_{vj}=25°C	-	-	1	mA
			T_{vj}=125°C	-	-	10	mA
Collector-Emitter saturation Voltage	$V_{CE(sat)}$ (terminal)	I_C=50A, V_{IN}=5V, Note *4	T_{vj}=25°C	-	1.30	1.65	V
			T_{vj}=125°C	-	1.45	1.80	
Forward voltage	V_F	I_F=50A	T_{vj}=25°C	-	1.55	2.05	V
			T_{vj}=125°C	-	1.60	-	
Turn-on time	t_{on}	V_{DC} = 300V, I_C = 50A, T_{vj} = 125°C, V_{IN}=0V <-> 5V, See Fig.2-1, Note *4		1.20	1.70	2.50	μs
Turn-on delay time	$t_{d(on)}$			-	1.60	-	
Turn-on rise time	t_r			-	0.15	-	
V_{CE}-I_C Cross time of turn-on	$t_{c(on)}$			-	0.35	0.70	
Turn-off time	t_{off}			-	1.85	2.50	
Turn-off delay time	$t_{d(off)}$			-	1.75	-	
Turn-off fall time	t_f			-	0.15	-	
V_{CE}-I_C Cross time of turn-off	$t_{c(off)}$			-	0.35	0.70	
Reverse Recovery time	t_{rr}			-	0.25	-	

Control circuit block

(T_{vj}=25°C, T_c=25°C, V_{CC}=15V, $V_{B(*)}$=15V, V_{IN}=0V, V_{IS}=0V, $V_{N(*)-COM}$=0V unless otherwise specified)

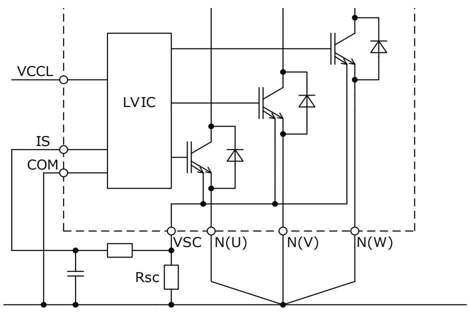
Description	Symbol	Conditions		min.	typ.	max.	Unit
Circuit current of Low-side	I_{CCL}	V_{CCL}=15V	V_{IN}=5V	-	0.7	1.1	mA
			V_{IN}=0V	-	0.7	1.1	
Circuit current of High-side (per one unit)	I_{CCH}	$V_{CCH(U)}$=15V, $V_{CCH(V)}$=15V, $V_{CCH(W)}$=15V	V_{IN}=5V	-	1.2	1.9	mA
			V_{IN}=0V	-	1.2	1.9	
Circuit current of Bootstrap circuit (per one unit)	I_{CCHB}	$V_{B(U)}$=15V, $V_{B(V)}$=15V, $V_{B(W)}$=15V	V_{IN}=5V	-	-	0.20	mA
			V_{IN}=0V	-	-	0.20	
Input Signal threshold voltage	$V_{th(on)}$	Note *10 $PW \geq$ 1.5µs		1.6	2.1	2.6	V
	$V_{th(off)}$			0.8	1.3	1.8	V
Input Signal threshold hysteresis voltage	$V_{th(hys)}$			0.35	0.8	-	V
Operational input pulse width of turn-on	$t_{IN(on)}$	V_{IN}=0V to 5V rise up, Note *6,Note *10		1.5	-	-	µs
Operational input pulse width of turn-off	$t_{IN(off)}$	V_{IN}=5V to 0V fall down, Note *6,Note *10		0.8	-	-	µs
Input current	I_{IN}	V_{IN}=5V Note *6		0.7	1.0	1.5	mA
Input pull-down resistance	R_{IN}	Note *6		3.3	5.0	7.2	kΩ
Fault Output Voltage	$V_{FO(H)}$	V_{IS}=0V,V_{FO} terminal pull up to 5V by 10kΩ		4.9	-	-	V
	$V_{FO(L)}$	V_{IS}=1V,I_{FO}=1mA		-	-	0.95	V
Fault Output pulse width	t_{FO}	C_{FO}=22nF Note *12,See Fig2-3,2-4		1.6	2.4	-	ms
Over Current Protection Voltage Level	$V_{IS(ref)}$	V_{CC}=15V Note *3, *11, *12 See Fig.2-3		0.455	0.48	0.505	V
Over Current Protection Delay time	$t_{d\ (IS)}$			0.6	1.25	1.9	µs
Over current trip level	I_{oc}	R_{sc} =40.2Ω(±1%), No shunt resistor connecting to N(U),N(V),N(W) See Fig.1-1		85	-	-	A
Output Voltage of temperature sensor	$V_{(temp)}$	Note *13	$T_{vj(LVIC)}$=90°C	2.63	2.77	2.91	V
			$T_{vj(LVIC)}$=25°C	0.88	1.13	1.39	V
Pull down Resistance of TEMP terminal	$R_{(temp)}$	Note *14		5	-	-	kΩ

Control circuit block (continued)

(T_{vj}=25°C, T_c=25°C, V_{CC}=15V, $V_{B(*)}$=15V, V_{IN}=0V, V_{IS}=0V, $V_{N(*)-COM}$ =0V unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit
V_{CC} Under Voltage Trip Level of Low-side	$V_{CCL(OFF)}$		10.3	-	12.5	V
V_{CC} Under Voltage Reset Level of Low-side	$V_{CCL(ON)}$	T_{vj}<150°C See Fig.2-4 Note *12	10.8	-	13.0	V
V_{CC} Under Voltage hysteresis	$V_{CCL(hys)}$		-	0.5	-	V
V_{CC} Under Voltage Trip Level of High-side	$V_{CCH(OFF)}$		8.3	-	10.3	V
V_{CC} Under Voltage Reset Level of High-side	$V_{CCH(ON)}$	T_{vj}<150°C See Fig.2-5	8.8	-	10.8	V
V_{CC} Under Voltage hysteresis	$V_{CCH(hys)}$		-	0.5	-	V
V_B Under Voltage Trip Level	$V_{B(OFF)}$		10.0	-	12.0	V
V_B Under Voltage Reset Level	$V_{B(ON)}$	T_{vj}<150°C See Fig.2-6	10.5	-	12.5	V
V_B Under Voltage hysteresis	$V_{B(hys)}$		-	0.5	-	V
Forward voltage of Bootstrap diode	$V_{F(BSD)}$	T_{vj}=25°C $I_{F(BSD)}$=10mA	0.5	0.9	1.3	V
Built-in limiting resistance	$R_{(BSD)}$	T_{vj}=25°C	16	20	24	Ω

Fig.1-1: Over current protection circuit



Note

*10 : This IPM module might make incorrect response if the input signal pulse width is less than $t_{IN(on)}$ and $t_{IN(off)}$.

*11 : "Over current protection" is functioning only for the low-side arms.

*12 : Fault signal is asserted corresponding to an "Over-current protection" or an "Under-voltage protection" at V_{CCL}.
Under the condition of "Over-current protection" or "Under-voltage protection", the fault signal is asserted continuously while these conditions are continuing.
However, the minimum fault output pulse width is t_{FO}(min.) even if very short failure condition (which is less than t_{FO}(min.)) is triggered. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO}. (C_{FO}(typ.) = t_{FO} x (9.1 x 10^{-6}) [F])

*13 : Fig.1-2 shows the measurement position of temperature.

*14 : It is recommended to insert pull down resister for getting linear output characteristics at low temperature below room temperature.

Thermal Characteristics (T_c=25°C)

Description	Symbol	min.	typ.	max.	Unit
Junction to Case Thermal Resistance (per single IGBT) Note *15	$R_{th(j-c)\_IGBT}$	-	-	0.95	°C/W
Junction to Case Thermal Resistance (per single Diode) Note *15	$R_{th(j-c)\_FWD}$	-	-	1.40	°C/W

Note
*15 : Thermal compound with good thermal conductivity should be applied evenly with about +100µm~+200µm on the contacting surface of this device and heat-sink.

Mechanical Characteristics (T_c=25°C)

Description	Symbol	Conditions	min.	typ.	max.	Unit
Mounting torque of screws	M_S	Mounting screw : M4	0.98	1.18	1.47	Nm
Heat-sink side flatness	-	The AL-IMS part : See (A1),(A2) of Fig.1-3.	-50	-	100	µm
Weight	-	-	-	37	-	g
Resistance to soldering heat	-	Solder temp : 260±5°C Immersion time : 10±1sec Solder alloy : Sn-Ag-Cu type	-	-	1	time

Fig.1-2 :
The measurement position of temperature

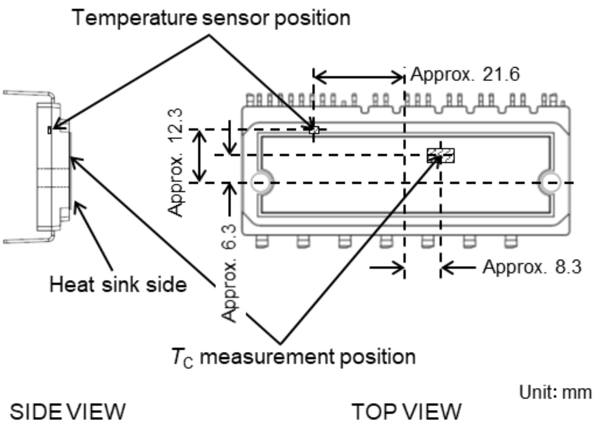
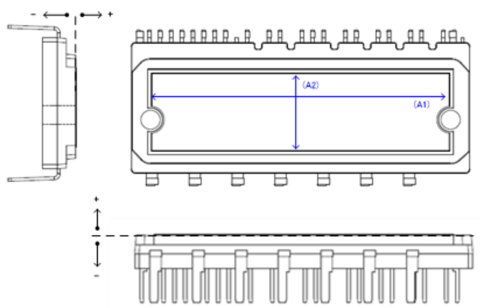


Fig.1-3 :
The measurement position of heat sink flatness



Note
*16 : Fig.1-3 shows the measurement position of heat sink flatness.

Recommended Operation Conditions (Note*20)

Description	Symbol	min.	typ.	max.	Unit
DC Bus Voltage	V_{DC}	0	300	400	V
High-side Bias Voltage for IGBT gate driving	$V_{B(*)}$	13.0	15.0	18.5	V
High-side Supply Voltage	$V_{CCH(*)}$	13.5	15.0	16.5	V
Low-side Supply Voltage	V_{CCL}	13.5	15.0	16.5	V
Control Supply variation (Under switching Condition)	ΔV_B	-1	-	1	V/µs
	ΔV_{CC}	-1	-	1	
Input signal voltage	V_{IN}	0	-	5	V
Voltage for current sensing	V_{ISC}	0	-	5	V
Potential difference between COM and N (including surge)	V_{COM_N}	-5	-	5	V
Dead time for preventing arm-short ($T_c \leq 125°C$)	t_{DEAD}	2.2	-	-	µs
Output current (Note *17)	I_O	-	-	50	A rms
Minimum input pulse width (Note *18, *19)	$PW_{IN(on)}$	1.5	-	-	µs
	$PW_{IN(off)}$	0.8	-	-	µs
PWM Input frequency	f_{PWM}	-	-	20	kHz
Operating Virtual Junction Temperature	T_{vjop}	-30	-	150	°C
Capacitance value between CFO and COM (Note*21)	C_{FO}	1	22	-	nF

Note

*17 : V_{DC}=300V, $V_{CCH(*)}=V_{CCL}=V_{B(*)}$=15V, PF=0.8, Sinusoidal PWM, 3phase modulation, $T_{vj} \leq 150°C$, $T_c \leq 100°C$, f_{PWM}=5kHz, f_O=200Hz, Ks=0.9

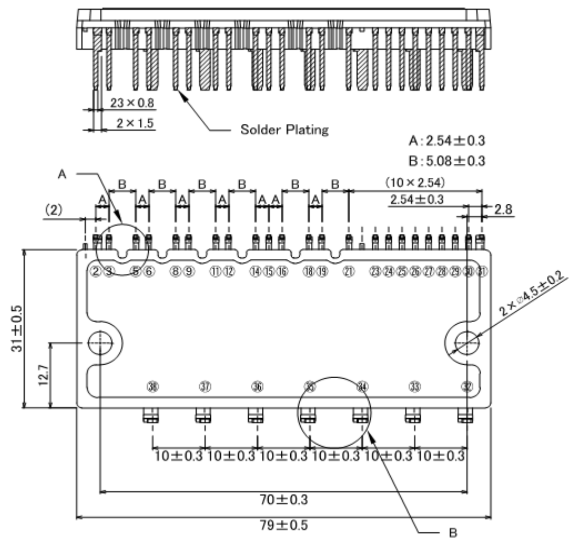
*18 : In the pulse width of 1.5us, the loss of IGBT increases for the saturation operation. To reduce the loss of IGBT, please enlarge the pulse width more than the switching time of IGBT.

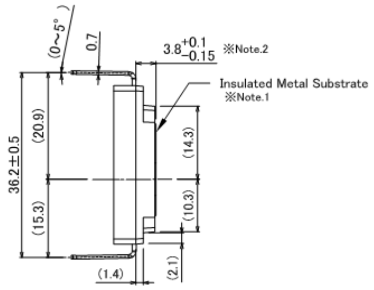
*19 : This IPM module might response according to input signal pulse even when the input signal pulse width is less than $PW_{IN(on)}$ and $PW_{IN(off)}$.

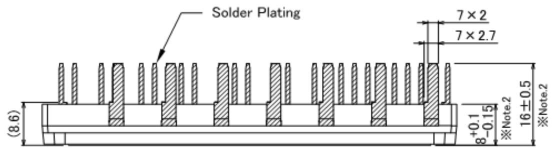
*20 : Recommended operating conditions are conditions for guaranteeing that the product operates normally. If it is used beyond this condition, operation and reliability may be adversely affected.

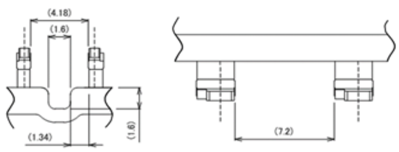
*21 : It is recommended to use low leakage current ceramic capacitor such as Murata Manufacturing RCER 71H series.

Package Outline dimensions (T_c=25°C)

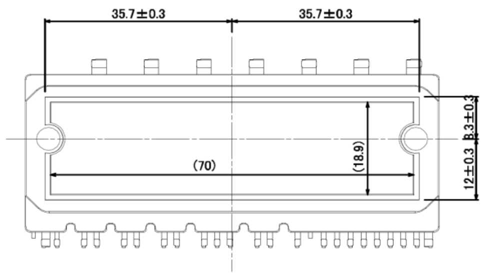








DETAIL A DETAIL B



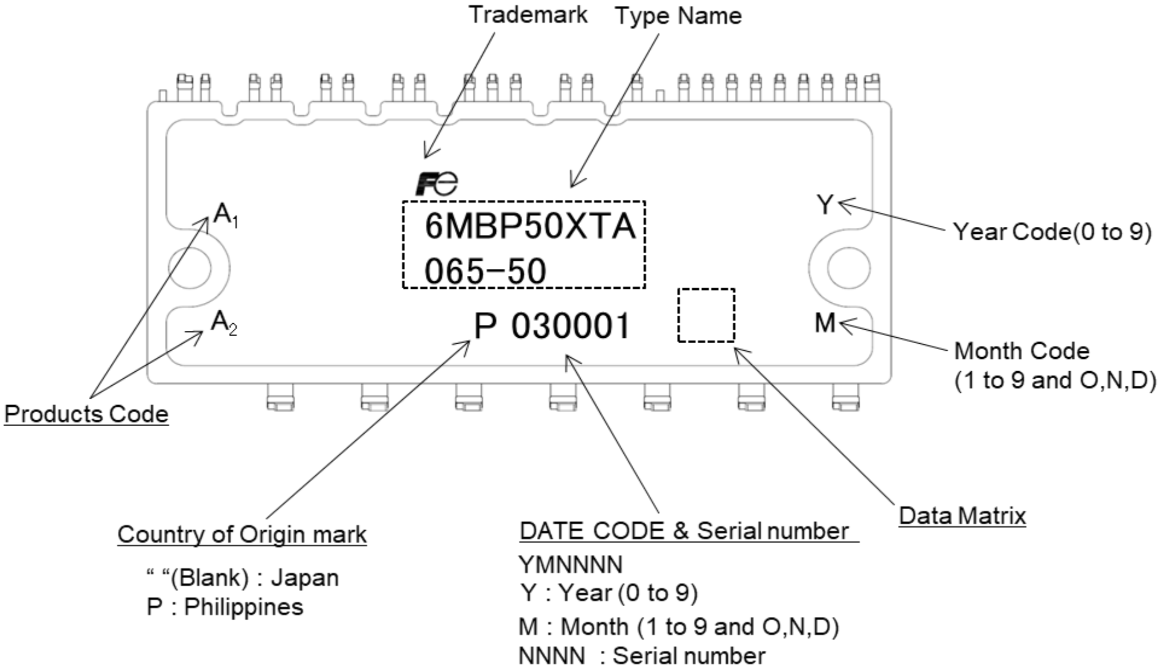
Unit:mm

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
2	IN(HU)	21	VSC	32	N(W)
3	VCCH(U)	23	VCCL	33	N(V)
5	VB(U)	24	COM	34	N(U)
6	VS(U)	25	TEMP	35	W
8	IN(HV)	26	IS	36	V
9	VCCH(V)	27	CFO	37	U
11	VB(V)	28	VFO	38	P
12	VS(V)	29	IN(LU)		
14	IN(HW)	30	IN(LV)		
15	VCCH(W)	31	IN(LW)		
16	COM				
18	VB(W)				
19	VS(W)				

Note.1
The IMS (Insulated Metal Substrate) is deliberately protruded to improve the thermal conductivity between IMS and heat-sink.

Note.2
Thickness from the package surface to the back side including the IMS.

Marking



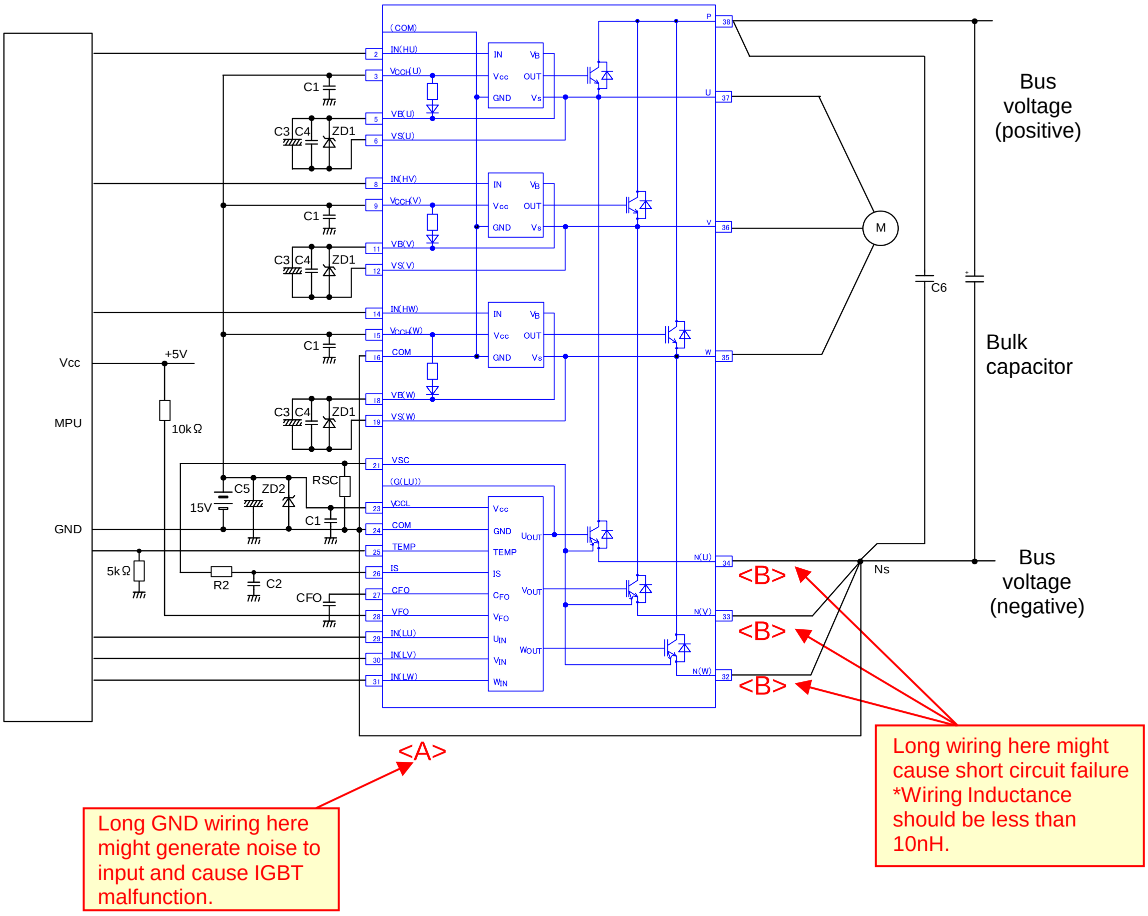
Note

Product code A_1 means current ratings , and "A" is marked.

Product code A_2 means variations , and "A" is marked.

An example of application circuit.

Fig. shows an example of an application circuit.



<Note>

1. Input signal for drive is High-Active. There is a pull-down resistor built in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using R-C coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
2. By the function of the HVIC, it is possible of the direct coupling to microprocessor (MPU) without any photo-coupler or pulse-transformer isolation.
3. VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.
4. To prevent erroneous protection, the wiring of (A), (B) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 1.1µs.
   Over current (OC) shutdown time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. All capacitors should be mounted as close to the terminals of the IPM as possible. (C1, C4 : narrow temperature drift, higher frequency and DC bias characteristic ceramic type are recommended, and C3, C5: narrow temperature drift, higher frequency and electrolytic type.)
7. To prevent surge destruction, the wiring between the snubber capacitor and the P terminal, Ns node should be as short as possible. Generally a 0.1µ to 0.22µF snubber capacitor (C6) between the P terminal and Ns node is recommended.
8. Two COM terminals (16 & 24 pin) are not connected inside the IPM, it must be both connected to the signal GND outside.
9. It is recommended to insert a zener-diode (22V) between each pair of control supply terminals to prevent surge destruction.
10. If signal GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect signal GND and power GND at only a point.
11. For sense resistor : R_{SC}, It should be pull down with 24 Ω or more to COM terminal, and the variation within 1% (including temperature characteristics), low inductance type is recommended. And the over 1/8W recommended, but it is necessary to evaluate in your real system finally.
12. Error signal output width(t_{FO}) can be set by the capacitor between CFO terminal and COM terminal. C_{FO}(typ.) = t_{FO} x (9.1 x 10^{-6}) (F)
13. When using an external shunt resistor for over current protection, use a chip-type shunt resistor with low inductance. Do not use a shunt resistor with a large inductance, such as a cement resistor.

Operation sequence

Fig.2-1 Switching waveforms

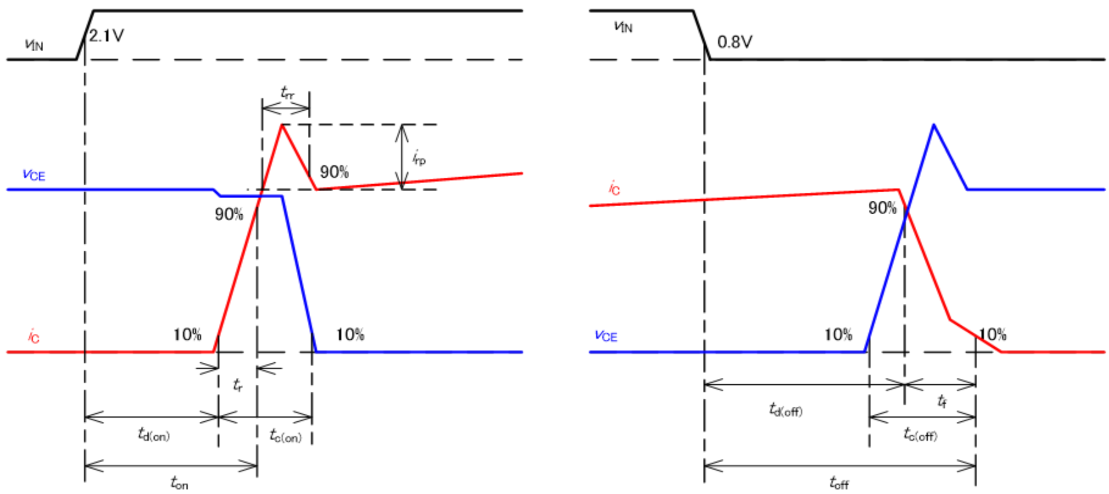
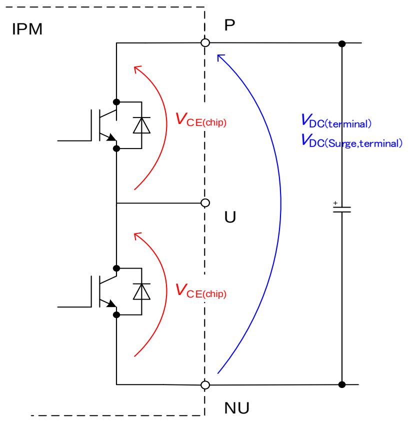


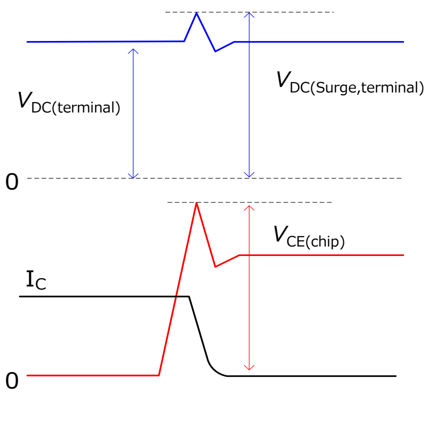
Fig.2-2 Rated Voltage



・$V_{DC(terminal)}$, $V_{DC(Surge,terminal)}$ are applied between P-N(U),P-N(V),P-N(W) at the lead stopper.

・$V_{CE(chip)}$ is Collector-Emitter voltage of internal IGBT chip.

[IGBT turn-off]



[FWD recovery]

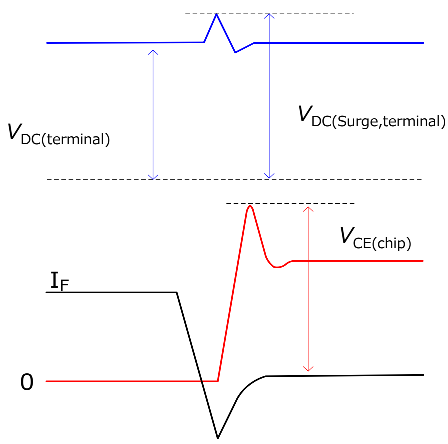
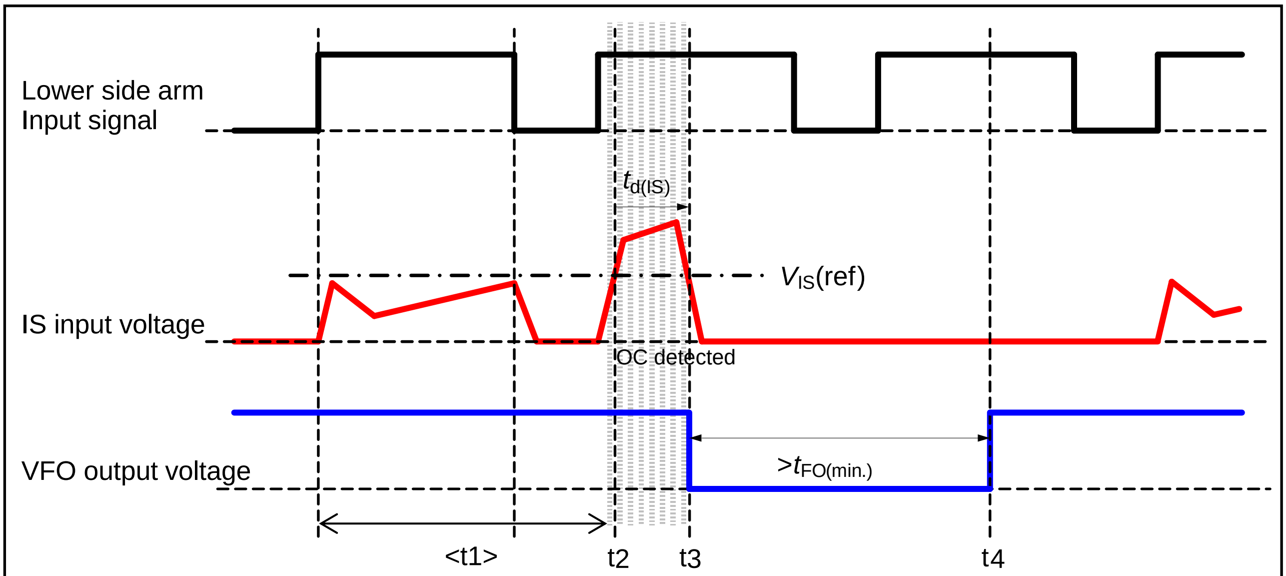


Fig.2-3 Operation sequence of Over current protection



Operation sequence of Over Current protection

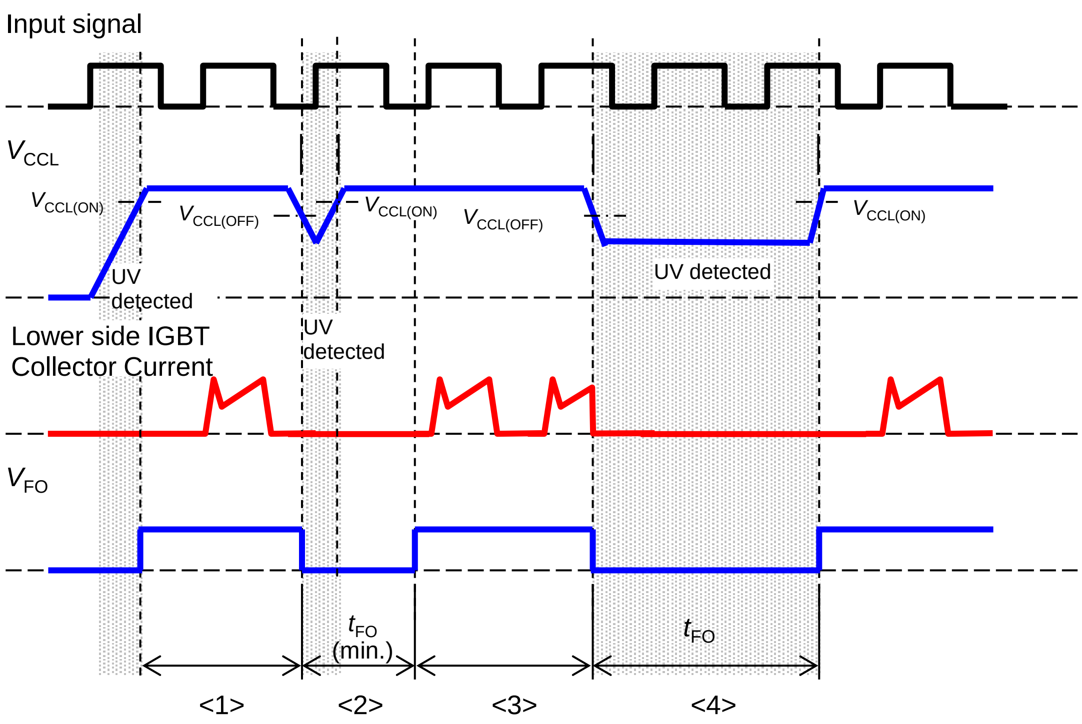
<t1> : IS input voltage does not exceed $V_{IS(ref)}$, while the collector current of the lower side IGBT is under the normal operation.

t2 : When IS input voltage exceeds $V_{IS(ref)}$, the OC is detected.

t3 : The fault output VFO is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $t_{d(IS)}$. Inherently there is dead time of LVIC in $t_{d(IS)}$.

t4 : After the fault output pulse width t_{FO}, the OC is reset. Then next input signal is activated.

Fig.2-4 Operation sequence of V_{CCL} Under voltage protection (lower side arm)



Operation sequence of V_{CCL} Under Voltage protection (lower side arm)

When V_{CCL} is under 4V, UV and fault output are not activated.

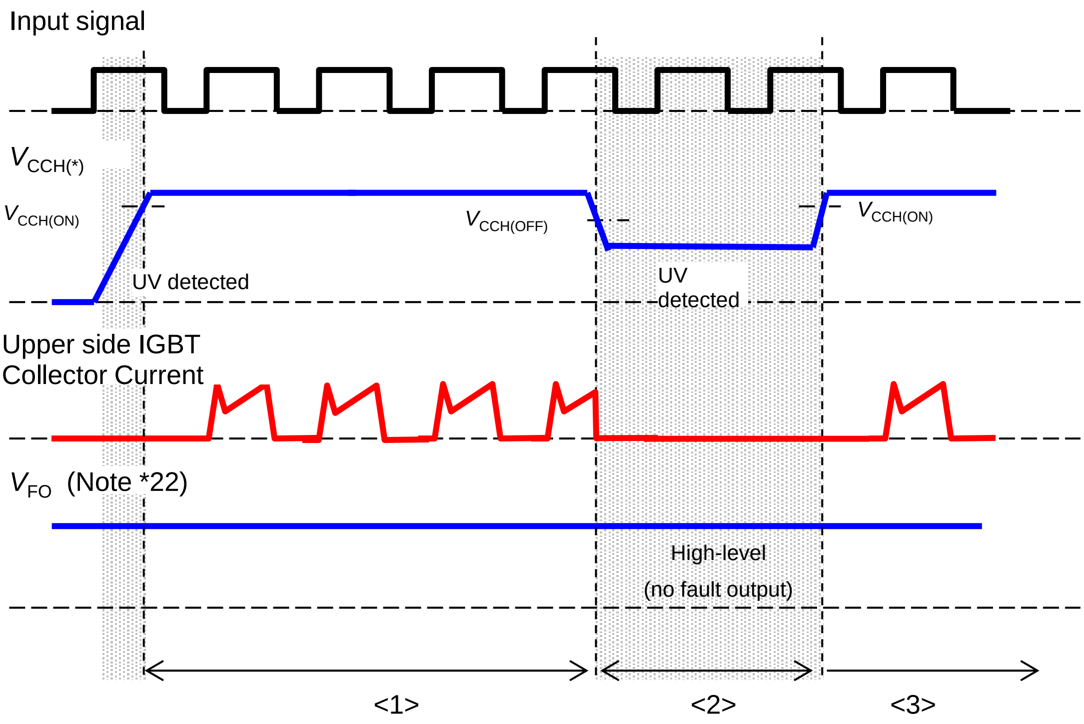
<1> When V_{CCL} is under $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} rises $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.

<2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
When the voltage drop time is less than t_{FO}(min.), the fault output pulse width is generated t_{FO}(min.) and all lower side IGBTs are OFF state in spite of input signal condition during that time.

<3> UV is reset after t_{FO} when V_{CCL} exceeds $V_{CCL(ON)}$ and the fault output VFO is reset simultaneously.
And the LVIC starts to operate, then next input is activated.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state in spite of input signal condition during the same time.

Fig.2-5 Operation sequence of $V_{CCH(*)}$ Under voltage protection (upper side arm)



Operation sequence of $V_{CCH(*)}$ (Note.*3) Under Voltage protection (upper side arm)

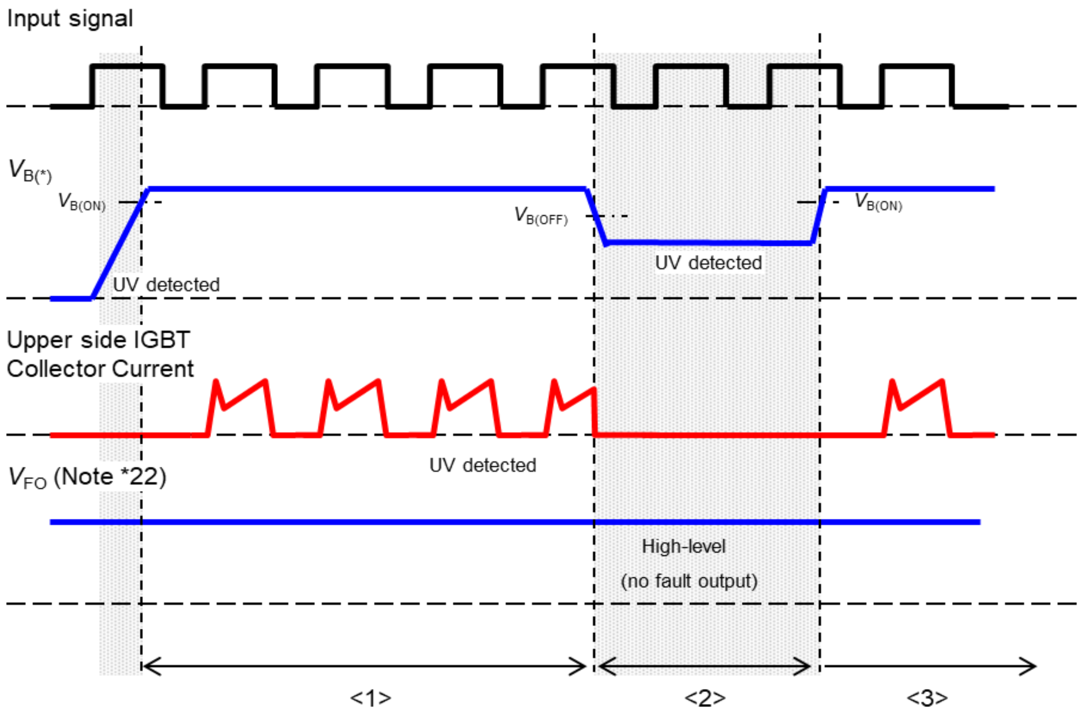
<1> When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ are under $V_{CCH(ON)}$, the corresponding upper side IGBTs are OFF state. After $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ exceed $V_{CCH(ON)}$, the corresponding upper side IGBTs start to operate. Then next input is activated.
The fault output VFO is constant (high level) not to depend on $V_{CCH(*)}$. (Note*22)

<2> After $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ fall below $V_{CCH(OFF)}$, the corresponding upper side IGBTs remain OFF state. But the fault output VFO keeps high level.

<3> The HVIC starts to operate after UV is reset, then next input is activated.

Note *22 : The fault output is not given HVIC bias conditions.

Fig.2-6 Operation sequence of $V_{B(*)}$ Under voltage protection (upper side arm)



Operation sequence of $V_{B(*)}$(Note.*4) Under voltage protection (upper side arm)

<1> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ are under $V_{B(ON)}$, the corresponding upper side IGBTs are OFF state.
After $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ exceed $V_{B(ON)}$, the corresponding upper side IGBTs start to operate.
Then next input is activated.
The fault output VFO is constant (high level) not to depend on $V_{B(*)}$. (Note*22)

<2> After $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ fall below $V_{B(OFF)}$, the corresponding upper side IGBTs remain OFF state.
But the fault output VFO keeps high level.

<3> The HVIC starts to operate after UV is reset, then next input is activated.

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