Critical conduction mode PFC IC
FA1B00N

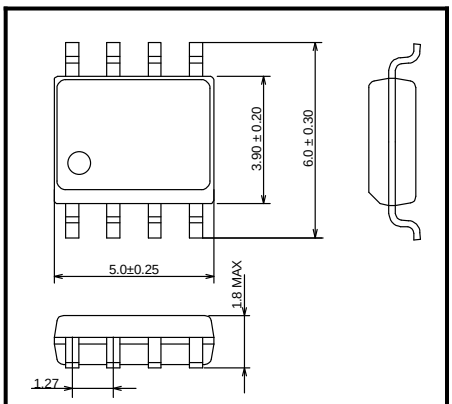
Datasheet

1. Overview

FA1B00N is power-factor correction converter IC operating in critical conduction mode. It realizes low power consumption by using high voltage CMOS process. It is equipped with many fault protection functions such as FB short-circuit detection circuit which stops the operation when abnormal output voltage is detected.

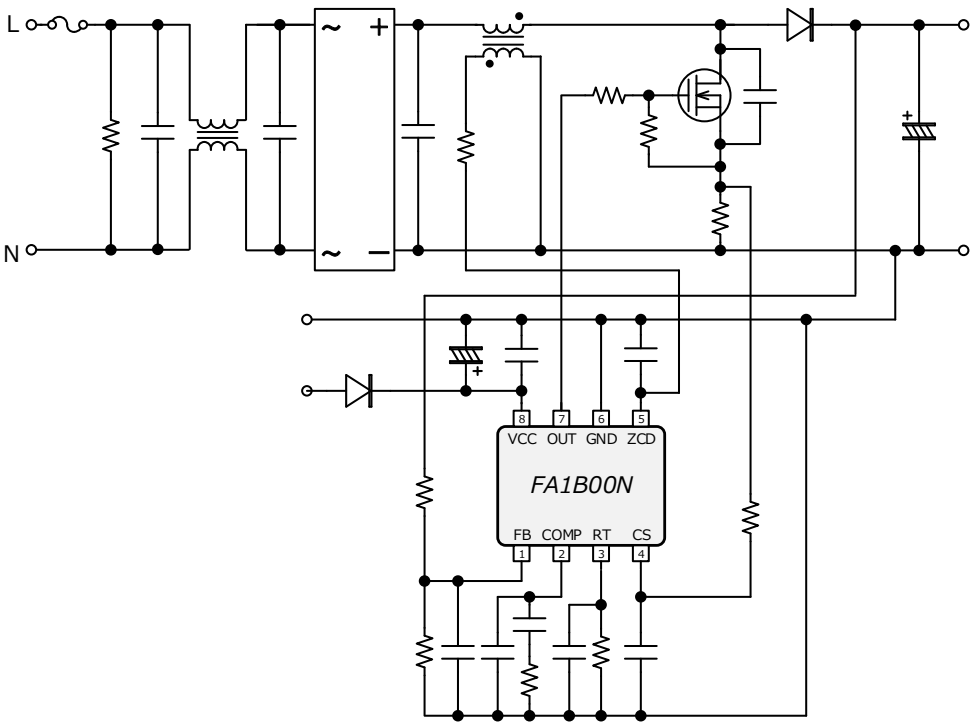
2. Features

- Very Low Standby Power by disusing Input Voltage Detection Resistors
- High-precision over current protection: 0.65V±2%
- Improved power efficiency at light load due to Maximum Frequency Limitation
- No Audible Noise at Startup by overshoot reduction circuit
- Low current consumption by CMOS process
- Start-up : 300μA(max.), Operating : 1.2mA(typ.)
- Enabled to drive power MOSFET directly
- Output peak current, source : 0.5A, sink : 1A
- Open/short protection at feedback (FB) pin
- Under-voltage Lockout, 13V ON / 9V OFF
- External signal-linked ON/OFF function built in FB pin
- 8-pin package: SOP-8

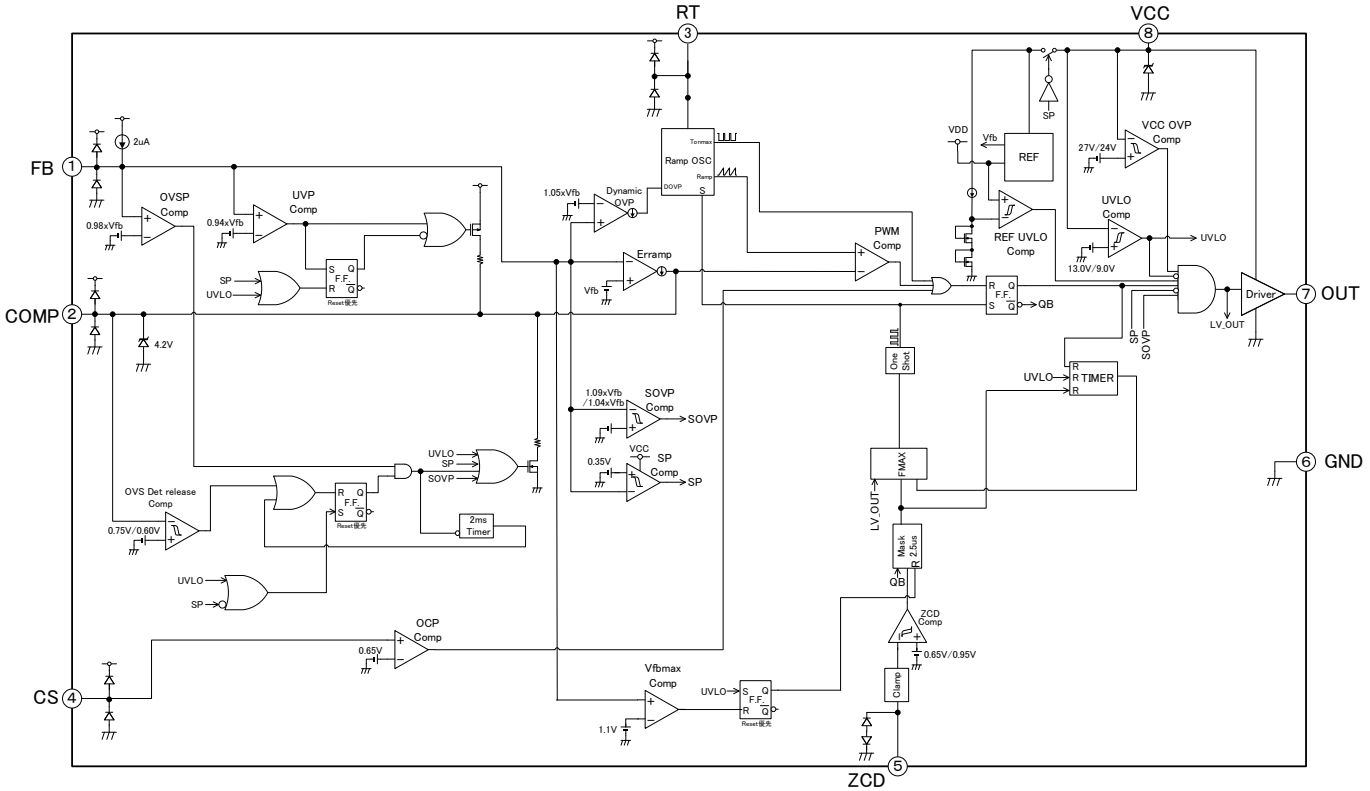


Package : SOP-8

3. Circuit diagram



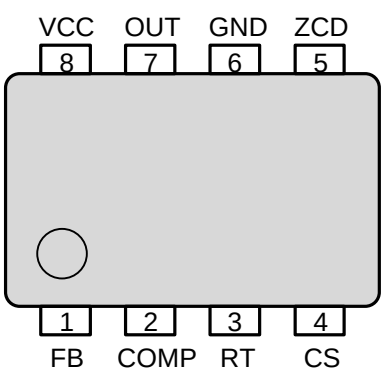
4. Block diagram



5. Description of pin functions

Pin No.	Pin name	I/O	Description	Note
1	FB	I	Voltage feedback input, Static over voltage protection(SOVP) , FB short protection, Under voltage protection(UVP)	*1
2	COMP	I/O	Error amplifier compensation	*1
3	RT	O	Maximum on time setting	*1,*2
4	CS	I	Current sense input, Over current protection	*1
5	ZCD	I	Zero current detect input	*1
6	GND	—	Ground	—
7	OUT	O	Output	—
8	VCC	I	Power supply, Under Voltage Lock Out(UVLO), Over Voltage Protection(OVP)	*1

Notes)
*1. Connects capacitor between pin and GND
*2. Connects resistor between pin and GND



6. Rating and characteristics

Malfunction or element damage can occur when exceeding the absolute maximum ratings.
The current value "-" represents the source, and "+" the sink.

(1) Absolute maximum ratings

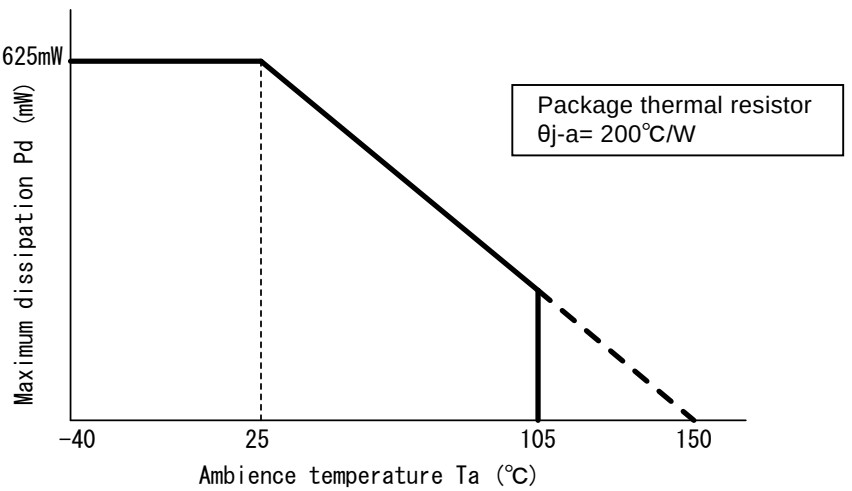
Item	Symbol	Rating	Unit
Supply voltage *1	*V*cc	-0.3 to 33	V
Voltage at OUT pin	*V*out	-0.3 to Vcc+0.3	V
Output peak current source or sink *1 *2	*I*o	-500 to +1000	mA
Control pin input voltage(FB)	*V*infb	-0.3 to 5.3	V
Control pin input current(FB)	*I*infb	+100 to -100	μA
Control pin input voltage(COMP)	*V*incomp	-0.3 to 5.3	V
Control pin input current(COMP)	*I*incomp	+100 to -100	μA
Control pin input voltage(RT)	*V*inrt	-0.3 to 5.3	V
Control pin input current(RT)	*I*inrt	+100 to -100	μA
Control pin input voltage(CS)	*V*incs	-0.3 to 5.3	V
Control pin input current(CS)	*I*incs	+100 to -100	μA
ZCD Voltage inputs	*V*inzcd	-3.5 to 7	V
Zero current detect input High state forward current	*I*inzcd	+2	mA
Low state reverse current		-2	
Power dissipation*1 (Ta=25℃)	*P*d	625	mW
Operating junction temperature	*T*j	-40 to +150	℃
Storage temperature	*T*stg	-40 to +150	℃

Notes）

*1 Please consider power supply voltage and load current well and use this IC within maximum temperature in operation. The IC may cross maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating value

*2 The period that exceeds 500mA must be 100ns or less.

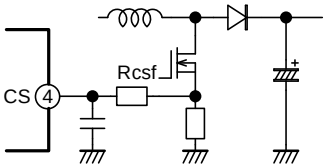
*Allowable loss reduction characteristic



(2) Recommended operating conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	*V*cc	10	12	24	V
VCC pin electrolytic capacitor	*C*vcce	10	-	47	uF
VCC pin ceramic capacitor	*C*vccc	0. 1	-	1	uF
RT pin resistance	*R*rt	20	39	200	kΩ
RT pin capacitor	*C*rt	0. 001	0. 01	0. 022	uF
FB pin resistance (output voltage divider resistor)	*R*fb	1	-	20	MΩ
CS pin filter resistance(fig. below)	*R*csf	47	-	100	Ω
ZCD pin current	*I*zcd	-	-	±1.5	mA
Operating ambient temperature	*T*a	-40	-	105	ºC

*The recommended operating conditions are to ensure that the product operates properly.
Use beyond these conditions can adversely affect operation and reliability.
*Use only after checking the operation with the actual device.



(3) Electrical characteristics (DC characteristics)

The measurement conditions are as follows, unless otherwise specified. The voltages described in the conditions are DC input, not AC input.

*T*j = 25°C, *V*cc = 12 V, *V*fb = 2.4 V, *V*comp = 4.2 V, *V*cs = 0 V, *V*zcd = 0 V, *R*rt = 39 KΩ, OUT pin open

Caution)

(1) We have not conducted a complete number of tests for items indicated with a "*1". The standard values are guaranteed by design.
(2) There are no guaranteed values for fields marked with a "-".
(3) In the output current characteristics, "-" represents the source current and "+" the sink current.

Error amplifier (FB pin, COMP pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage feedback input threshold	*V*fb		2. 475	2. 5	2. 525	V
Line regulation	Regline	*V*cc=10V to 24V	-20	-10	+20	mV
Temperature stability *1	*V*dT	*T*j=-30 to 85℃	-	±0.5	-	mV/ºC
Transconductance	*G*m	*V*fb(DC)=2.4V, 2.6V、*V*comp(DC)=Vfb *G*m=*I*comp_2.6-*I*comp_2.4/(2.6-2.4)	40	80	120	umho
Output source current	*I*compso	*V*fb(DC)=1.0V *V*comp(DC)=*V*fb	-45	-30	-15	uA
Output sink current	*I*compsi	*V*fb(DC)=2.65V, *V*comp(DC)=*V*fb	6	12	18	uA
COMP pull-up FB voltage *2	*V*fb_co pull	*V*fb(DC) decrease	0.92 x *V*fb	0.94 x *V*fb	0.96 x *V*fb	V
FB voltage drop COMP pull-up resistor *2	*R*comp_pul	*V*fb(DC)=2.0V *V*comp(DC)=1.0V	40	50	60	kΩ

*2: If the FB pin voltage falls below the "COMP pull-up FB voltage", the COMP pin is pulled up by the "COMP pull-up resistor at FB voltage drop" (except at startup).

Lamp oscillator (RT pin, COMP pin, FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OUT pin maximum on time (At normal operation)	*T*onmax	*V*fb(DC)=2.4V *V*comp(DC)=4.2V *R*rt = 39 kΩ	9.5	13	16.5	μs
OUT pin maximum frequency	*F*max	*R*rt = 82 kΩ	180	250	320	kHz
Maximum frequency Voltage *3	*V*fbmax	*V*fb(DC) increase	0.9	1.1	1.3	V
COMP pin threshold voltage for stop switching at OUT pin	*V*thcomp	*V*comp(DC) decrease Switching at OUT pin stop	0.54	0.6	0.66	V
RT pin output voltage	*V*rt	*V*fb(DC)=2.4V	0.95	1.1	1.25	V
COMP pin clamp voltage	*V*clpcomp	*V*fb(DC)=1V	4.1	4.2	4.3	V

*3 : After starting the IC, until FB pin voltage goes over the "Maximum frequency voltage" once, off-time of the OUT pin is "Restart timer delay ". And it goes over "Maximum frequency voltage" once, off-time of the OUT pin is "OUT pin maximum frequency lock time " or " (1/"OUT pin maximum frequency") - "OUT pin on time""

Overvoltage protection comparator (FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static OVP Threshold voltage	*V*sovph	*V*fb(DC) increase Switching at OUT pin stop	1.070 x *V*fb	1.090 x *V*fb	1.105 x *V*fb	V
	*V*sovpl	*V*fb(DC) decrease Switching at OUT pin start	1.020 x *V*fb	1.040 x *V*fb	1.060 x *V*fb	V
	*V*sovphys	*V*sovph – *V*sovpl	0.030 x *V*fb	0.040 x *V*fb	0.060 x *V*fb	V
Pull up current	*I*pullup	*V*fb=2.5V	-2.6	-2.0	-1.4	μA
Dynamic OVP Threshold voltage	*V*dovp	*V*fb(DC) increase *T*on=*T*onmax x 0.7	1.025 x *V*fb	1.050 x *V*fb	1.075 x *V*fb	V
Staric to dynamic OVP (70%) hysteresis voltage	*V*hyssd	*V*sovph-*V*dovp	0.010 x *V*fb	0.030 x *V*fb	0.050 x *V*fb	V
COMP pin pull down resistance at sovp *4	*R*comp_ sovp	*V*FB (DC) > *V*sovph *V*COMP(DC) =1.0V	1.75	2.50	3.25	kΩ

*4 FB pin voltage becomes over “Static OVP threshold voltage ”,
COMP pin is pulled down by “COMP pin pull down resistance”.

FB short circuit detection comparator (FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FB pin Threshold voltage	*V*thfb	*V*fb(DC) increase Switching at OUT pin stop	0.15	0.35	0.55	V

Current sense comparator (CS pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CS pin threshold voltage for stop switching at OUT pin	*V*thcsh	*V*cs increasing DC input voltage	0.637	0.65	0.663	V
CS threshold voltage Temperature dependency *1	*V*thcshdt	*T*j=-40℃~85℃	-1.5	-	+1.5	%
Delay to output	*T*phl	*V*cs(PULSE) High level =700mV Low level = 0V dV/dT= 40V/us	100	180	400	ns

Zero current detection (ZCD pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ZCD pin threshold voltage for stop switching at OUT pin	*V*thzcdh	*V*zcd(DC) increasing	0.884	0.95	1.017	V
ZCD pin threshold voltage for start switching at OUT pin	*V*thzcdl	*V*zcd(DC) decreasing	0.585	0.65	0.715	V
Hysteresis voltage	*V*hyszcd	*V*thzcdh-*V*thzcdl	0.2	0.3	0.4	V
Input clamp voltage	*V*ih	*I*source=-3.0mA	5.6	6.6	7.6	V
	*V*il	*I*sink=+3.0mA	-2.9	-1.9	-0.6	V
Minimum detect pulse width *1	*T*mw	*V*zcd(pulse) : High level=2V Low level=0.3V dv/dt= 40V/us *V*zcd low pulse width decrease	150	-	-	ns
Delay to output	*T*zcd	*V*zcd(pulse) : High level=2V Low level=0.3V dv/dt= 40V/us	100	140	300	ns
Maximum frequency lock time	*T*zcdmax	V_{FB}(DC)=2.4V	1.7	2.5	3.3	μs
Temperature stability of maximum frequency lock time *1	*V*zcdmaxdt	*T*j=-40℃ to 85℃	-	±5	±10	%

Output (OUT pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage low state	*V*ol	*V*comp(DC)=0V *I*sink(OUT)= 200mA	-	1.2	3.3	V
Output voltage high state*1	*V*oh	*I*source(OUT)= 50mA	8	9	10	V
Output voltage rise time	*T*r	*C*out=1000pF	-	50	120	ns
Output voltage fall time	*T*f	*C*out=1000pF	-	25	100	ns

Restart timer (ZCD pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OUT pin restart timer delay	*T*dly	V_{FB}(DC)=0.8V	15	30	45	μs

Low voltage protection (VCC pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Startup threshold voltage	*V*on	*V*cc(DC) increase Switching at OUT pin start	11.5	13	14	V
Shutdown threshold voltage	*V*off	*V*cc (DC) decrease Switching at OUT pin stop	8	9	10	V
Hysteresis width	*V*hysvcc	*V*on – *V*off	3	4	5	V
NMOS on resistance *2	*R*comp UVLO	V_{VCC} (DC) > *V*off V_{COMP} (DC)=1.0V	1.75	2.5	3.25	kΩ

Consumption current (VCC pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Startup power supply current	*I*start	*V*cc(DC)=Von-0.1V	100	200	300	μA
Operating power supply current	*I*cc	*C*out=OPEN	0.3	0.8	1.3	mA
Dynamic operating power supply current	*I*op	*C*out=1000pF	0.5	1.2	1.9	mA
Stand-by current	*I*stb	*V*fb=0V	-	30	60	μA

VCC overvoltage protection (VCC pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VCC overvoltage protection operation Threshold voltage	*V*ccovph	VCC increase OUT switching stop	25	27	29	V
VCC overvoltage protection release Threshold voltage	*V*ccovpl	VCC increase OUT switching start	22	24	26	V
Hysteresis width	*V*hysovp	*V*ccovph-*V*ccovpl	2	3	4	V

Overshoot reduction (FB pin, COMP pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Overshoot reduction operation FB pin voltage *5	*V*thfbovs	*V*fb(DC) increase	0.96 x *V*fb	0.98 x *V*fb	0.995 x *V*fb	V
COMP pin pull-down resistor at overshoot reduction operation *1 *5	*R*comp_ovs	*V*fb (DC) increase	1.75	2.5	3.25	kΩ
Overshoot reduction Operating time *1 *6	*T*ovs	*V*fb (DC) increase	1	2	3	ms
Overshoot reduction release COMP pin Threshold voltage *6	*V*comp_ovsh	*V*comp(DC) increase	0.70	0.75	0.80	V
	*V*comp_ovsl	*V*comp (DC) decrease	0.55	0.60	0.65	V

*5 If the FB pin voltage exceeds the “overshoot reduction operation FB pin voltage” at startup, pull-down will occur via the “COMP pull-down resistor at COMP pin overshoot reduction operation”.

*6 If the overshoot operating time elapses or if the COMP pin voltage falls below the “overshoot reduction release COMP pin voltage”, pull-down will be released.

7. Characteristic curve

The measurement conditions are as follows, unless otherwise specified.

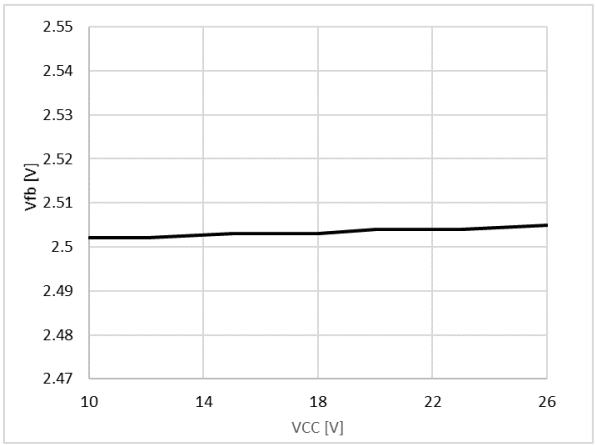
*T*j = 25°C, *V*cc = 12 V, *V*fb = 2.4 V, *V*comp = 4.2 V, *V*cs = 0 V, *V*zcd = 0 V, *R*rt = 39 kΩ, OUT pin open

Notes)

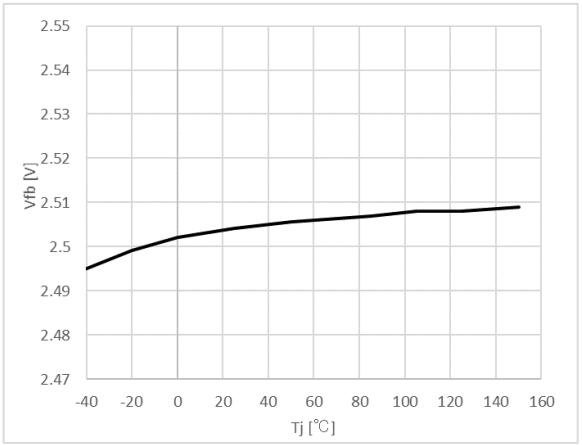
(1) The current specification "-" represents the source, and "+" the sink.

(2) The data described here shows the characteristics of typical ICs and does not guarantee the characteristics.

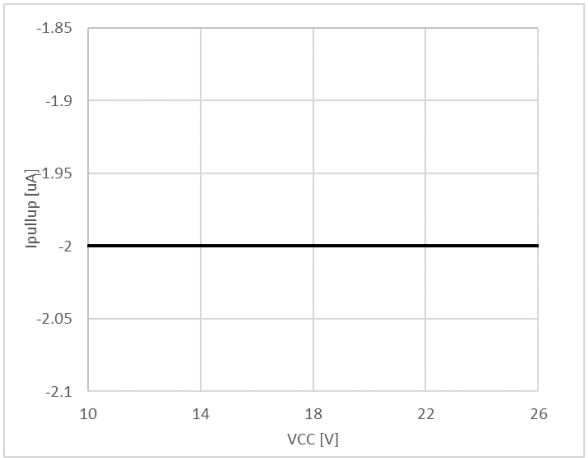
Error amplifier voltage feedback input threshold(Vfb) vs. supply voltage(Vcc)



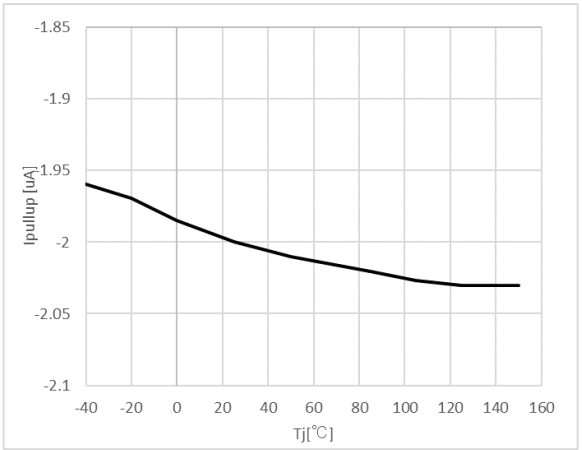
Error amplifier voltage feedback input threshold(Vfb) vs. junction temperature(Tj)



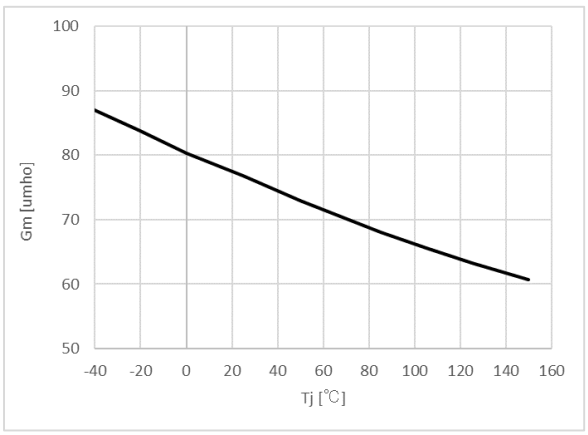
Pull up current (Fb) vs. supply voltage(Vcc)



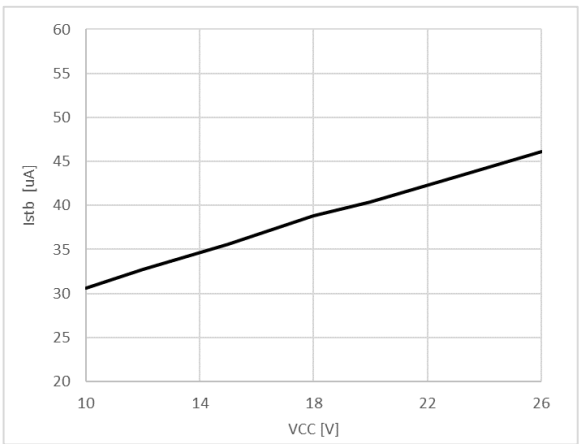
Pull up current (Fb) vs. junction temperature(Tj)



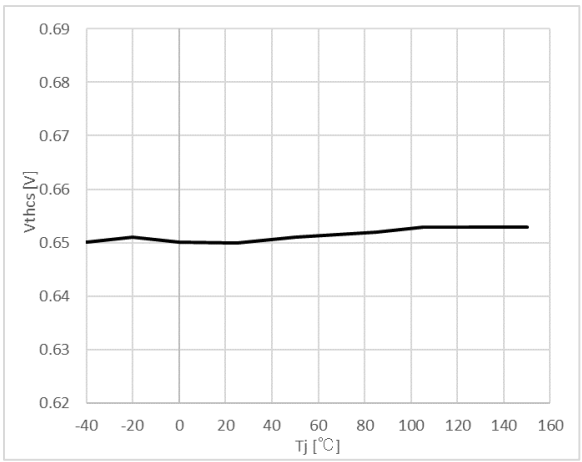
Error amplifier transconductance(Gm) vs. junction temperature(Tj)



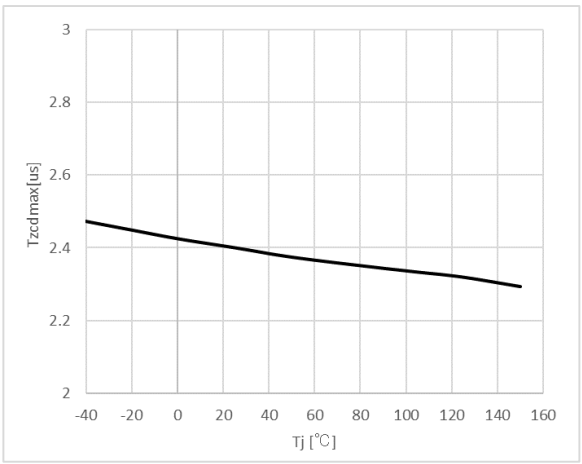
Standby current(Istb) vs. supply voltage(Vcc)



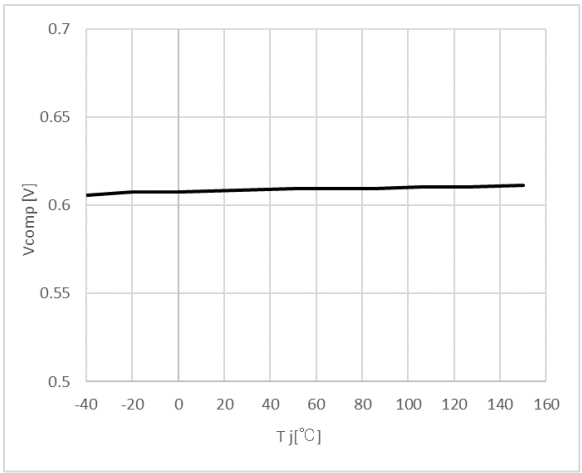
Current sense comparator maximum threshold(Vthcs) vs. junction temperature(Tj)



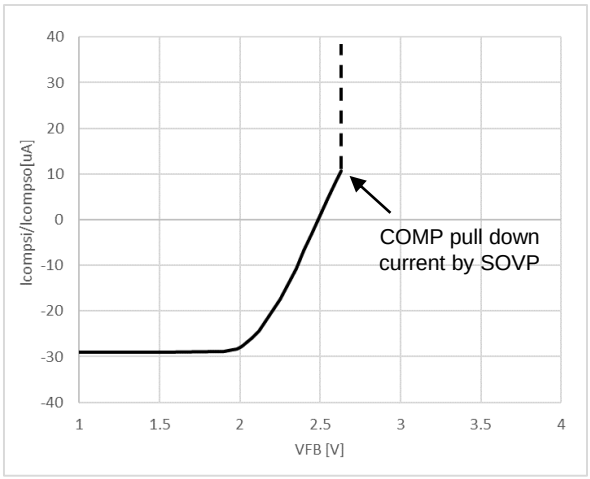
Maximum frequency lock time (Tzcdmax) vs. junction temperature(Tj)



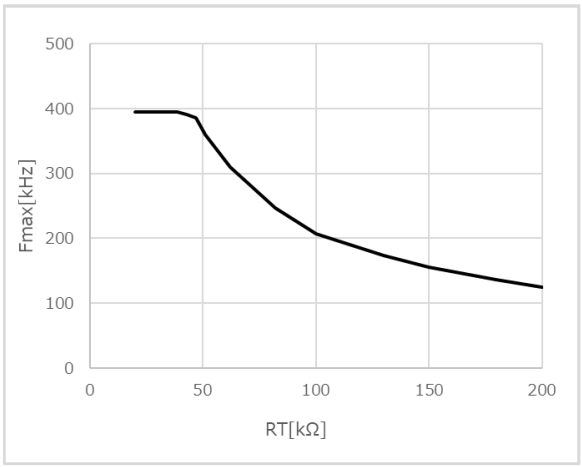
COMP Threshold voltage (Vthcomp) vs. junction temperature(Tj)



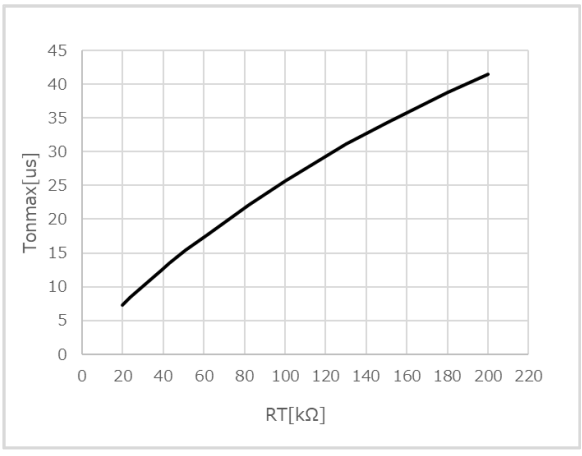
Error amplifier sink/source current (Icompsi/Icompso) vs. FB Pin voltage(VFB) Vcomp=2.5V



Maximum oscillating frequency(Fmax) vs. RT resistance(Rrt)



Maximum on-range(Tonmax) vs. RT resistance(Rrt)



8. Overview of boost chopper circuit operation

The IC has been designed to facilitate control of power factor improvement converters that utilize a boost chopper or flyback. It makes use of critical mode operation. This section uses the boost chopper schematic diagram in Fig. 1 to summarize the two types of operation: switching operation and power factor improvement operation.

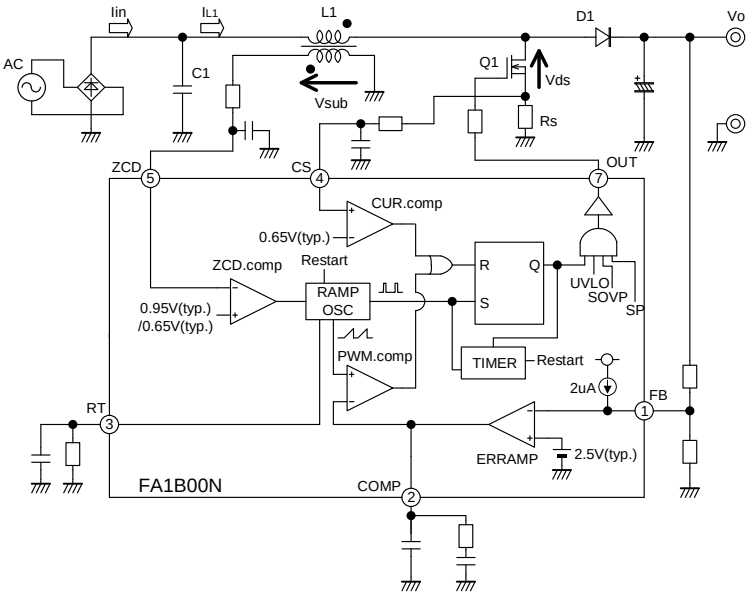


Fig. 1: Schematic operation circuit block

(1) Switching operation

The IC performs switching operation in critical mode via self-oscillation without the use of an oscillator. An overview of the switching operation waveforms in steady state is shown in Fig. 2. The operation is as follows:

t1. When Q1 is turned on, the current of the inductor (L1) rises from zero. Furthermore, the output Vramp of the lamp oscillator rises when Q1 is turned on.

t2. The PWM comparator compares the output Vramp of the lamp oscillator with the output Vcomp of the error amplifier. If Vramp > Vcomp, Q1 is turned off and the output of the lamp oscillator is decreased. When Q1 turns off, L1 voltage is inverted, and L1 current decreases while providing current to the output side via D1. At such a time, the voltage of the auxiliary winding is also inverted and a positive voltage is generated.

t3. When L1 current completely returns to zero, L1 voltage resonates with the parasitic capacitors inside the circuit and decreases rapidly. At the same time, the voltage Vsub of the auxiliary winding in L1 also decreases rapidly.

t4. When the Vsub drops to the internal reference voltage of 0.65 V (typ.), the output of the zero current detector (ZCD.comp) becomes high, a pulse is output from the lamp oscillator, Q1 is turned on, and transition is made to the next switching cycle (t1).

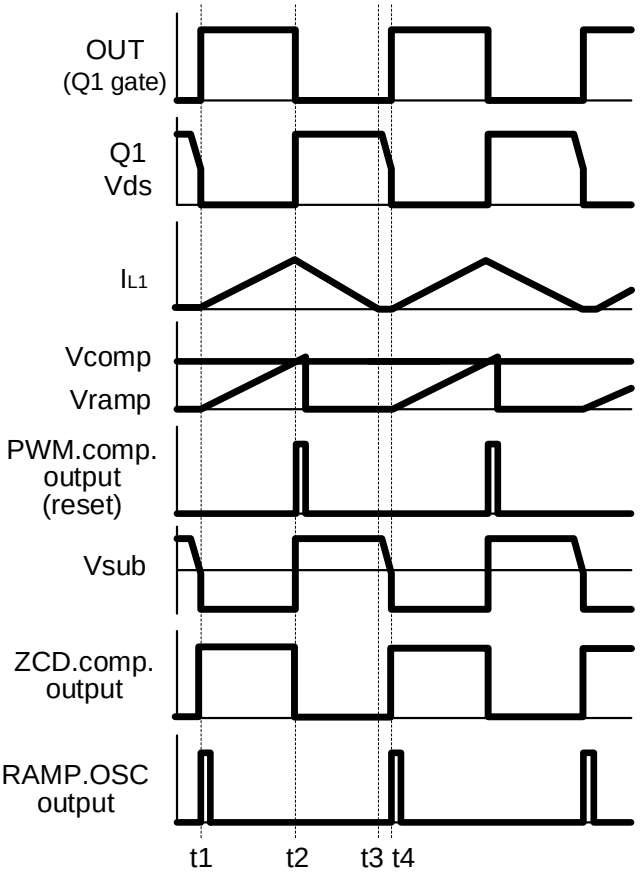


Fig.2: Waveforms of each part of switching operation (overview)

Switching continues in critical mode by repeating the operations described in t1. to t4.
In the critical mode based power factor improvement circuit, the switching frequency constantly changes in accordance with each of the instantaneous values of the AC input voltage. Moreover, the switching frequency also changes when the input voltage or load changes.

(2) Power factor improvement operation of the boost chopper PFC

As described in the switching operation section, the current flowing through the inductor is a repeating triangular wave. The mean value of this continuous triangular wave-like current (I_{L1}(mean)) becomes 1/2 of the peak value (I_{L1}(peak)). (Fig. 3)
By controlling the peak values of the inductor current in a sine wave-like manner and removing the ripple current associated with switching, the current flowing from the AC input power supply can be made into a sine wave.

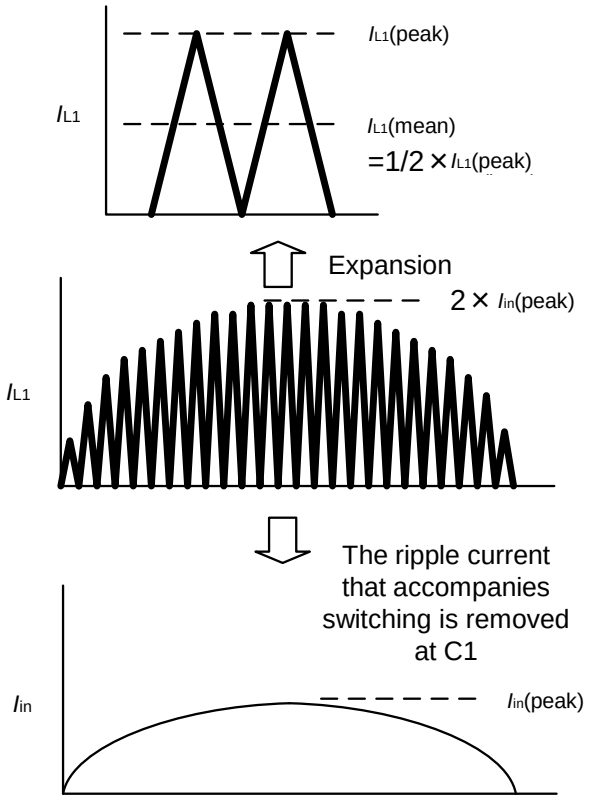


Fig. 3: Power factor improvement operation waveform for the boost chopper circuit

The FA1B00N makes use of a control method characterized by on-width fixed control as shown in Fig. 4. On-width fixed control determines the on-width of the IC output (Power Mos gate signal) by coinciding the sawtooth wave with the error amplifier. Since the output of the error amplifier is constant when the load is constant, the on-width will also be constant.
Since the slope of the inductor current depends on the input voltage (the slope becomes steeper as the input voltage increases) and the on-width is constant, the peak waveform of the inductor current will have the same AC waveform as the input voltage, thus enabling the power factor improvement operation.

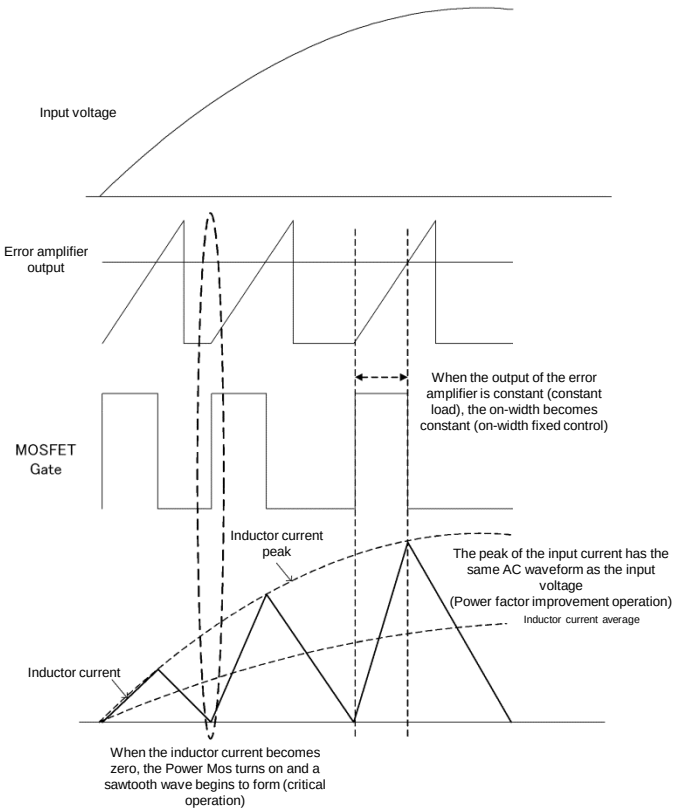


Fig. 4: On-width fixed control (overview)

9. Description of each block operation

The standard values in the following explanations are typical values unless otherwise specified.

(1) Error amplifier

The error amplifier controls the output voltage in order to ensure a constant voltage. The IC uses a transconductance amplifier. The transconductance amplifier uses the voltage as the input signal and the current as the output signal.

The non-inverting input pin is connected to a 2.5 V internal reference voltage inside the IC.

The inverting input pin is used to input the output voltage of the power factor improvement converter. It inputs the normal converter output voltage via resistance voltage dividing. Furthermore, the inverted input is connected to a constant current source of 2 µA inside the IC to enable the FB open detection function.

The error amplifier output (COMP) is connected to the PWM comparator to control the on-width of the OUT output.

The output voltage of the PFC often contains twice as much frequency ripple as the normal AC line frequency (generally, 50 or 60 Hz). If a ripple component corresponding to twice the frequency of the AC line has a considerable influence on the error amplifier output, the power factor improvement converter will not operate stably. Therefore, phase correction is usually implemented by connecting a capacitor or resistor between GND and pin 2 (COMP), i.e., the output of the error amplifier.

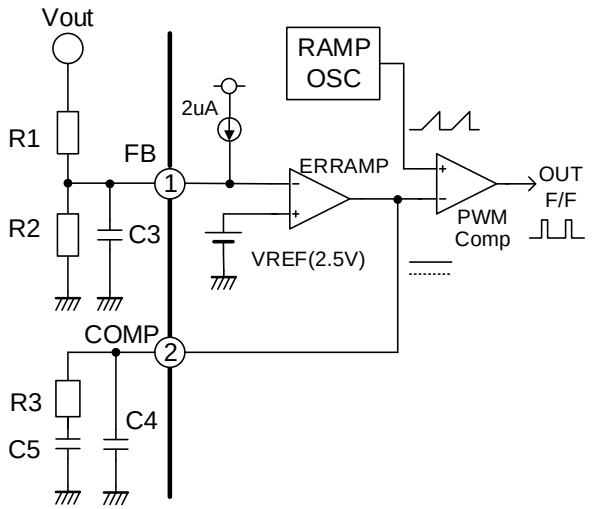


Fig. 5: Error amplifier peripheral circuit

(2) Overvoltage protection circuit (OVP)

This circuit limits the voltage when the output voltage of the power factor improvement converter exceeds the set value. The output voltage of the converter may also rise above the set value at certain times, such as when the converter starts up or when there is a sudden load change. In such a case, the rise in the output voltage will be suppressed and the circuit protected.

FA1B00N comes equipped with a dynamic OVP function that linearly limits the on-width when it reaches 1.05 times the FB pin voltage Vfb, as well as a static OVP function that stops the OUT pin output when it reaches or exceeds 1.09 times the Vfb.

Normally, FB pin voltage operates at 2.5 V, which is approximately the same as the reference voltage of the error amplifier. If the output voltage rises due to start-up or sudden load change and the FB pin voltage rises above 2.5 V, the on-width will first be narrowed by the dynamic OVP function. If it continues to rise and exceeds the comparator reference voltage, the output of the output voltage of the comparator (OVP) will then be inverted and OUT pin output will be stopped. (Fig. 6)

When the output voltage returns to a value less than or equal to 1.05 times the reference voltage, the pulse will be output from the OUT pin again.

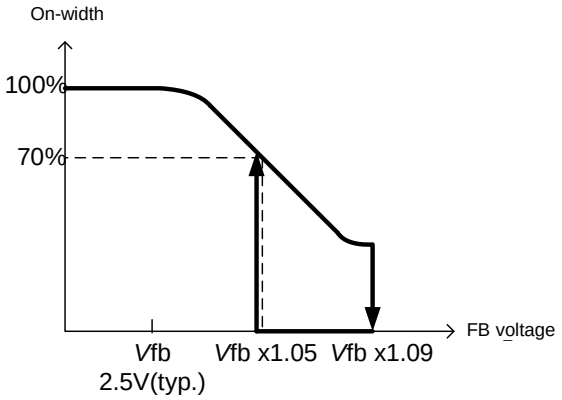


Fig. 6: On-width during overvoltage

(3) FB short circuit/open detection circuit

In the FB pin peripheral circuit of the boost chopper circuit shown in Fig. 7, if no voltage is input to the FB pin, such as when the resistance voltage-dividing circuit of the FB pin has an R2 short circuit failure or R1 open failure, the error amplifier will not be able to control the constant voltage and output voltage will rise abnormally. In such a case, the detection of the output voltage will be abnormal, and this will also prevent the overvoltage protection circuit from operating.

In order to avoid this, the IC includes an integrated FB short-circuit detection circuit.

This circuit is composed of a reference voltage of 0.35 V (typ.) and a comparator (SP). If the input voltage of the FB pin falls below 0.35 V due to an R2 short circuit failure or R1 open failure, the output of the comparator (SP) will be inverted, and the OUT output and internal circuit of the IC will be stopped.

Furthermore, if there is an open failure between the FB pin and the resistance voltage-dividing circuit, the FB pin voltage will be forcibly raised by a 2 µA constant current source connected to the FB pin inside the IC. Since the error amplifier output (COMP) voltage is reduced due to the rise in FB pin voltage, the OUT output will be stopped or PFC output voltage reduced.

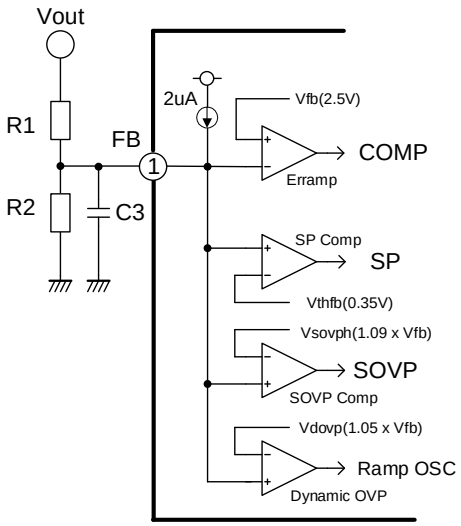


Fig. 7: FB pin peripheral circuit

(4) Ramp oscillation circuit

The ramp oscillation circuit receives a signal from the zero current detection circuit or restart circuit, and outputs an F/F set signal for OUT output and a sawtooth wave signal for PWM comparator duty determination.

(4-1) Maximum frequency limitation

The critical mode PFC switching frequency rises during light loads.

FA1B00N includes a maximum frequency limitation function to improve efficiency during light loads. The rise in frequency is limited to *F*max (Hz) during light loads. (Fig. 8)

Maximum frequency *F*max is determined by the resistor connected between the RT pin and GND.

When the switching frequency is at or below maximum frequency *F*max, it is turned on when Vds is at the bottom through detecting a zero level inductor current and turning the MOSFET on, as shown in Figure 9.

When the switching frequency is limited to maximum frequency *F*max during a light load, it is turned on at a cycle of 1/Fmax without detecting a zero level inductor current and turning on after the zero current detection delay *T*zcd, as shown in Figure 10.

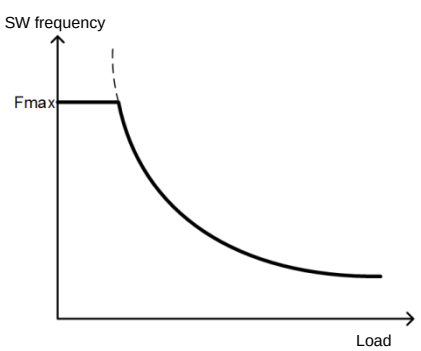


Fig. 8: Maximum frequency limit

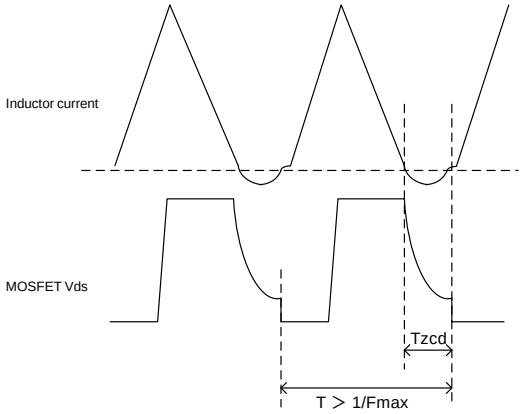


Fig. 9: SW frequency at or below maximum frequency

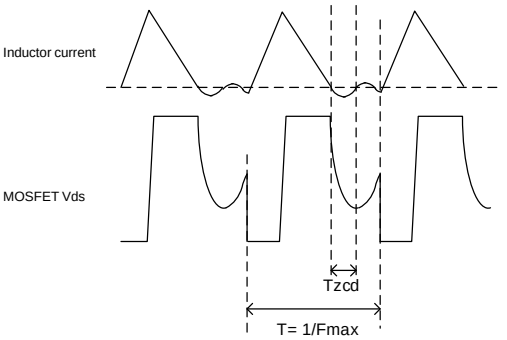


Fig. 10: Frequency limited to maximum frequency

(5) Zero current detection circuit

This IC performs switching operations in critical mode, which uses self - oscillation rather than a fixed frequency from the oscillator.

Zero current detection circuit ZCD.comp is used to detect that the inductor current has dropped to zero, in order to perform critical mode operations.

The voltage from the auxiliary winding (sub) attached to the inductor is input to the ZCD pin at the polarity shown in Figure 11. When this happens, a positive voltage will be generated for the auxiliary winding during the off period of the MOSFET. Then, once the inductor current falls to zero, the auxiliary winding voltage suddenly drops. This voltage drop is detected by ZCD.comp to make transition to the next cycle, and the ramp oscillation circuit (RAMP OSC) sends the set signal to the R-S flip-flop and turns the MOSFET on.

The voltage of the auxiliary winding changes significantly depending on factors such as the circuit or input voltage. It therefore includes a clamp circuit with an upper limit of 6.6 V and a lower limit of -1.9 V.

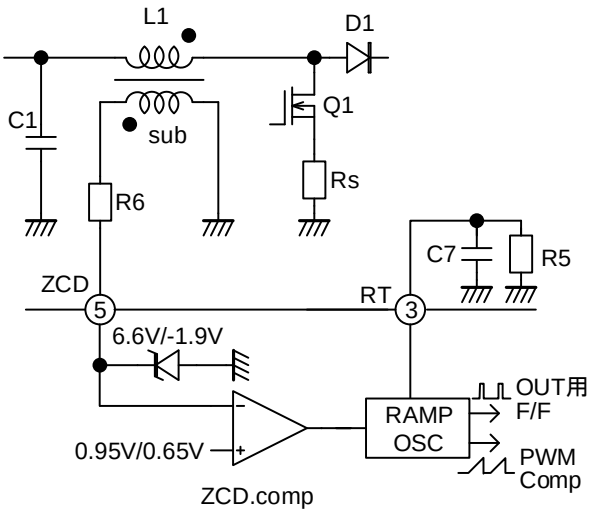


Fig. 11: Zero current detection peripheral circuit

(6) Overcurrent detection protection circuit

The overcurrent detection protection circuit detects the inductor current and then protects the MOSFET by turning OUT output off when the current is at a certain level or higher. (Fig. 12)

During overcurrent detection, the voltage generated in current detection resistor Rs (connected between the MOSFET source and the GND line) is input to the CS pin and then compared by the overcurrent detection comparator. If the CS pin voltage is 0.65 V or higher, it is output as an overcurrent state. When an overcurrent is detected, OUT output F/F is reset and the MOSFET is turned off.

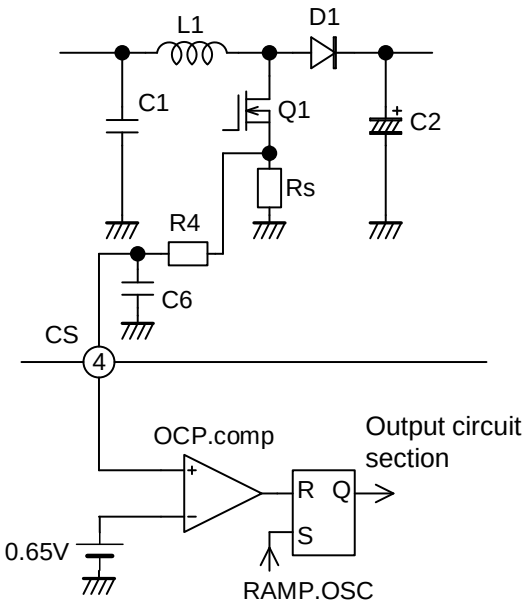


Fig. 12: Overcurrent protection circuit

(7) Restart timer

This IC uses self - oscillation rather than a fixed frequency from the oscillator to turn the MOSFET on using a signal from the zero current detector when in a steady state. However, some kind of trigger signal will be required when generating the initial on signal (such as during startup) or when performing stable operations during light loads. This IC therefore includes a restart timer.

During startup, the restart timer generates a trigger signal while the ZCD pin voltage is at a low level and the off period for OUT output continues for at least 30 us, up until the point where the FB pin voltage exceeds maximum oscillation frequency operation voltage *V*fbmax (1.1 V) once.

If the FB pin voltage is equal to or greater than maximum oscillation frequency operation voltage *V*fbmax (1.1 V), it is turned on in a state limited to the maximum frequency due to the ZCD pin voltage being at a low level.

This allows for stable operation even during startup or under a light load.

(8) Under voltage lock out (UVLO)

The built-in under voltage lock out (UVLO) prevents circuit malfunction when the power supply voltage drops.

As the power supply voltage rises from zero, it begins operating at 13 V for FA1B00N.

Once operation begins, as the power supply voltage drops, it stops operating at 9 V, and the capacitor connected to the COMP pin is discharged by the discharge circuit inside the COMP pin.

The under voltage lock out operates, and then the OUT pin switches to low and output is blocked while the IC is stopped.

(9) External signal-linked ON/OFF function

This IC contains a function that allows an external signal to stop OUT pin output. There are two possible methods. The first is to pull down the FB pin voltage to 0.35 V or less (Figure 13), while the second is to pull down the COMP pin voltage to 0.6 V or less (Figure 14). In the first method, a rise in the FB pin voltage is detected once the pull down has been released and OUT output begins, and then the overshoot reduction function operates.

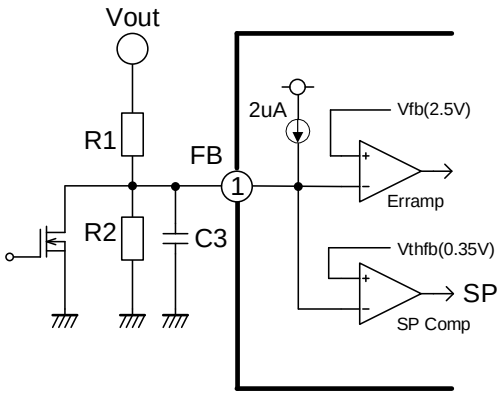


Fig. 13: ON/OFF using FB pin

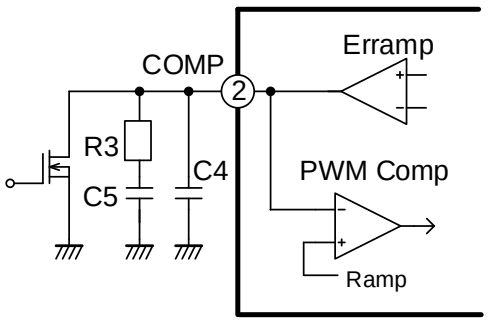


Fig. 14: ON/OFF using COMP pin

(10) Overshoot reduction circuit

FA1B00N contains an overshoot reduction function to suppress output voltage overshooting during startup. The overshoot reduction circuit temporarily pulls down the COMP pin voltage once the overshoot reduction operation start FB voltage (0.98 × Vfb) or higher is reached from UVLO release, curbs output voltage rising by limiting the on width of the OUT pin, and reduces overshooting. (Fig. 15)

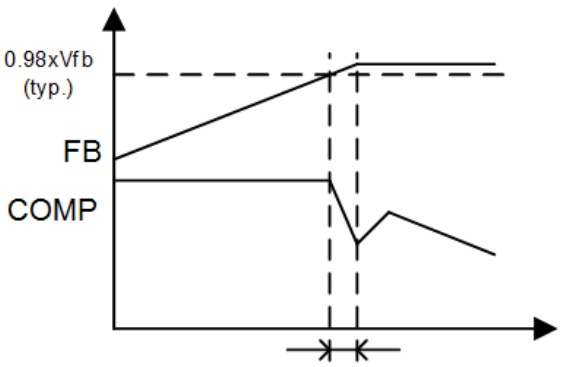


Fig. 15: Overshoot reduction function

(11) Under output voltage protection 1 (UVP1)

When the PFC output voltage decreases due to a dynamic load change and so on, the FA1B00N can suppress a rapid decrease on the PFC output voltage. This function is the Under output voltage protection (UVP).

If the FB pin voltage lowers to “FB pin threshold voltage when COMP pin pull up (0.94*V_{fb})”, the improvement of the load response function is operated, and the COMP pin is temporarily pulled up by the COMP pull up resistance inside IC. Then ON width of the OUT pin pulse gradually increases according to the COMP pin voltage, it suppresses a rapid decrease on the PFC output voltage (see Fig.16).

The FB pin voltage rises to above “FB pin threshold voltage when COMP pin pull up (0.94*V_{fb})” again, this function is canceled.

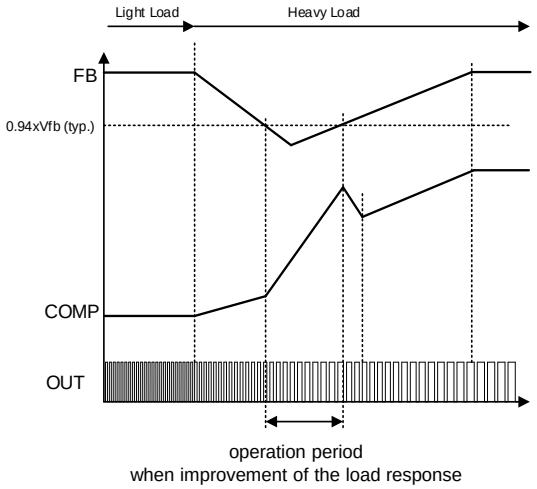


Fig. 16: Under output voltage protection operation

(12) Output circuit section

The output area has a push-pull circuit structure where the MOSFET can be driven directly.

The peak current in the output area will be sink 1 A and source 0.5 A at maximum.

10. Pin usage

The standard values in the following explanations are typical values unless otherwise specified.

(1) Pin No. 1 (FB pin)

[Function]

(i) Inputs a feedback signal for setting the output voltage
(ii) Detects FB pin short circuits.
(iii) Detects an output overvoltage state.
(iv) ON/OFF from external source

[Usage]

(i) Feedback signal input.

• Connection method

Connect the voltage-dividing section of the resistor circuit for setting the output voltage, as shown in Figure 17.

• Operation

The resistance voltage is divided for PFC output voltage Vout, and the voltage input to the FB pin is controlled so that it matches the internal reference voltage (2.5 V).

The FB pin is detected as open, so a pull-up current (Ipullup) flows into the FB pin. This current flows to GND over R2. Therefore, this current must be taken into consideration and resistors R1 and R2 must be set when setting the output voltage (Vout).

$$V_{out} = \left(\frac{VREF}{R2} - Ipullup\right) \times R1 + VREF$$

VREF : Reference voltage = 2.5 V
Ipullup : FB pin pull-up current = 2 uA

Connect capacitor C3 (from 100 pF to 0.01 µF) between the FB pin and GND to prevent malfunctions caused by noise.

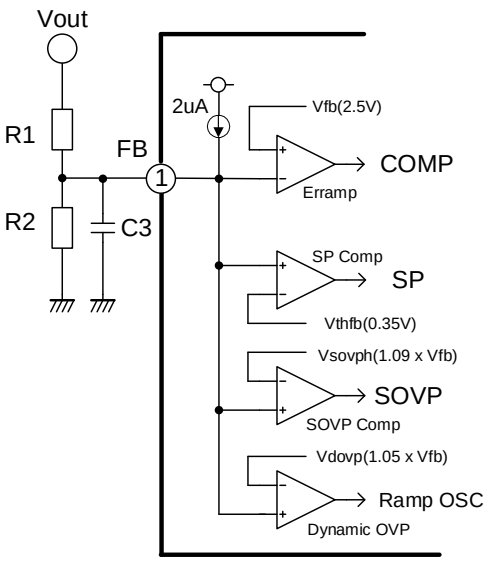


Fig. 17: FB pin circuit

(ii) FB pin short circuit detection

• Connection method

(i) The same as feedback signal input.

• Operation

When the input voltage of the FB pin is 0.35 V or less due to a short circuit or other failure in resistance voltage-dividing circuit R2, the output from the comparator (SP) is inverted and output from the IC is stopped.

(iii) Output overvoltage detection

• Connection method

(i) The same as feedback signal input.

• Operation

The normal FB pin voltage operates at nearly the same reference voltage (2.5 V) of the error amplifier. If the output voltage rises for some reason and the voltage of the FB pin reaches the reference voltage of the comparator (1.09 x *V*fb), the output from the comparator (OVP) will be inverted for that period of time, and the OUT pulse will be stopped. When the output voltage returns to a normal value (1.04 x *V*fb), the OUT pulse will be output again.

(iv) ON/OFF from external source

• Connection method

Connect a MOSFET or the like between FB and GND, as shown in Figure 18.

• Operation

The OUT output and internal circuit of the IC stop when the FB pin voltage is pulled down to Vthfb_l or lower. When the FB pin is used to turn the IC ON/OFF, the internal circuit is stopped, so the current consumption of the IC switches to the current when a switching stop signal is input (30 uA). This makes it possible to suppress the power consumption of the IC. However, the overshoot reduction function will not function if the VCC pin voltage does not fall below operation stop voltage *V*off and the IC is not reset first.

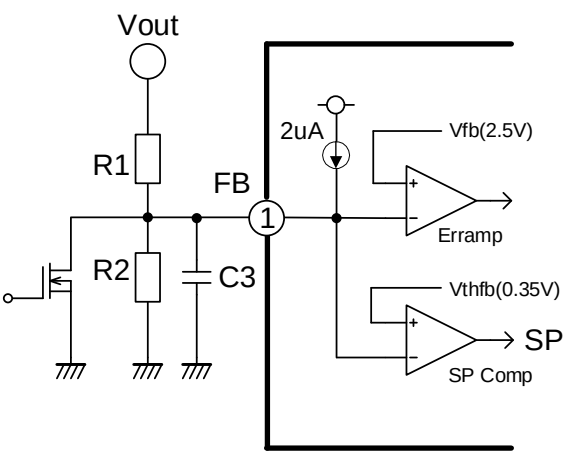


Fig. 18: ON/OFF using FB pin

(2) Pin No. 2 (COMP pin)

[Function]
(i) Phase compensation for built-in ERRAMP output
(ii) ON/OFF operation from external source

[Usage]
(i) Phase compensation for built-in ERRAMP output
• Connection method
Connect C and R between COMP and GND, as shown in Figure 19.
• Operation
If C and R are connected to the COMP pin, the frequency ripple component two times that of the AC line frequency shown in FB output, will not be shown.
(Reference)
Circuit example: C4 = 0.1 uF

C5 = 1 uF

R3 = 10 kΩ

The values above are merely examples for reference. Determine the actual values through careful verification on actual hardware.

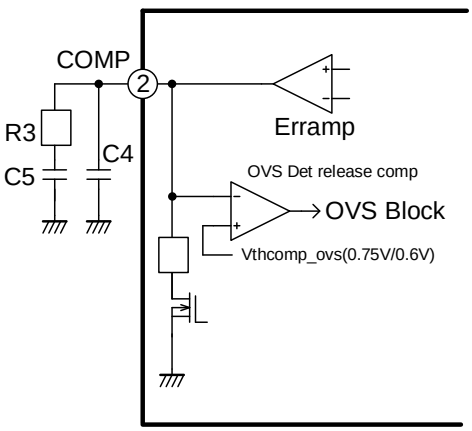


Fig. 19: COMP pin circuit

(ii) ON/OFF operation from external source
• Connection method
Connect a MOSFET or the like between COMP and GND, as shown in Figure 20.
• Operation
The OUT output of the IC stops when the COMP pin voltage is pulled down to *V*thcomp or lower. When this happens, the COMP pin current will be -30 uA, and the internal circuit will not stop.

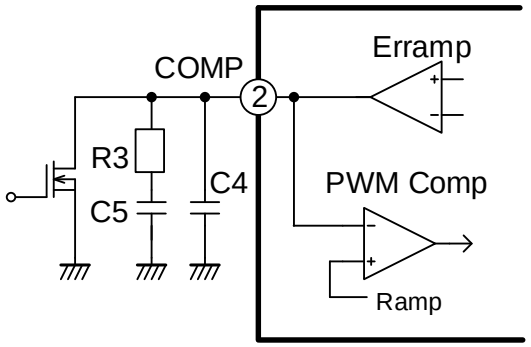


Fig. 20: ON/OFF using COMP pin

(3) Pin No. 3 (RT pin)

[Function]
(i) Setting of maximum on width
(ii) Setting of maximum oscillation frequency

[Usage]
(i) Setting of maximum on width
• Connection method
Connect R5 between RT and GND, as shown in Figure 21.
Refer to "7. Characteristic curves" for the resistance dependency of the maximum on width. The current sourced from the RT pin changes depending on the connected resistor. A 200 kΩ resistor will result in a small current of around 5.5 uA., so connect the resistor in parallel with a 1000 pF to 0.022 uF capacitor to the RT pin, as shown in the figure.

For a booster circuit, the input/output conditions and on period Ton during each switching cycle can be logically represented with the following equation.

$$T_{on} = \frac{2 \times L_p \times P_o}{{V_{ac}}^2 \times \eta}$$

Input voltage (Vrms): Vac
Inductor (H): Lp
Maximum output power (W): Po
Efficiency: η

Maximum on width *T*onmax must be set to at least the on width for the minimum input voltage time Vac (min) where the on width is at its maximum. Set the maximum on width according to the following equation.

$$T_{onmax} > \frac{2 \times L_p \times P_o}{{V_{ac(min)}}^2 \times \eta}$$

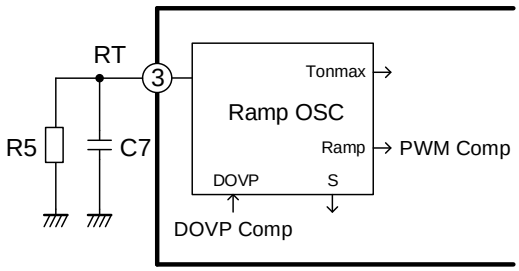


Fig. 21: RT pin circuit

(ii) Setting of maximum oscillation frequency
FA1B00N limits the rise in frequency to *F*max (kHz) during light loads, in order to improve efficiency during the light load. Maximum frequency *F*max is determined by the resistor connected between the RT pin and GND. However, the same resistor is used for setting both the maximum oscillation frequency and the maximum on width, so prioritize setting the maximum on width when adjusting.

(4) Pin No. 4 (CS pin)

[Function]
(i) Detects overcurrent from the MOSFET and turns OUT output OFF.

[Usage]
(i) Detects the current value of the MOSFET.
Threshold voltage *V*thcsh of the CS pin is 0.637 V (min). Set current detection resistor Rs so that the required current flows with regard to *V*thcsh.
If maximum output Po (W) and minimum input voltage Vac (min) are set,
the maximum value (ILP (max)) of the peak current of the inductor and MOSFET can be represented with the following equation.

$$I_{Lp(max)} = \frac{2 \times \sqrt{2} \times P_o}{\eta \times V_{ac(min)}}$$

Therefore, the value of Rs (Ω) can be determined as follows.

$$R_S < \frac{V_{thcsh}}{I_{Lp(max)}} = \frac{0.637}{I_{Lp(max)}}$$

• Connection method
Connect current detection resistor Rs between the MOSFET source terminal and GND. Input the MOSFET current-voltage conversion signal generated in this resistor.
• Operation
(i) If the CS pin voltage is larger than 0.65 V, the comparator output signal is inverted, and OUT output turns OFF.

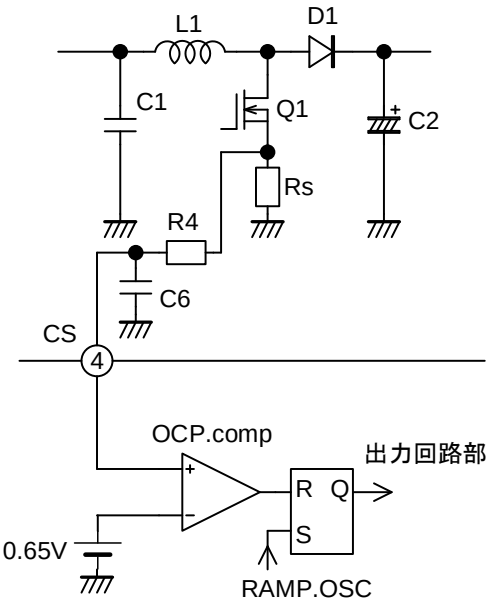


Fig. 22: CS pin circuit

[Supplementary note]
When the MOSFET turns on, a surge current flows into current detection resistor Rs due to the gate drive current of the MOSFET and the parasitic capacitance of the circuit being discharged. If this surge current is large, the input current waveform could be disrupted due to a malfunction. Additionally, depending on the size and timing of the surge current, an extremely short pulse may become mixed in with the turn-off portion of the OUT pulse from the IC. Therefore, this should normally be used with a CR filter connected, as shown in Figure 22. The cutoff frequency of this CR filter must be set sufficiently higher than the switching frequency, to prevent normal operation from being affected.
This cutoff frequency should be set to around 1 to 2 MHz.

$$\frac{1}{2 \times \pi \times C6 \times R4} \fallingdotseq 1\sim2[MHz]$$

(5) Pin No. 5 (ZCD pin)

[Function]
(i) Detects zero current.

[Usage]
The L1 auxiliary winding voltage is input to the ZCD pin to detect when the MOSFET turns on.
The current flowing into the ZCD pin is used within the rating of the IC, so this is normally used with resister R6 (for limiting current) inserted between the ZCD pin and auxiliary winding. (Fig. 23)

• Connection method
Connect R6 between the auxiliary winding and ZCD, as shown in Figure 23.
In order to ensure normal operation, the current flowing to the clamp circuit of the ZCD pin must be suppressed to 1.5 mA or lower, as shown in the recommended conditions. The following relational equation must therefore be satisfied.

$$R6 > \frac{-1.9 + \sqrt{2} \times V_{ac(max)} \times \frac{N_s}{N_p}}{1.5 \times 10^{-3}}$$

$$R6 > \frac{V_o \times \frac{N_s}{N_p} - 6.6}{1.5 \times 10^{-3}}$$

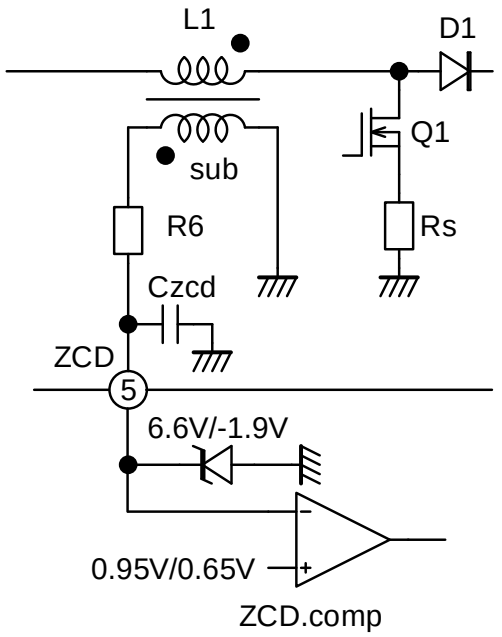
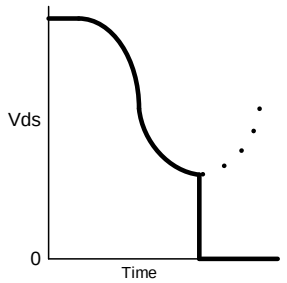
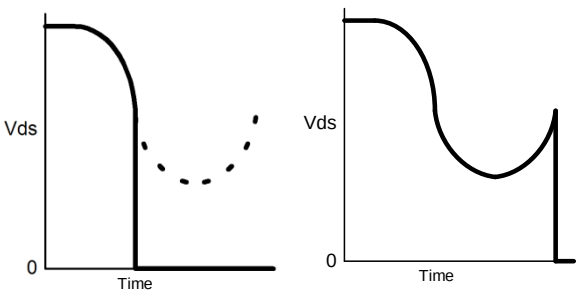


Fig. 23: ZCD pin circuit

• Turn-on timing adjustment
The MOSFET (Q1) turns on once the current in inductor L1 returns to zero. When this happens, Vds between the MOSFET drain and source begins to vibrate as it resonates with L1 and the parasitic capacitor component on the circuit, immediately prior to turning on. R6 and Czcd are adjusted so that the MOSFET turns on in the valley portion of this resonance, as shown in Figure 24. If R6 is several 10s of kΩ and adjustment cannot be performed with a resistor only, this can generally be adjusted by adding Czcd (to a normal value up to around several 10s of pF). Doing this can minimize switching loss following the MOSFET turning on, and can also minimize the surge current that occurs when it is turned on.



(When the values for R6 and Czcd are appropriate)



(When the values for R6 and Czcd are not appropriate)

Fig. 24: Turn on position adjustment

(6) Pin No. 6 (GND pin)

[Function]
The standard voltage for each part of the IC

(7) Pin No. 7 (OUT pin)

[Function]
Drives the MOSFET.

[Usage]
• Connection method
Connect to the gate pin of the MOSFET through a resistor. (Fig. 25)

• Operation
While the MOSFET is turned on, this switches to a high state and a voltage roughly the same as the VCC voltage is output.
While the MOSFET is turned off, this switches to a low state and a voltage of around 0 V is output.

• Supplementary note
Connect a gate resistor to limit the current of the OUT pin and prevent vibration of the gate pin voltage.
The output current rating for the IC is source 0.5 A and sink 1 A.
The connections shown in Figure 26 and Figure 27 will allow the gate drive current for MOSFET on and off to be set independently.

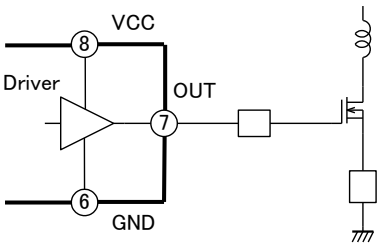


Fig. 25: OUT pin circuit (1)

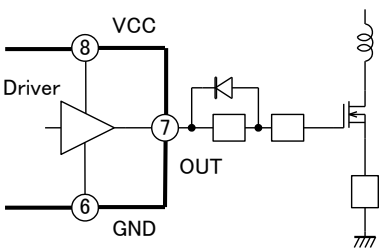


Fig. 26: OUT pin circuit (2)

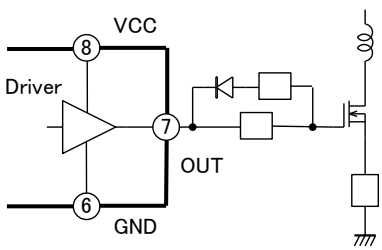


Fig. 27: OUT pin circuit (3)

(8) Pin No. 8 (VCC pin)

[Function]
(i) Provides IC power supply.

[Usage]
(i) Provides IC power supply.
• Connection method
Connect a starting resistor between the voltage line and VCC pin, after rectification.
This is generally connected after rectifying/smoothing the voltage of the auxiliary winding attached to the transformer. (Fig. 28)
Also connect an external DC power supply. (Fig. 29)

• Operation
When VCC voltage is provided from the auxiliary winding during startup, the current flowing from starting resistor R7 is charged by smoothening capacitor C8, and the IC starts once it rises to the ON threshold voltage of the under voltage lock out (UVLO). A current of at least the startup current of the IC (300 uA (max)) must be provided immediately prior to startup.
During steady operation, VCC is provided from the auxiliary winding of the inductor. As the power supply voltage rises from zero, it begins operating at 13 V. Once operation begins, as the power supply voltage drops, the UVLO causes it to stop operating at 9 V, and it discharges the COMP pin capacitor. The under voltage lock out (UVLO) operates, and the OUT pin switches to low and output is blocked while the IC is stopped.

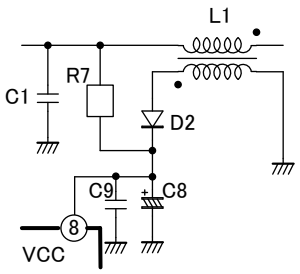


Fig. 28: VCC pin circuit (1)

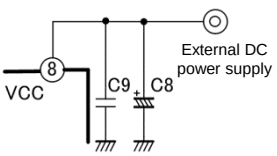


Fig. 29: VCC pin circuit (2)

[Supplementary note]
The under voltage lock out function is meant to prevent circuit malfunction when the power supply voltage drops. Starting resistor R7 must provide a current of at least the startup current of the IC (300 μA) immediately prior to startup, and the following equation must be satisfied.

$$R7 < \frac{\sqrt{2} \times V_{ac(min)} - V_{on(max)}}{300 \times 10^{-6}}$$

Von (max): Under voltage protection ON threshold voltage

This relational equation represents the minimum condition required to start the IC. On actual hardware, this will need to be determined after considering factors such as the startup time required for setting.

During steady operation, Vcc is supplied from the inductor auxiliary winding.
Following IC startup, however, there is a slight time delay until the auxiliary winding voltage rises sufficiently. It is necessary to decide the capacity of capacitor C8 connected to Vcc so that Vcc does not drop to the UVLO OFF threshold voltage during this time (Figure 30). This time delay differs depending on the circuit, and therefore a decision should be made by verifying at the actual device. Furthermore, it is recommended that ceramic capacitor C9 (approx. 0.1 uF) be mounted to eliminate switching noise.

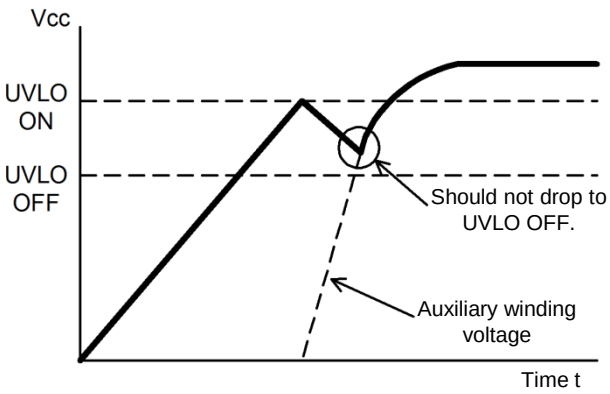


Fig. 30: VCC pin voltage at startup

• Startup time
When Vcc rises to the threshold voltage of 13 V with current determined by starting resistance, and the IC is activated, COMP voltage rises, and when it reaches 0.6 V, it is output by the OUT pin, and the IC starts up.
Startup time Tstart can be calculated with the following equation.

$$T_{start} = \frac{C8 \times V_{on}}{\frac{V_{ac(min)} \times \sqrt{2}}{R7} - I_{start}}$$

Istart: startup current

This startup time must actually be decided by measuring it during circuit operation.
The size of capacitor C8 connected to Vcc cannot normally be reduced very much, and therefore startup will take time if startup resistor R7 is large.
Startup time will be shorter if the size of startup resistor R7 is reduced, however, there will be an increase in starting resistance loss, and resultant drop in efficiency. To shorten startup time without the drop in efficiency, the startup circuit may be configured as shown in Fig. 31.

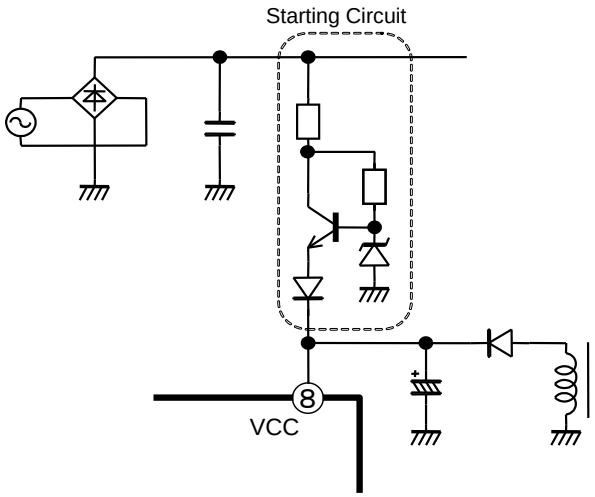


Fig. 31: Starting circuit

(9) pin negative voltage

The Vds voltage oscillation immediately before MOSFET turn-on may be transferred to the OUT pin through parasitic capacitance and so on, resulting in negative voltage being applied to the OUT pin. If this negative voltage is large, the parasitic element inside the IC will conduct, resulting in possible IC malfunction.
In cases where this negative voltage exceeds -0.3 V, connect a Schottky barrier diode between the OUT pin and GND, as shown in Figure 32. The negative voltage can be clamped with the Schottky barrier diode forward voltage.
In the same way, take care to prevent negative voltage being applied to other pins also.

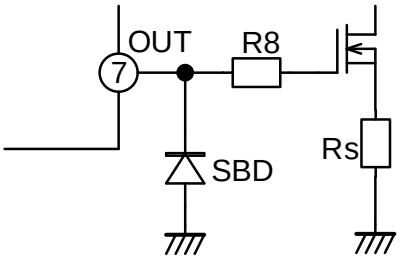


Fig. 32: Negative voltage prevention

(10) Inductor L1 design (auxiliary winding)

Auxiliary windings normally have two functions.
- Detecting the MOSFET ON timing at ZCD
- Supplying Vcc

It is necessary to decide the turn ratio with the main winding to be able to satisfy both of these conditions.

The auxiliary winding voltage changes constantly with respect to each AC input instantaneous value. This can be seen in Fig. 33.
All conditions are obtained based on this operation.

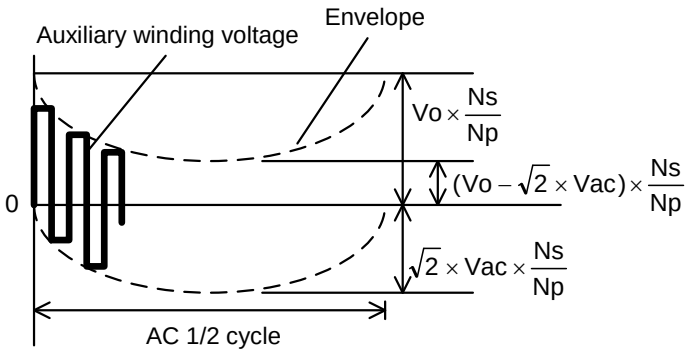
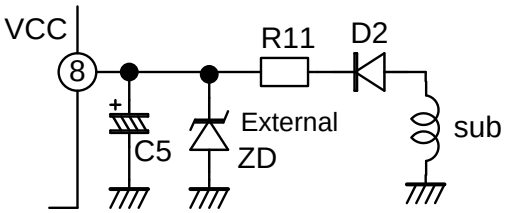


Fig. 33: Auxiliary winding voltage



If using external ZD

Fig. 34: VCC circuit (1)

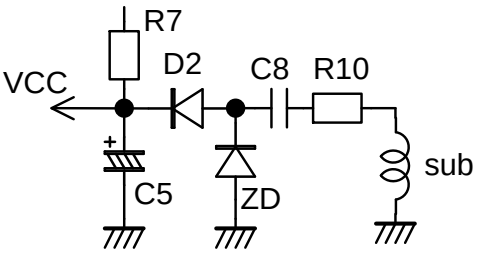


Fig. 35: VCC circuit (2)

ZCD threshold voltage

The ZCD comparator threshold voltage is 1.017 V (max.) at startup. This threshold voltage must be exceeded even when the auxiliary winding voltage is at its lowest, and therefore the following conditional expression must be satisfied.

$$N_s/N_p > \frac{1.017}{V_o - \sqrt{2} \times V_{ac(max)}}$$

Vcc supply

If Vcc is used in the 10 V to 24 V range from the recommended conditions, the following condition must be satisfied.

$$\frac{10}{V_o} < N_s/N_p < \frac{24}{V_o}$$

It is necessary to set the auxiliary winding to a turn ratio that is capable of satisfying both of these relational expressions.

If the PFC boost ratio (ratio of Vac to Vo) is small, it may not be possible to set the number of auxiliary winding turns so that they can both be satisfied.
If this is the case, use the following method.

a. Install one auxiliary winding for ZCD and one for Vcc.
b. Set by giving priority to ZCD. With this, there is a possibility that Vcc will exceed the recommended conditions, and therefore an external ZD should be used to limit the Vcc voltage. (Fig. 34)
In this case, resistor R11 is required for current limiting between the auxiliary winding and Vcc.

Furthermore, it may not be possible to supply stable Vcc when light loads are involved.
In such a case, improvement may be possible with a circuit connection such as shown in Fig. 35.
The optimum value for the C8 and R10 constants will differ depending on the circuit, and therefore the value should be decided during actual circuit operation.

11. Usage precautions

(1) Pattern design precautions

Main circuit MOSFETs, inductors, and diode switching operations are performed with large voltage and current. Consequently, as ICs and the signal wiring input to the ICs are mounted near main circuit parts, they may malfunction due to the noise produced.

Particular caution is required in cases such as the following. (This is a bad example.)

- ICs are mounted beneath main circuit parts such as inductors, or on the immediate reverse side of main circuit parts on double-sided PCBs. (Fig. 36)
- ICs are mounted right next to inductors, MOSFETs, or diodes. (Fig. 37)
- Signal wiring is run beneath inductors, or near MOSFETs or diodes. (Fig. 38)

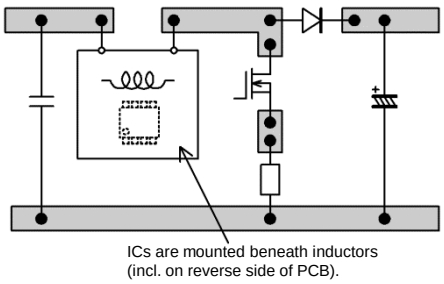


Fig. 36: Bad arrangement example (1)

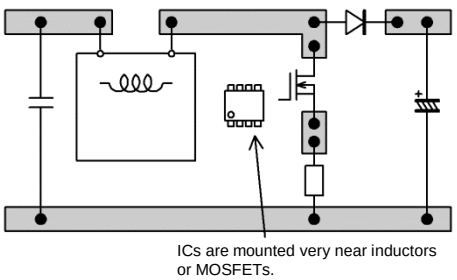


Fig. 37: Bad arrangement example (2)

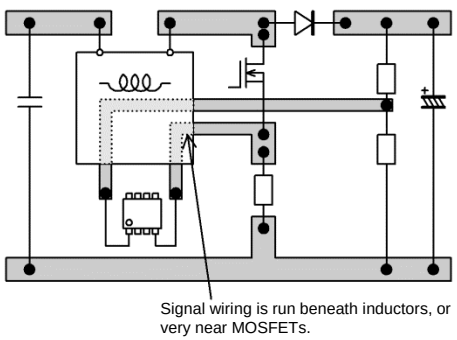


Fig. 38: Bad pattern example

(2) IC peripheral GND wiring example

(Caution)

This wiring example has been prepared for the purpose of helping users understand the thinking behind the routing of GND wiring.

Noise and associated malfunctions will vary with individual sets, and there is no guarantee that all sets will function normally using this wiring example (Fig. 39).

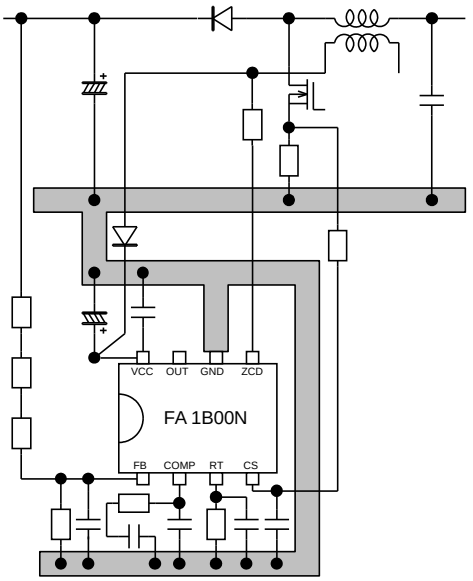


Fig. 39: Good GND wiring example

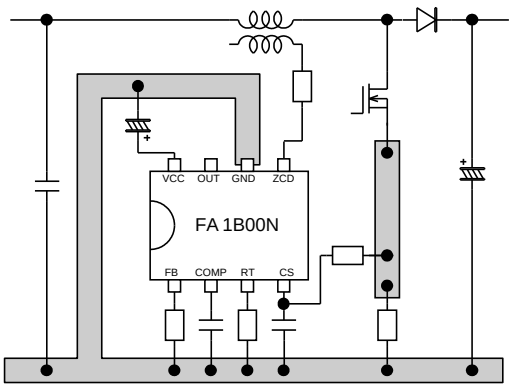


Fig. 40: Bad GND wiring example

12. Boost chopper PFC application circuit example

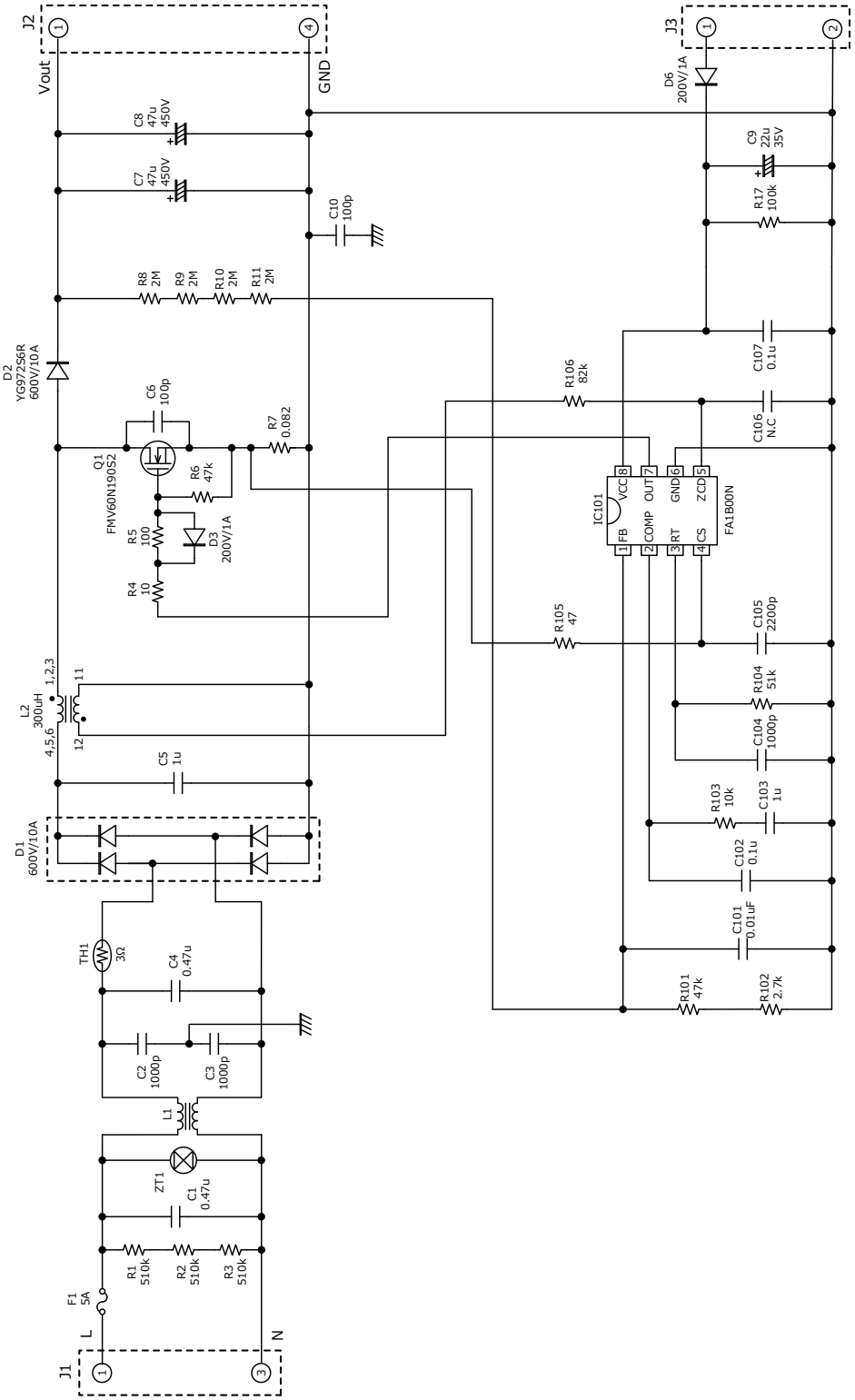


Fig. 41: Boost type PFC application circuit example

Caution) This application circuit example is reference material prepared for the purpose of describing a typical usage method for this IC, and does not guarantee operation or characteristics.

13. Usage precautions due to pin noise

The following defects will be a concern if each of the IC pins is subjected to noise. Use power supplies only after sufficiently ensuring that there will be no instability or malfunction due to noise.

13-1. A noise input within the absolute maximum ratings

condition	Pin	malfunction in fear	Input regulations	cautions in design
input noise (within absolute maximum ratings)	FB	switching may stop when noise is over Over voltage protection voltage	input signal is only for feedback voltage of output voltage	connect capacitor near terminal pin
		IC may become stanbay mode when noise is under short detection level (after standby mode cancellation become restart mode)		
		offset occurs in output voltage and output voltage rises or falls by a noise		
	COMP	on width may become not constant by load, output may change heavily by a noise	cancel noise	confirm sufficiently phase compensation constant
		switching may become when noise is over stop switching at OUT pin threshold voltage		
		switching may stop when noise is under stop switching at OUT pin threshold voltage		
	RT	on width may become not constant by load, output changes heavily by a noise	cancel noise	connect capacitor near terminal pin care the paturn of substrate
		restriction of maximum on time may not work when voltage is higher than pin voltage (on width may change when voltage is higher than pin voltage)		
		on width and restriction may change when voltage is lower than pin voltage		
	CS	switching may stop become when noise is over Over current protection threshold voltage	cancel noise	connect capacitor near IC
	ZCD	turn-on occurs unintentional timing, Mos/Diode heat and switching noise may becomes bigger by a noise	cancel noise	connect capacitor near pin
		It may not turn on when the time below turn-on threshold is less than delay time	Although Inductor and Mos capacitance is resonant, input voltage more than threshold over delay time	connect capacitor near pin
		it may become maximum frequency mode when noise frequency is faster than maximum frequency of setting	cancel noise	connect capacitor near pin
	GND	reference voltage changes, IC may not behave normally	cancel noise	ground wiring should be a wide wiring
	OUT	the output may fall not to be able to drive Mos normally when signals more than the ability of the driver are input	cancel noise	—
	VCC	IC may stop when noise under UVLO is input	don't input noise under UVLO when operating	connect capacitor near pin

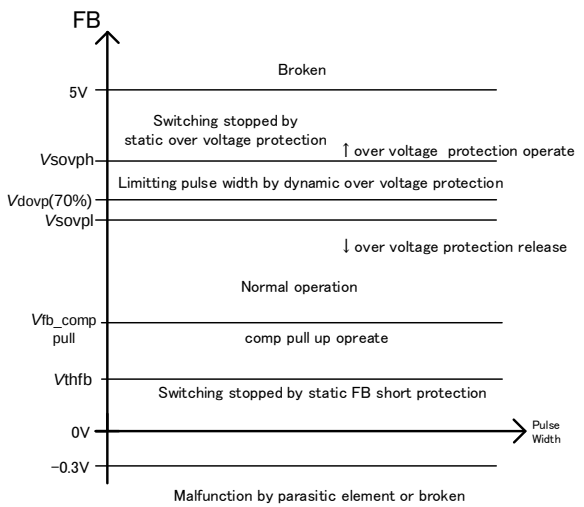
condition	Pin	malfunction in fear	Input regulations	cautions in design
input minus voltage (less than absolute maximum voltage)	FB	a parasitism element works, and the malfunction such as IC stop may occur	don't input minus voltage less than maximum absolute voltage	—
	COMP			
	RT			
	CS			
	ZCD			
	OUT	IC may be destroyed		—
	VCC	a parasitism element works, and the malfunction such as IC stop may occur		—
input plus voltage (more than absolute maximum voltage)	FB	IC may be destroyed	don't input plus voltage more than maximum absolute voltage	—
	COMP			
	RT			
	CS			
	ZCD			
	OUT	IC may be destroyed		
	VCC			

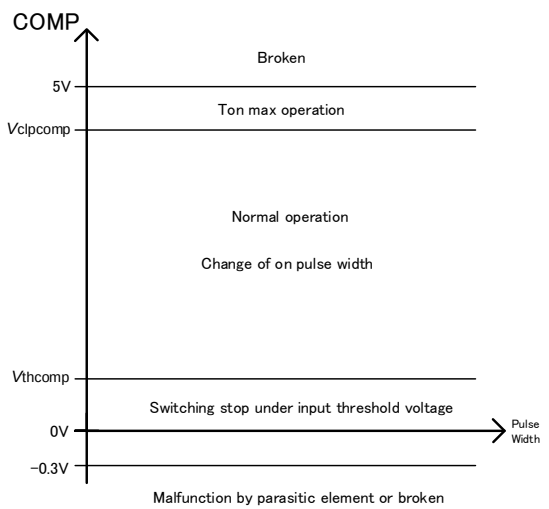
13-2. A noise input to GND pin

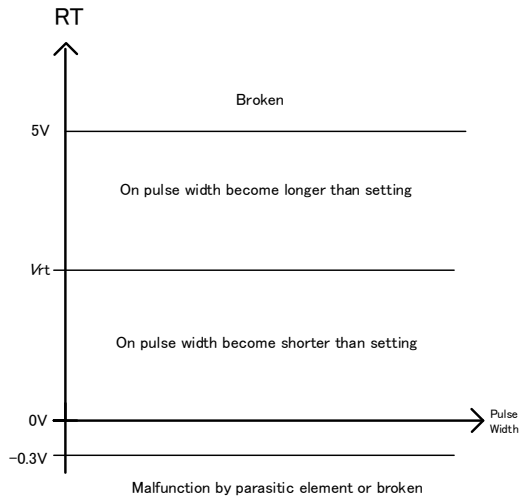
In the items mentioned above as 13-1, the GND level is assumed to be fixed 0V. If a noise is inputted to GND pin, it can be recognized as the equivalency inverted noise inputted to each pin on the basis of GND level.

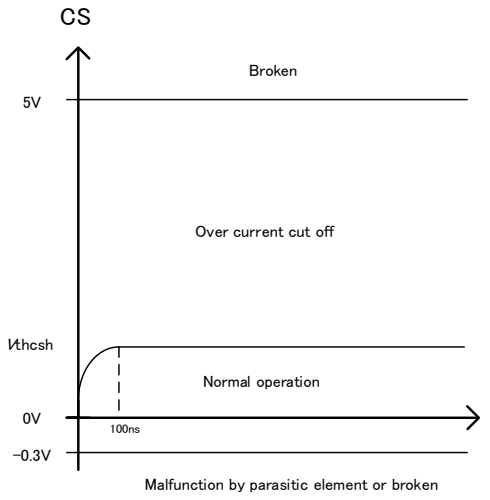
13-3. Pin conditions when the noise inputted to the pin

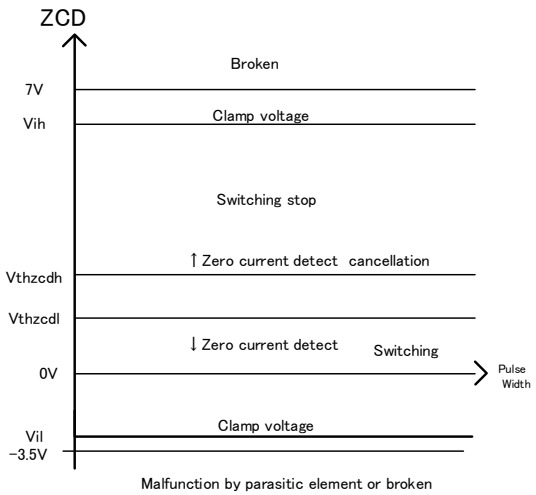
The characteristics in this section are those in conditions as follows unless otherwise specified.
T_j=25℃, V_{cc}=12V, V_{fb} = 2.4V, V_{comp}=4.2V, V_{cs}=0V, V_{zcd}=0V, R_{rt}=39kΩ, OUT pin open

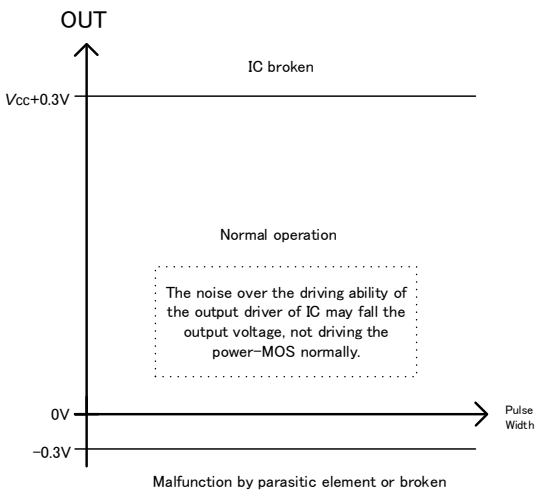


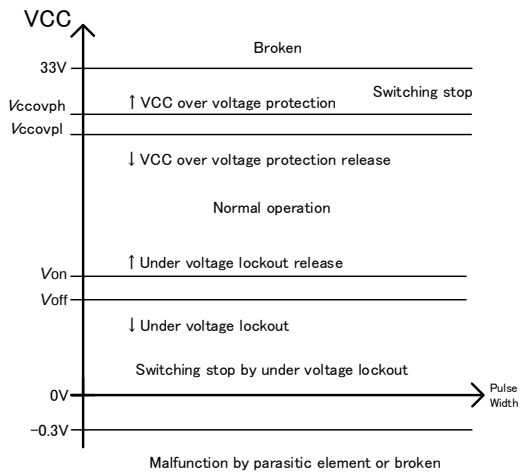












These figures explain the behavior of IC when the single-pulse noise is inputted to the terminal of IC, and no one to guarantee normal operation and the characteristic according to the value of the description. The tolerance to noise and behavior of IC when the noise is inputted to the terminal are different according to unevenness of IC, terminal conditions, other terminal conditions, ambient conditions, mounted conditions and so on. Moreover, the tolerance to continuous inputted noise is lower than the tolerance to single-pulse inputted noise. Please confirm neither the unusual operation nor the malfunction occurs by the noise in the use of this IC.

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