Green mode PWM IC
FA5680N / 81N

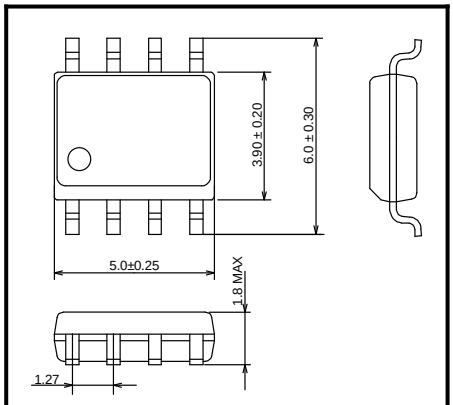
Datasheet

1. Overview

FA5680/81 is a current mode type switching power supply control IC possible to drive a power MOSFET. Although it is small 8-pin package, FA5680/81 integrates many functions and so is very suited for saving energy during light load and reducing number of external parts. Therefore, power supply of high cost performance can be built..

2. Features

- Frequency reduction function improves efficiency at middle load.
- The minimum switching frequency is set to 26k Hz to prevent audio noise.
- Intermittent operation (burst operation) at light load realizes low standby power.
- Low power consumption by built-in 750V startup circuit.
- Overload protection (FA5680: auto restart, FA5681 latch off) and overvoltage protection functions are built-in and so small number of components is required for protective operation.
- Since current detection is negative polarity, overload compensation for AC line voltage change can be made easily.
- Latch off function by external signal is incorporated. The function is suited for overtemperature protection (OTP) using external thermistor.
- Drive circuit for Power-MOSFET is built-in.
  Output current: 1.0 A (sink) / 0.5 A (source)
- Under voltage lockout for Vcc is built-in.
- Frequency diffusion function achives low EMI.
- Since dynamic self supply (DSS) function is provided, VCC voltage is supplied from VH pinpin to supply power when no voltage is supplied from auxiliary winding of transformer.



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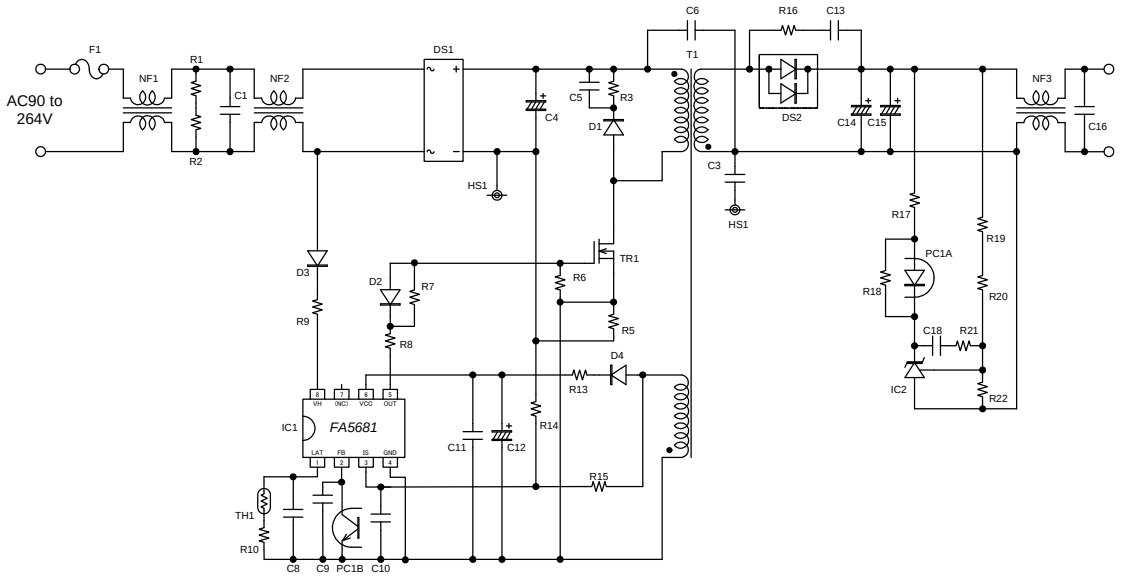
Function list by types

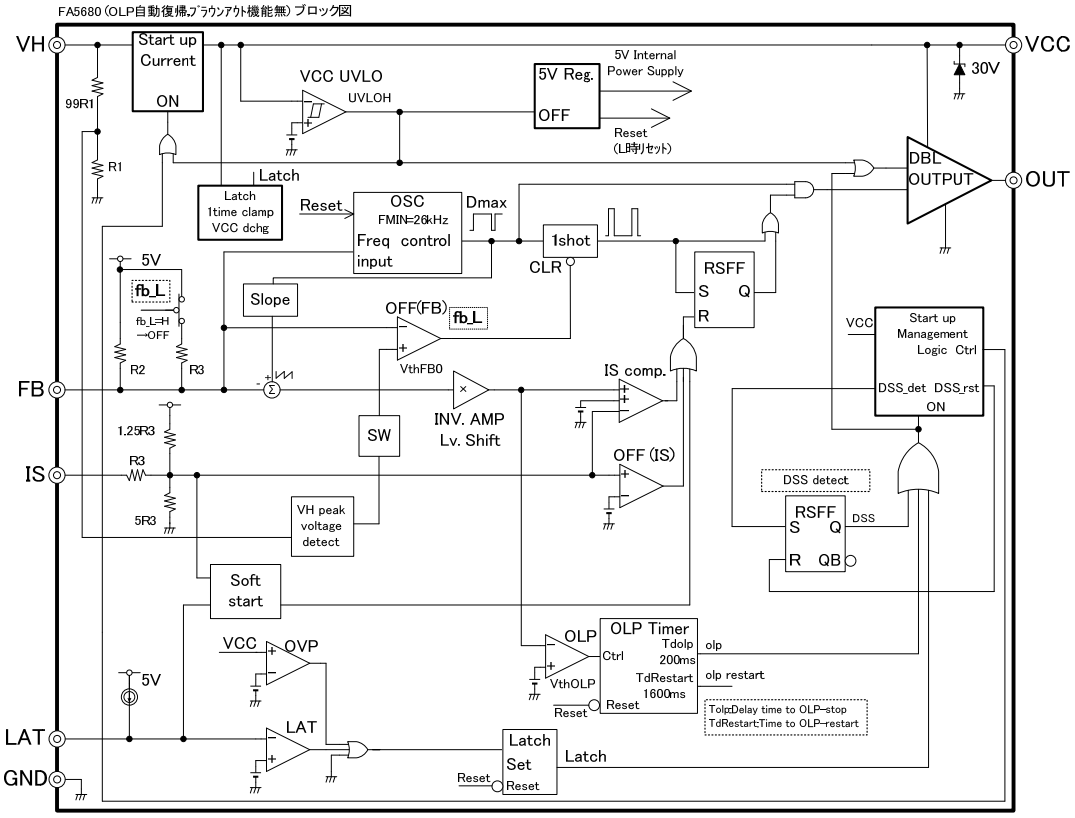
Type	Overload protection	External latch, over-voltage protection,	Brown out protection	Frequency
FA5680N	Automatic recovery	Latch	No	65kHz
FA5681N	Latch			

3. Application circuit example

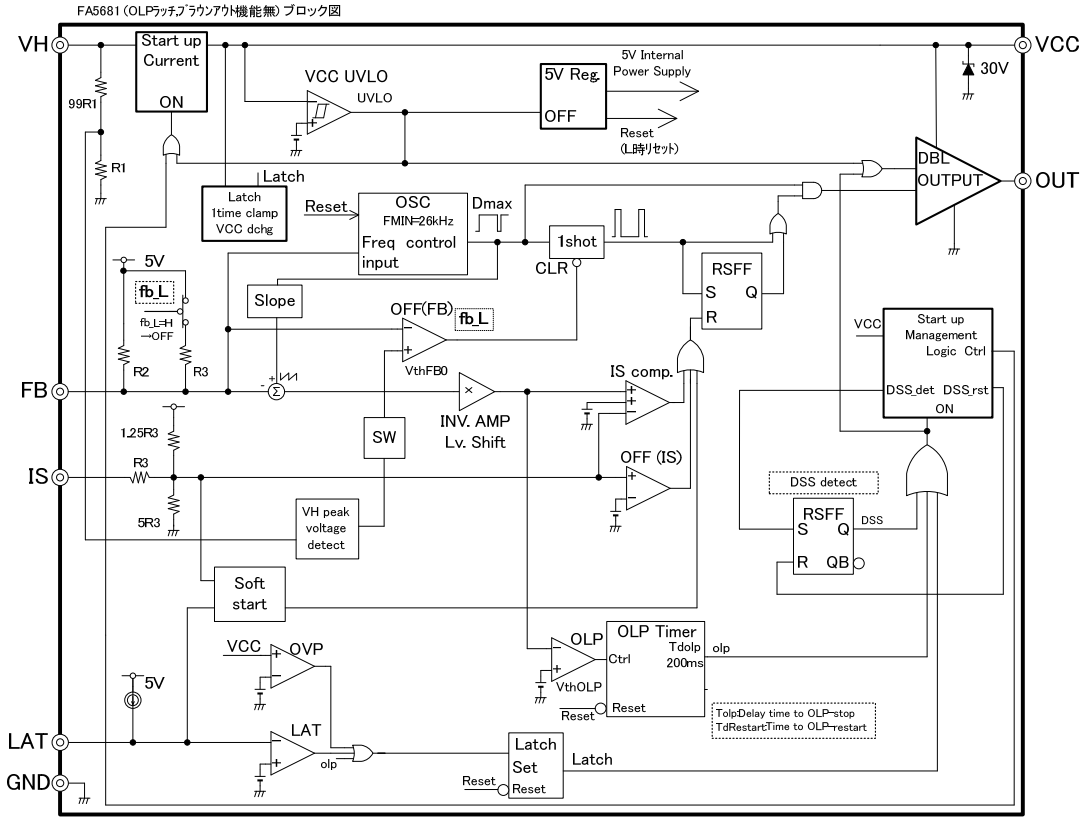


4. Block diagram

FA5680N (overload protection: auto recovery)

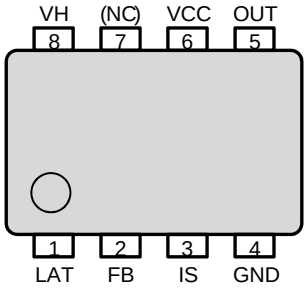


FA5681N (overload protection: latch off)



5. Functional description of pins

Pin No.	Pin name	Pin Function	Note
1	LAT	Overtemperature protection, external latch signal input	*1
2	FB	Feedback input	*1
3	IS	Current sense input	*1
4	GND	IC Ground	—
5	OUT	Output	—
6	VCC	Power supply	*1
7	(NC)	Not used	—
8	VH	High voltage input (750 V max.)	*2



Notes)
*1 Connect capacitor between terminal pin and GND.
*2 Connect diodes and resistor between VH and the AC lines.

6. Rating & characteristics

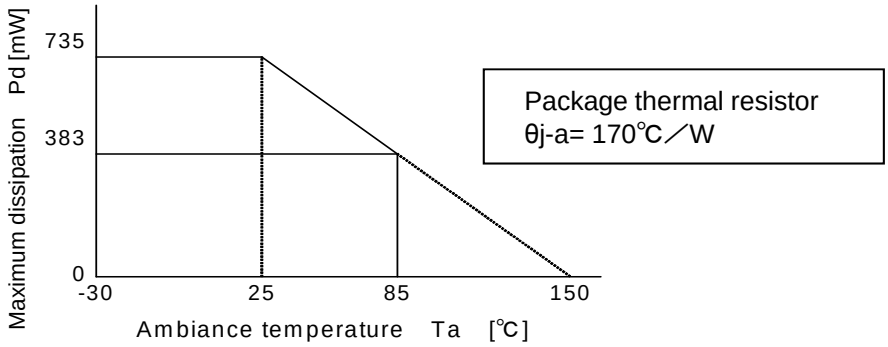
Stress exceeding absolute maximum ratings may malfunction or damage the device.
"-" shows source and "+" shows sink in current descriptions.

(1) Absolute maximum ratings

Item		Symbol	Value	Unit
LAT pin voltage		VLAT	-0.3 to 5.0	V
LAT pin current		ILAT	-100 to 100	uA
FB pin voltage		VFB	-0.3 to 5.0	V
FB pin current		IFB	-500 to 100	uA
IS pin voltage		VIS	-2.0 to 5.0	V
IS pin current		IIS	-100 to 100	uA
OUT pin voltage		VOUT	-0.3 to VCC+0.3	V
Peak current at OUT pin *1		IOH	-0.5	A
		IOL	+1.0 (The period that exceeds +1.0A is 100ns or less.)	A
VCC pin voltage		VVCC	-0.3 to 28	V
VCC pin current *1 (Tj=25℃)	at input plus voltage	IVCC	-30 to 15	mA
	at input minus voltage		-0.1 to 0	
VH pin voltage		VVH	-0.3 to 750	V
VH pin current *1 (Tj = 25° C)		IVH	-0.1 to 30	mA
Power dissipation (Tj = 25° C)		Pd	735	mW
Operating maximum junction temperature		Tj	-30 to +150	℃
Storage temperature		Tstg	-40 to +150	℃

Notes) *1 Never exceed power dissipation Pd.

※Maximum dissipation curve



(2) Recommended operating conditions

Item	symbol	MIN	TYP	MAX	Unit
Supply voltage (After IC start up)	VCC	10	18	24	V
VH pin voltage	VVH	100	—	650	V(DC)
VH pin resistance	RVH	2	—	15	kΩ
LAT pin capacitor	CLAT	0.22	1.0	2.2	uF
VCC pin capacitor	CVCC	10	33	100	uF
Operating ambiance temperature	Ta	-30	—	85	℃

Notes）

※ If switching operation is performed by power supply from the VH pin (DSS operation), IC power loss and VCC hold voltage vary depending on operating conditions (operating frequency, Qg of MOSFET and ambient temperature). If MOSFET is driven while DSS is operating, select VH pin resistor while considering IC power loss and VCC voltage.

※ Recommended value is conditions for guaranteeing that the product operates normally.
If it is used out of this condition, there is possibility of have a negative influence on operation and reliability.

※ Please use it after confirming operation enough with your products when you use it.

(3) DC electrical characteristics

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input values (not AC input values).

Tj=25℃,VCC=18V(After IC started up),VH=120V,VFB=2.5V,VIS=0V,CLAT=0.22uF,no load,

Notes）
(1) The item which indicated “*1” are not 100% tested in production but guaranteed by design.
(2) No guaranteed value exists for the column of “—“.
(3) “-” shows source current and “+” shows sink current in current output characteristics

(3)-1. Over temperature protection and external latch-off section(LAT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Source current of LAT pin	ILAT	LAT=1.15V,FB=0V	-85	-70	-55	uA
External latch-off Threshold voltage level	VthLAT	VLAT=Decreasing	1.00	1.05	1.10	V
LAT pin resistance at latch	RLAT	VthLAT / -Ilat	12	15	18	kΩ
Latch-off delay timer *1	TdLAT	VLAT=VthLAT	50	65	80	us

(3)-2. Soft-start section (LAT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LAT pin voltage of output minimum ON pulse at OUT pin	Vss1	*2-1	1.9	2.1	2.3	V
LAT pin hold voltage at latch or auto restart mode	Vss2	*2-1	2.3	2.5	2.7	V
Start soft-start LAT pin voltage *1	Vss	*2-1	1.8	2.0	2.2	V
Finish soft-start LAT pin voltage	Vss3	*2-1	1.5	1.6	1.7	V
After soft-start LAT pin voltage	VssL	*2-1	1.5	1.6	1.7	V
	VssH		1.9	2.1	2.3	V

*2-1：At the time of Start or Re-start

(3)-3. Switching oscillator section (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
(Center) oscillation frequency	Fosc	VFB=2V	60	65	70	kHz
Voltage stability	Fdv	VCC=11 to 24V, VFB=2V	-2	—	+2	%
Temperature stability *1	Fdt	Tj=-30 to 150℃, VFB=2V	-5	—	+5	%
Frequency modulation width *1	Fm	VFB=2V	±5	±7.0	±9.0	%
Frequency modulation period *1	Tfm	VFB=2V	7.0	8.0	9.0	ms
FB pin voltage at light load mode	Vfbm	VLAT=1.8V *3-1 VFB=Decreasing	1.65	1.80	1.95	V
FB pin voltage at minimum frequency	Vfmin	VLAT=1.8V *3-1 VFB=Decreasing	1.35	1.50	1.65	V
Oscillation frequency reduction ratio	Kf	⊿f/⊿VFB, VLAT=1.8V *3-1 ⊿VFB=Vfbm-Vfmin	105	125	145	kHz/V
Minimum oscillation frequency	Fmin	VLAT=1.8V ,VFB=0.5V *3-1	23.5	26.0	28.5	kHz

*3-1 After IC starts, the voltage at LAT pin voltage rises to VSS1.

(3)-4. Pulse width modulator section (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum duty cycle	Dmax	VFB=4.5V	75	85	95	%
Minimum duty cycle	Dmin	VFB=0V	—	—	0	%
FB pin threshold voltage for stop switching *4-1	VthFB0L	VFB=Decreasing, DUTY=0%, VH<VthVH	0.90	1.05	1.20	V
	VthFB0H	VFB=Decreasing, DUTY=0%, VH>VthVH	0.75	0.90	1.05	V
FB pin source current	Ifb0	VFB=0V,VLAT=1.8V	-270	-220	-170	uA
	Ifb1	VFB=1.65V,VLAT=1.8V	-220	-165	-110	uA
Minimum ON pulse width	Tmin	start(restart)/over load	180	280	380	ns

*4-1：There is a possibility that VH pin voltage does not fall to VthSETVH when the input voltage is high in the condition of full-wave connection. In that case, please note that “FB pin threshold voltage for stop switching” doesn't change even if VthVH is exceeded. Especially, please use “FB pin threshold voltage for stop switching” switch function after confirming the voltage level of the VH pin voltage in all input voltage ranges in the world-wide input specification.

(3)-5. Over load protection and auto-restart circuit section (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Over load detection threshold voltage *1	VthOLP	VFB=Increasing	3.2	4.0	4.8	V
Over load detection Delay time (FA5680: automatic reset)	TdOLP	VFB=VthOLP	60	70	80	ms
Over load protection operating time (FA5680: automatic reset)	TdRestart	VFB=VthOLP	1300	1530	1760	ms
Over load stop delay time (FA5681: latch stop)	TdOLP	VFB=VthOLP	170	200	230	ms

(3)-6. Current sense section (IS pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage gain	AvIS	VFB=2V to 1.5V ⊿VFB/⊿VIS	-4.6	-3.8	-3.0	V/V
Maximum threshold voltage	VthIS1	VFB= VthOLP	-0.525	-0.500	-0.475	V
Input bias current	IIS	VIS=0V,VFB=0V	-50	-40	-30	uA
Delay to output *1	TpdIS	IS input:0V to -1.0V (pulse signal)	50	100	200	ns

(3)-7. Output circuit section (OUT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low output voltage	VOL	IOL=+100mA,VFB=0V	0.4	0.8	1.6	V
High output voltage	VOH	IOH=-100mA,,VFB=2V	14.5	16	18	V
Rise time *1	tr	VCC=24V,VFB=3V, CL=1nF	30	60	100	ns
Fall time *1	tf	VCC=24V,VFB=3V, CL=1nF	20	40	70	ns

(3)-8. VCC circuit section (VCC pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
ON threshold voltage	VCCon	VCC=Increasing	16	18	20	V
OFF threshold voltage	VCCoff	VCC=Decreasing	7.5	8.0	8.5	V
Hysteresis width	Vhys	VCCon-VCCoff	8.5	10	11.5	V
VCC over-voltage protection threshold voltage(OVP)	Vthovp	VCC=Increasing	25	26	27	V
OVP delay time *1	TdOVP	VCC=Vthovp	50	65	80	us
VCC voltage at latch	VCCLHH	VH=120V,VFB=2V 1time clamp	13	14.5	16	V
	VCCLH	VH=120V,VFB=2V Upper level	12	13	14	V
	VCCLL	VH=120V,VFB=2V Lower level	11	12	13	V
VCC clamp voltage at OLP mode	VCCOLPH	Upper level	14	15	16	V
	VCCOLPL	Lower level	12	13	14	V
VCC clamp voltage at operating by Start-Up Circuit	VCCDSSH	Upper level	11.5	12.5	13.5	V
	VCCDSSL	Lower level	9.5	10.5	11.5	V

(3)-9. Power supply current (VCC pin)

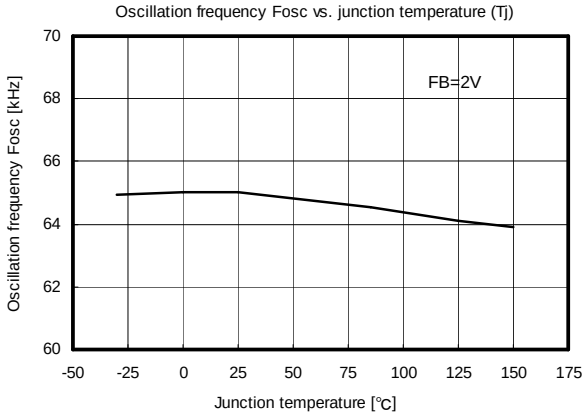
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating-state supply current	ICCop1	Duty=Dmax,VFB=2V, OUT=no load	0.90	1.35	1.60	mA
	ICCop2	Duty=0%,VFB=0V OUT=no load	0.85	1.30	1.50	mA
supply current at OLP	ICColp	VH=0V,VFB=0V, VCC=14.5V	0.6	0.9	1.1	mA
Latch mode supply current	ICClat	VH=0V,VFB=0V, VCC=11V	0.6	0.8	1.1	mA

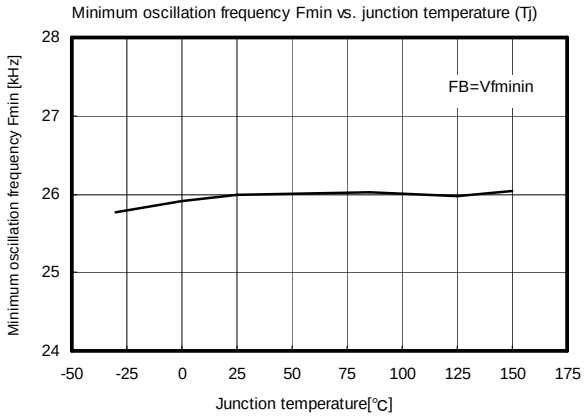
(3)-10. High-voltage input Section (VH pin、VCC pin)

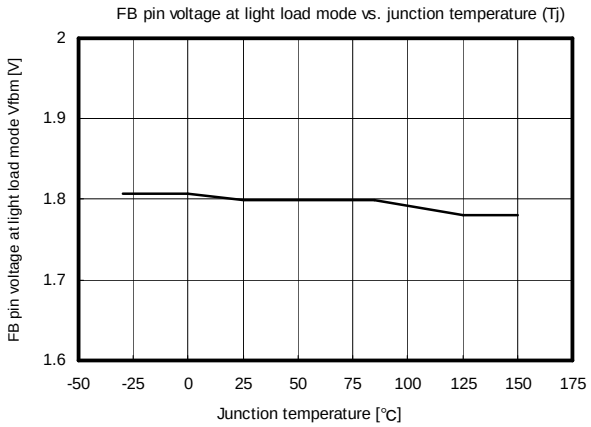
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input current of VH pin	IHrun	VH=450V,VFB=0V	10	15	20	uA
	IHstb	VH=120V, VCC=0V,VFB=0V	3.5	6.5	9.5	mA
		VH=120V,VCC=2 to 8V, VFB=0V	11	17	23	
		VH=120V,VCC=11V, VFB=0V	6	12	18	
		VH=120V,VCC=16V, VFB=0V	3.5	8	14	
Charge current for VCC pin	Ipre1	VCC=16V, VH=120V,VFB=0V	-14	-8	-3.5	mA
	Ipre2	VCC=11V, VH=120V VFB=0V, ラッチ時	-18	-12	-6	mA
VH peak detect voltage at changing FB voltage for stop switching	VthVH	VH decreasing, VthFB0L⇔VthFB0H	190	210	235	V
VH set voltage changing FB voltage for stop switching	VthSETVH	VH decreasing	70	80	90	V

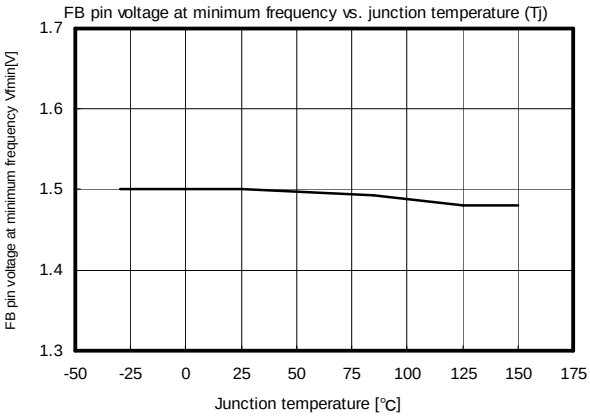
7. Characteristic curve

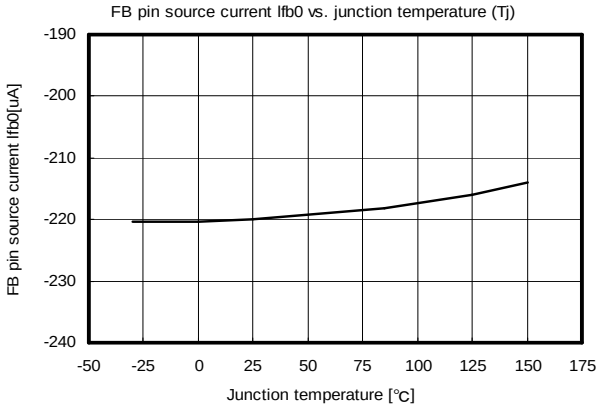
The characteristics in this section are under described conditions as follows unless otherwise specified.
Tj=25℃, VCC=18V(IC起動後), VH=120V,VFB=2.5V, VIS=0V,CLAT=0.01uF,
Notes）
（1）“-” shows source current and “+” shows sink in current regulations of the current.
（2）The data listed here show the typical characteristics of an IC, and does not guarantee the characteristic.



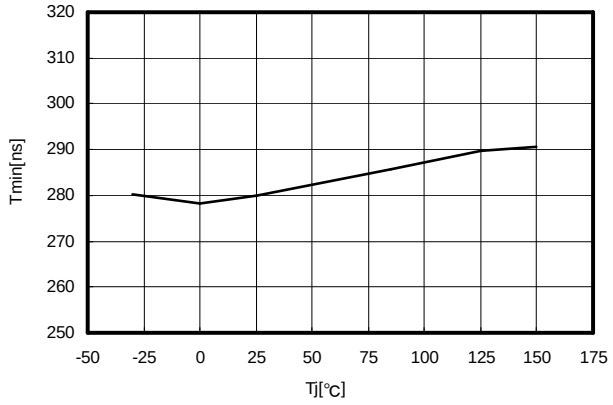




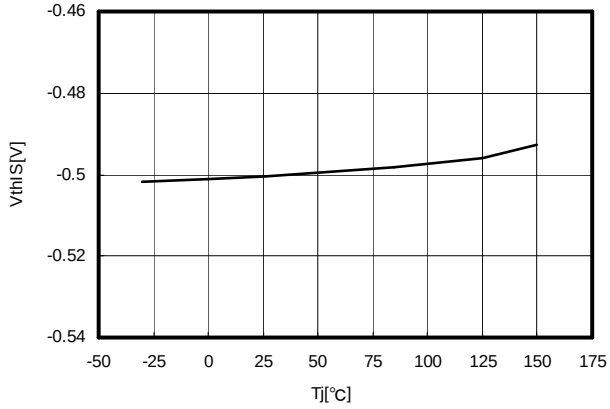




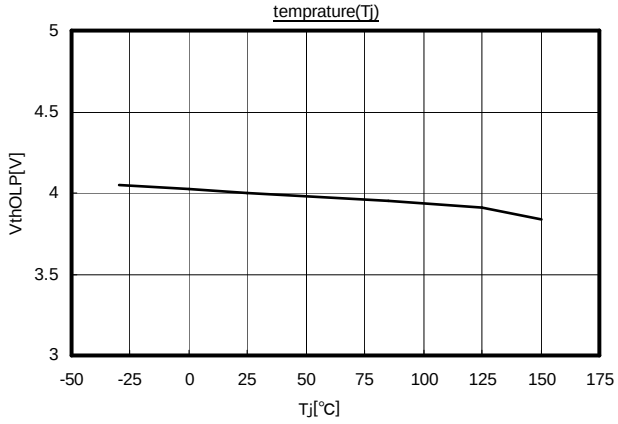
Minimum on pulse width(Tmin) vs Junction temprature(Tj)



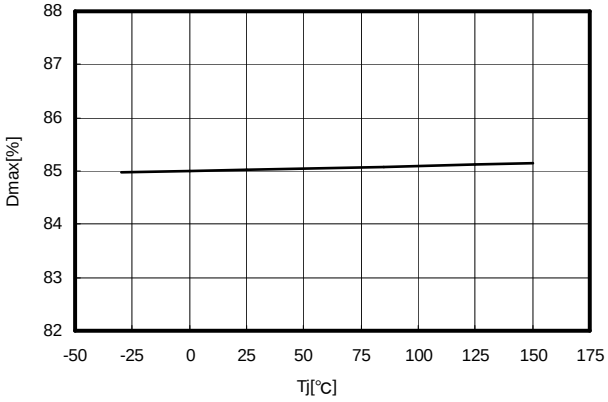
Maximum threshold voltage(VthIS) vs Junction temprature(Tj)



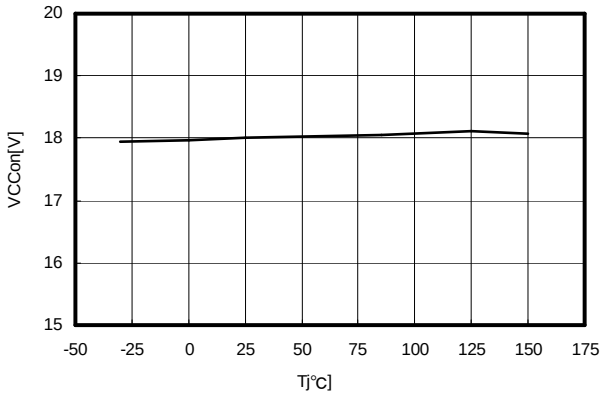
Over load detection threshold voltage(VthOLP) vs Junction temprature(Tj)



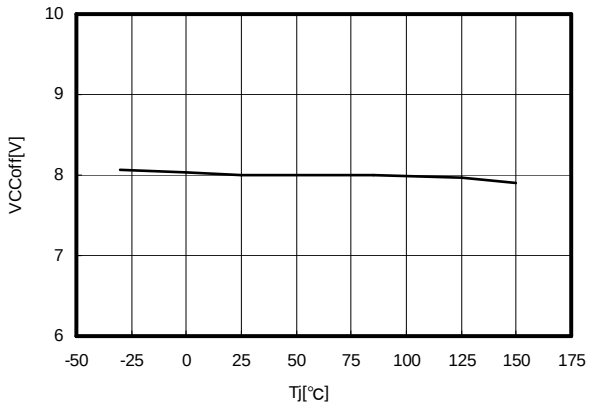
Maximum duty cycle(Dmax) vs Junction temprature(Tj)



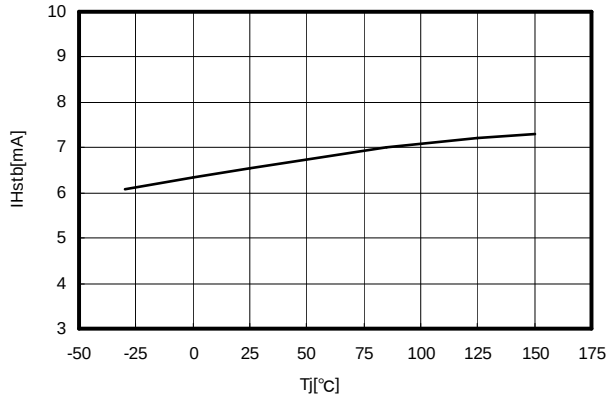
Start-up threshold voltage(VCCon) vs Junction temprature(Tj)



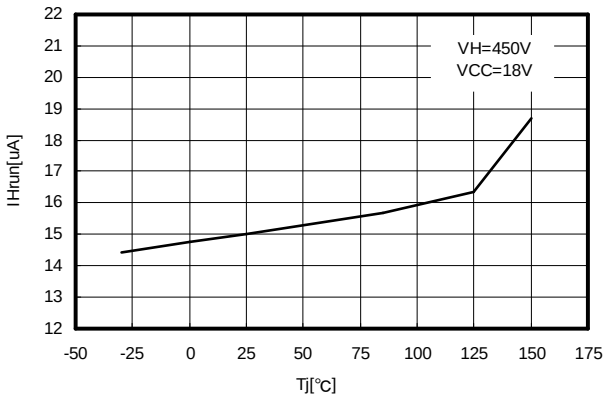
Shutdown threshold voltage(VCCoff) vs Junction temprature(Tj)



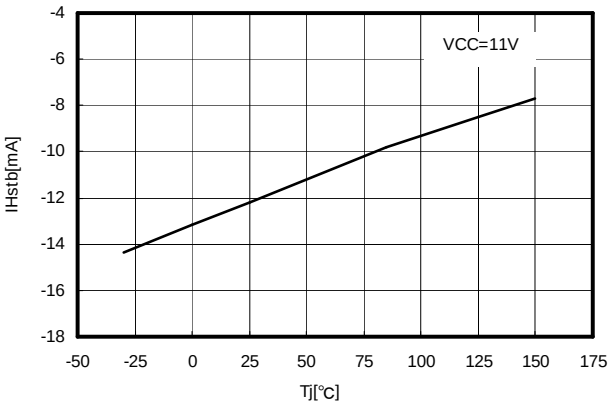
Input current of VH pin(IHstb) vs Junction temprature(Tj)



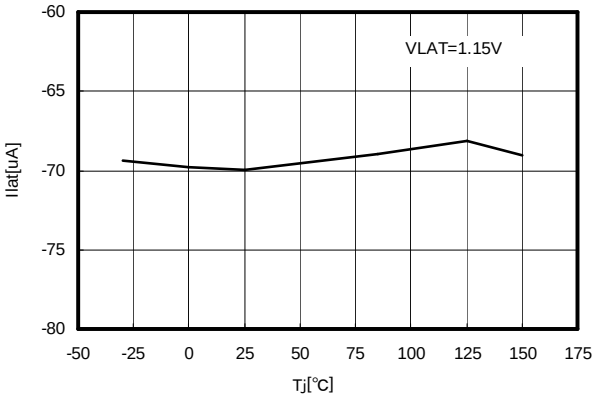
Input current of VH pin(IHrun) vs Junction temprature(Tj)



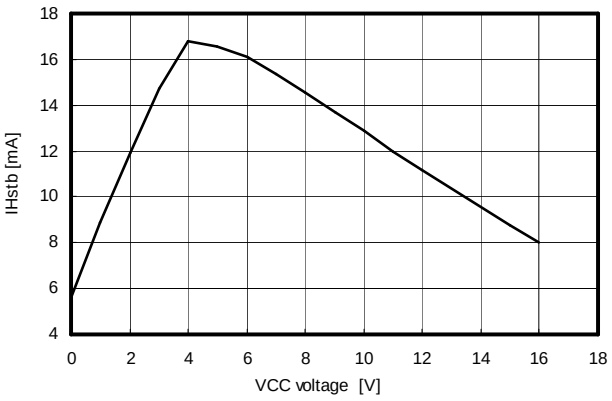
Charge current for VCC pin(Ipre2) vs Junction temprature(Tj)



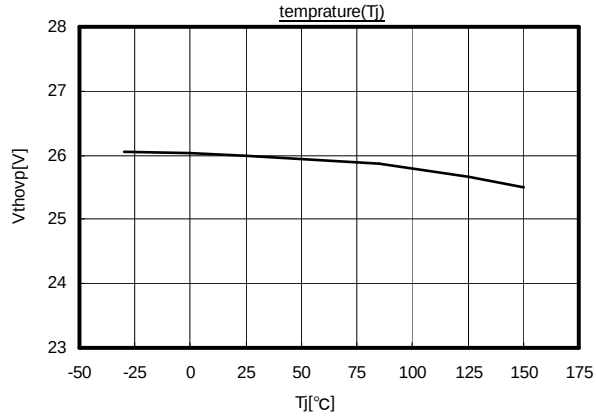
Source current of LAT pin(Ilat) vs Junction temprature(Tj)



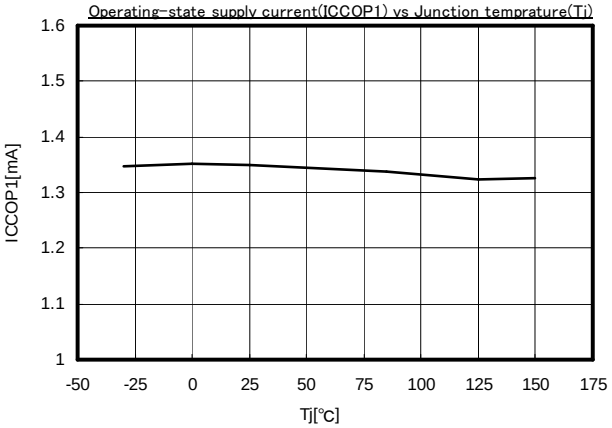
Input current of VH pin(IHstb) vs VCC pin voltage



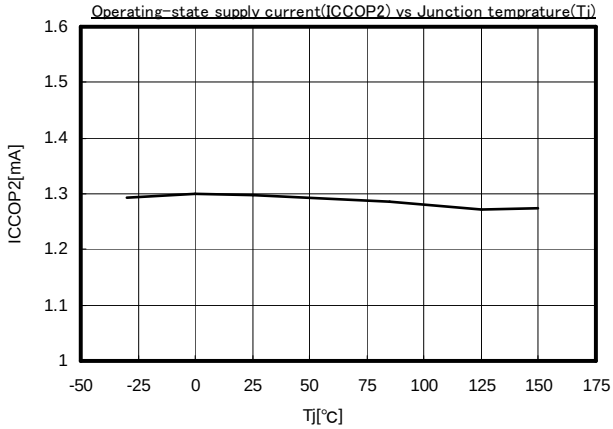
VCC over-voltage protection threshold voltage(Vthovp) vs Junction temprature(Tj)



Operating-state supply current(ICCOP1) vs Junction temprature(Ti)



Operating-state supply current(ICCOP2) vs Junction temprature(Ti)



8. Description of each circuit （The values in the following description are typical values unless otherwise specified.）

(1)Startup circuit

FA5680/81 incorporates startup circuit of absolute maximum rating of 750 V. The connection method is shown in Figs. 1 to 3. When AC line voltage is applied, the capacitor C2 connected to the VCC pin is charged by current supplied from the startup circuit to the VCC pin and voltage rises. Subsequently, when Vcc voltage exceeds the ON threshold voltage VCCon (Vcc = 18 V typ.) , the IC starts operation.

When the IC starts operation, the startup circuit is cut off and the VH pin current is narrowed down to tens of uA.

Resistor RVH is connected to the VH pin in series to prevent damage by surge voltage in the AC line and disperse IC power during DSS operation (See Page 21 for DSS operation) and overload protection operation.

Fig. 1 shows the most typical connection method in which the VH pin is connected in half-wave rectification waveform of AC input voltage. Start time in this method is the longest within the three methods.

In Fig. 2, the VH pin is connected in full-wave rectification waveform of AC input voltage. In this method, the start time is reduced to about half that of the half-wave rectification in Fig. 1.

In Fig. 3, the VH pin is connected after AC input voltage is rectified and smoothed. Start time in this method is the shortest within the three methods. In this method, however, even after the IC stops in the latch mode and the AC input voltage is cut off, the voltage charged in C1 is applied to the VH pin. Therefore, it takes time to reset the latch mode. Be careful because generally it takes several minutes till the latch mode is reset after AC input is cut off.

In states of DSS operation, overload stop and latch stop (OVP operation and external latch by the LAT pin), the startup circuit is on/off controlled and the VCC voltage is kept within the range of VCCLH: 13 V (typ.)/VCCLL: 12 V/ (typ.), VCCOLPH: 15 V (typ.)/VCCOLPL: 13V (typ.) or VCCDSSH: 12.5 V (typ.)/VCCDSSL: 10.5V (typ.) to maintain operation of the IC by the VH pin. Therefore, if input voltage is high (especially VH pin connected to rectified voltage as Fig.3), voltage applied to the VH pin becomes high and power consumption of the IC becomes large. To avoid this phenomenon, it is necessary to select start resistor RVH of proper value.

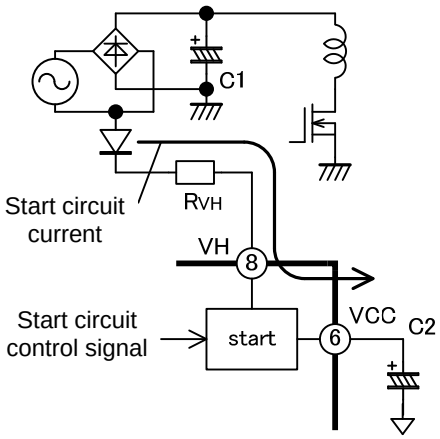


Fig. 1 Startup circuit 1 (Half wave)

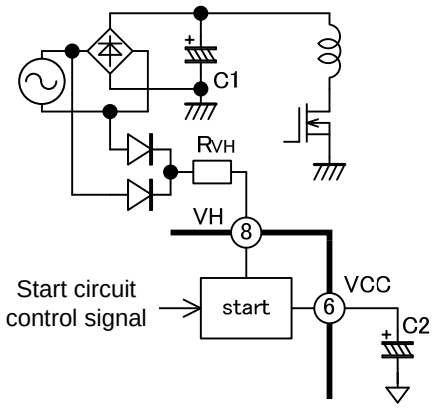


Fig. 2 Startup circuit 2 (Full wave)

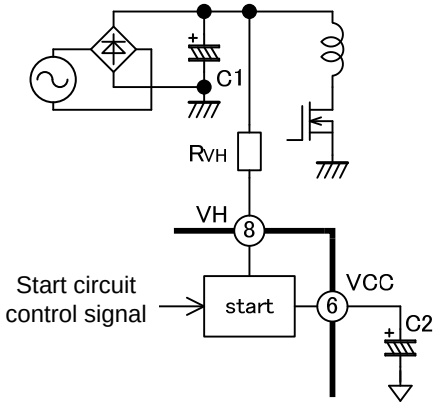


Fig. 3 Startup circuit (Rectification)

(2) Oscillator

The oscillator decides switching frequency. Switching frequency in the normal operation mode is set to 65 kHz (Fosc) within the IC.

This IC is provided with the function for automatically decreasing switching frequency during middle load to reduce power-supply loss in the standby state.

Frequency during middle load decreases almost linearly to the minimum frequency (Fmin) in proportion to the FB pin voltage (Fig. 4). This minimum frequency is set to 26 kHz (typ.).
If the load become further lighter and the FB pin voltage decreases to the pulse stop FB threshold voltage VthFB0L: 1.05 V (typ.) or VthFB0H: 0.9 V (typ.) or lower, intermittent operation (burst operation) is started.

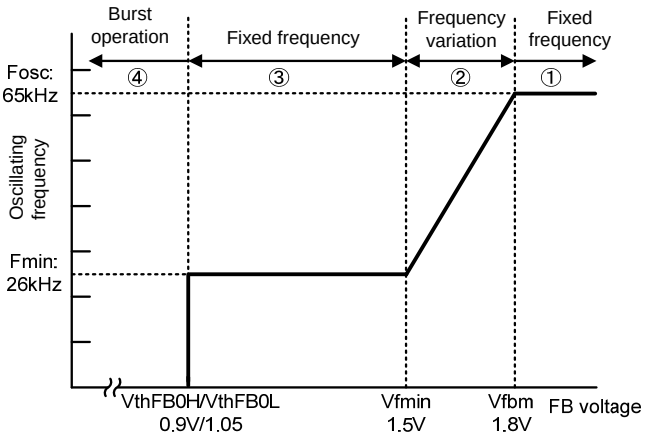
This pulse stop FB threshold voltage (point where burst operation is started) is changed according to input voltage. Input voltage is detected by VH pin. When the VH pin voltage exceeds the peak detection VH voltage VthVH: 210 V (typ.) then drops the set VH voltage VthSETVH: 80 V (typ.) , pulse stop FB threshold voltage is changed to VthFB0H for high line voltage. .
Therefore, if DC voltage is applied to VH pin, operation is performed at the VthFB0L level regardless of input voltage because no set signal is input.
In addition, note that if full-wave rectification is applied to VH pin, the VH pin voltage may not drop the set VH voltage VthSETVH: 80 V (typ.) and the pulse stop FB threshold FB voltage may not be changed.

Oscillation frequency is set to 26 kHz (typ.) during intermittent operation.

The oscillator generates the pulse signal for maximum duty cycle, and the ramp signal for slope compensation, in addition to the trigger signal for switching frequency.

(3) Frequency diffusion (spectrum diffusion)

FA5680/81 is provided with frequency modulation (Fm) of ±7.0% (typ.) for the switching frequency Fosc: 65 kHz. This function can disperse noise energy of switching compared with fixed frequency and reduce conductive EMI. Although effect of conductive EMI reduction depends on filter parts mounted on the power-supply board, effective use of this function can reduce number of filter parts and component values.
This function always provides the frequency modulation of ±7.0% for the operating frequency also in the frequency reduction area and the 26 kHz operating area during intermittent operation. Therefore, this function can also reduce conductive EMI of light load.



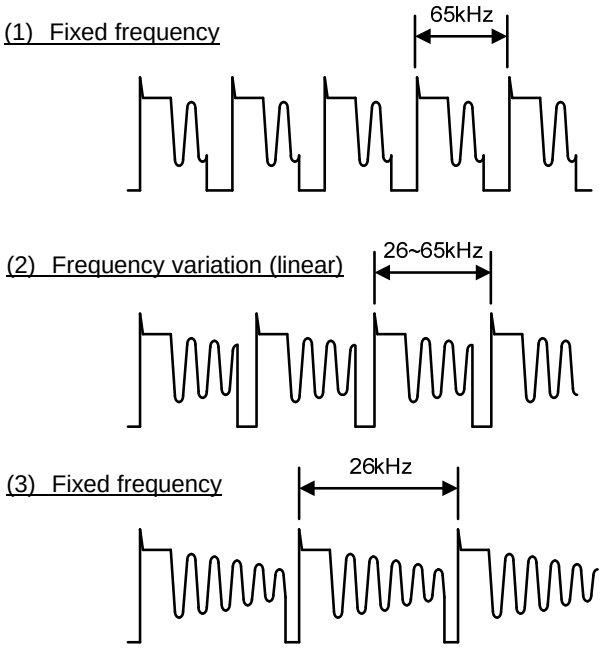


Fig. 4 Oscillating frequency

(4) Current comparator and PWM circuit

FA5680/81 performs current mode control. The basic operation circuit block is shown in Fig. 5 and the timing chart is shown in Fig. 6.
Current detection voltage of the IS pin is negative polarity. GND of IC is connected between current detection resistor Rs and MOSFET. (See Fig. 5.)

Trigger signal of switching frequency, which is output from the oscillator, passes through the one-shot (1 shot) circuit and is input into PWM (F.F.) as set signal. Subsequently PWM output and also OUT pin voltage are in the high state. On the other hand, the current comparator (IS comp.) monitors current of MOSFET and if the threshold voltage is reached, reset signal is output. PWM (F.F.) output becomes low when the reset signal is input, and the OUT pin voltage also becomes low.
Therefore, ON pulse width of the OUT pin is controlled by threshold voltage of the current comparator (IS comp.). The threshold voltage of this IS comp. is changed by the feedback signal to control output.

The FB pin voltage is level-shifted by the inverting amplifier and input into the current comparator (IS comp.) as threshold voltage as shown in Fig. 5. In addition, the reference voltage of –0.5 V is input within the IC to specify the maximum input threshold voltage VthIS1 (overcurrent limit threshold) of the IS pin.

For the threshold voltage of the IS pin, priority is given to higher voltage between the inverting amplifier output and the maximum threshold voltage.
The maximum input threshold voltage VthIS1 restricts the maximum current of MOSFET. If the FB pin voltage rises due to overload, the inverting amplifier output becomes lower than VthIS1.Therefore, the threshold voltage of the IS pin is restricted to VthIS1.

Pulse is output from the oscillator to decide the maximum duty cycle of OUT pulse. The maximum duty cycle is set to Dmax; 85% (typ.) by using this pulse.

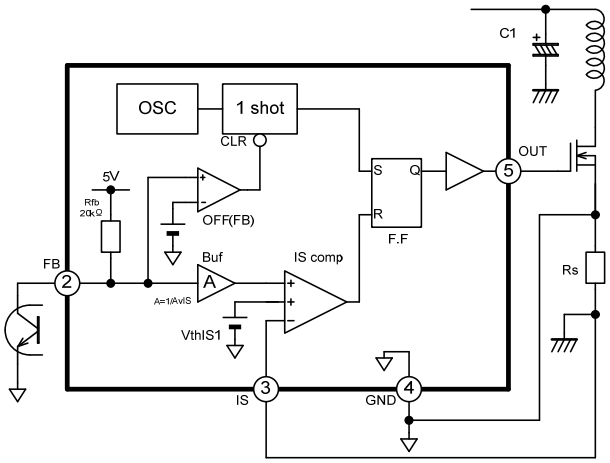


Fig. 5 Basic operation circuit block of current mode

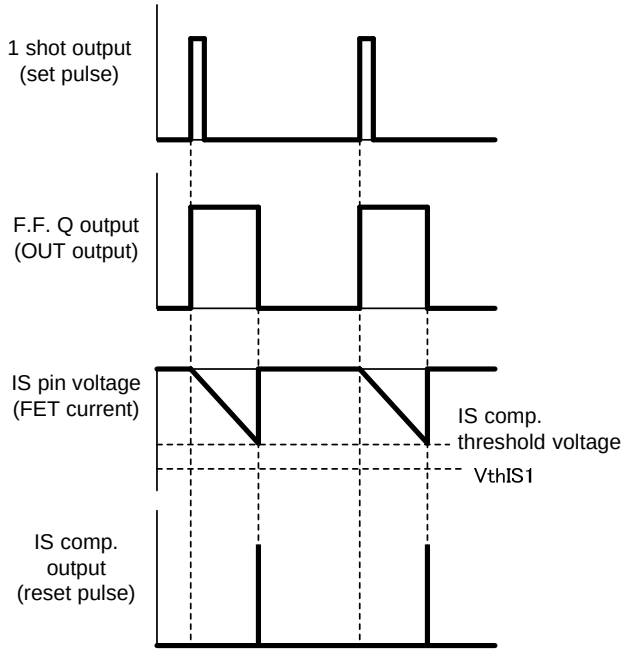


Fig. 6 Basic operation timing chart of current mode

(5) One-shot circuit (minimum ON width)

When MOSFET turns on, surge current is generated due to discharge for main circuit capacity and gate drive current. If this surge current reaches the threshold voltage of the IS pin, the current comparator output may be inverted and normal pulse may not be generated from the OUT pin.

To avoid this phenomenon, the minimum ON width for the OUT pin output is provided in the 1 shot circuit within the IC.

The minimum ON width of the OUT pin output operates as follows. When trigger signal of switching frequency is input from the oscillator, pulse signal of fixed width is output as set signal of PWM (F.F).

Priority is given to the set signal among the PWM input signals. Therefore, while the set signal is input from the 1 shot circuit, the PWM (F.F.) output is not inverted even if reset signal is input from the current comparator (IS comp.). (See Fig. 5.)

Resultantly, for a certain period (Tmin: 280 ns) just after OUT pin goes high pin, IS pin input becomes invalid and no response is made to the surge current at turn on. (See Fig. 7.)

IS pin noise filter may not be required because of this minimum ON width function.

In addition, a dedicated comparator is built-in to have no output pulse in complete no-load state. Output of this comparator is inverted if the FB pin voltage becomes VthFB0: 400 mV (typ.) or less. Then, no set pulse is output from the 1 shot circuit. Resultantly, no set signal is input to PWM (F.F.) and output is kept low. (See Fig. 5.)

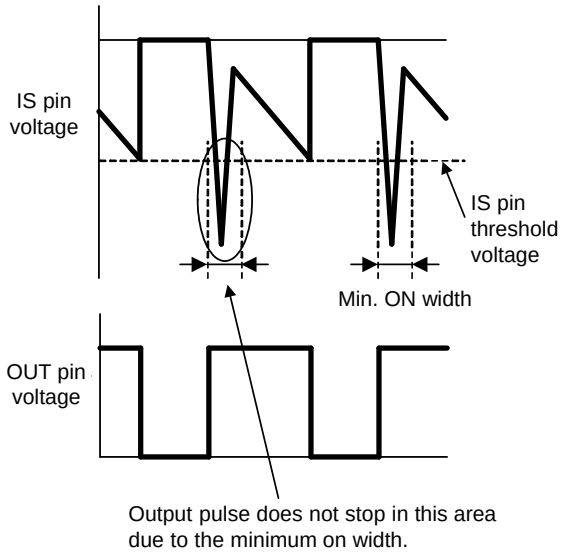


Fig. 7 Minimum ON width

(6) Overload protection circuit

(6)-1 Latch mode (FA5681)

FA5681 incorporates overload protection function of latch method. The overload protection circuit detects overload by FB pin voltage, and switching is stopped if overload state continues for the specified period TdOLP: 200 ms (typ.). The circuit block is shown in Fig. 8 and the timing chart of protective operation is shown in Fig. 9.

If output current increases in overload state, MOSFET current increases and current is limited by the maximum threshold voltage VthIS1: −0.5 V (typ.) of the IS pin. Subsequently, secondary output voltage cannot be kept and output voltage drops. If FB voltage rises to the overload detection threshold voltage VthOLP: 4.0 V (typ.), overload is detected. At the same time when overload is detected, the built-in OLP timer starts counting delay time. If overload continues for over the overload delay time TdOLP: 200 ms (typ.), switching pulse is stopped and the latch mode is started.

However, if overload is shorter than the overload delay time, switching pulse is not stopped (the latch mode is not started). During latch stop, the startup circuit is on/off controlled and VCC voltage is kept within the range of VCCLH: 13 V (typ.)/VCCLL: 12 V (typ.).

The latch mode can be released by reducing the VCC pin voltage to the OFF threshold voltage VCCoff: 8.0 V (typ.) or less.

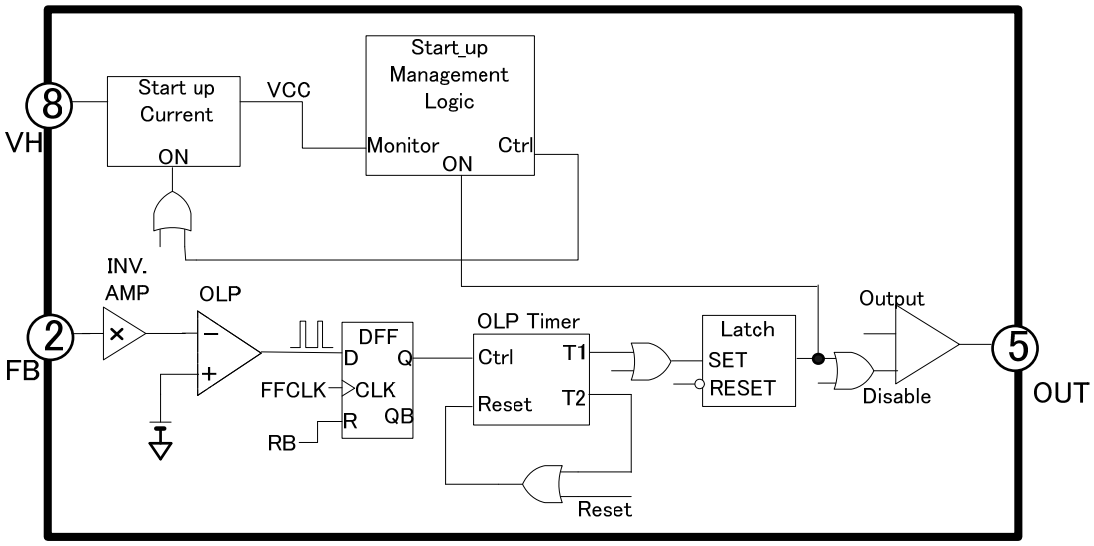


Fig. 8 Overload protection circuit (latch)

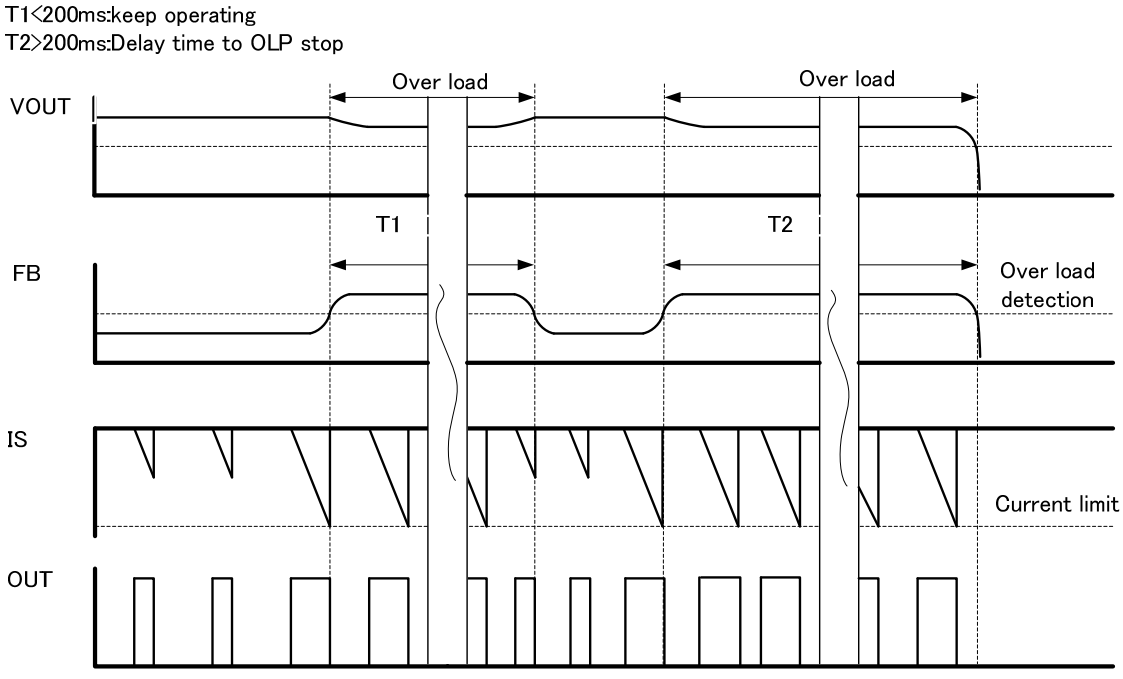


Fig. 9 Overload protection timing chart (latch)

(6)-2 Auto restart mode (FA5680)

FA5680 incorporates overload protection function of auto restart. The circuit block is shown in Fig. 10 and the timing chart of protective operation is shown in Fig. 11.

If output current increases in overload state, MOSFET current increases and current is limited by the maximum threshold voltage VthIS1: −0.5 V (typ.) of the IS pin. Subsequently, secondary output voltage cannot be kept and output voltage drops. If FB voltage rises to the overload detection threshold voltage VthOLP: 4.0 V (typ.), overload is detected. At the same time when overload is detected, the built-in OLP timer starts counting delay time. If overload continues for over the overload delay time TdOLP: 70 ms (typ.), switching pulse is stopped. When the overload stop period TdRestart:1600 ms (typ.) is passed after switching pulse is stopped, switching is restarted automatically. Stop and restart are repeated until the overload state is removed.

While switching pulse is stopped, the startup circuit is on/off controlled and VCC voltage is kept within the range of VCCOLPH: 15 V (typ.)/VCCOLPL: 13 V (typ.).

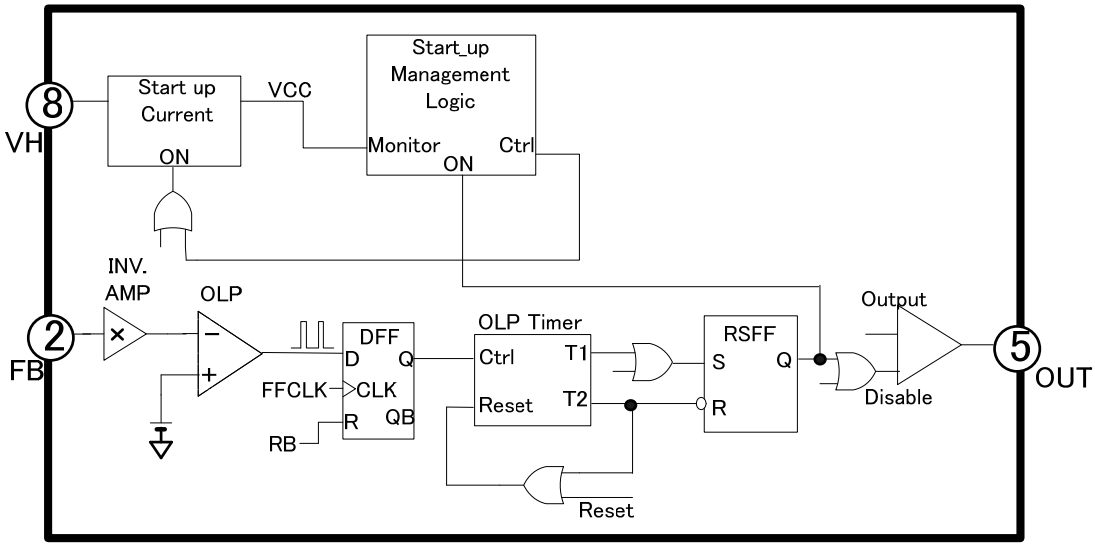


Fig. 10 Overload protection circuit (auto restart)

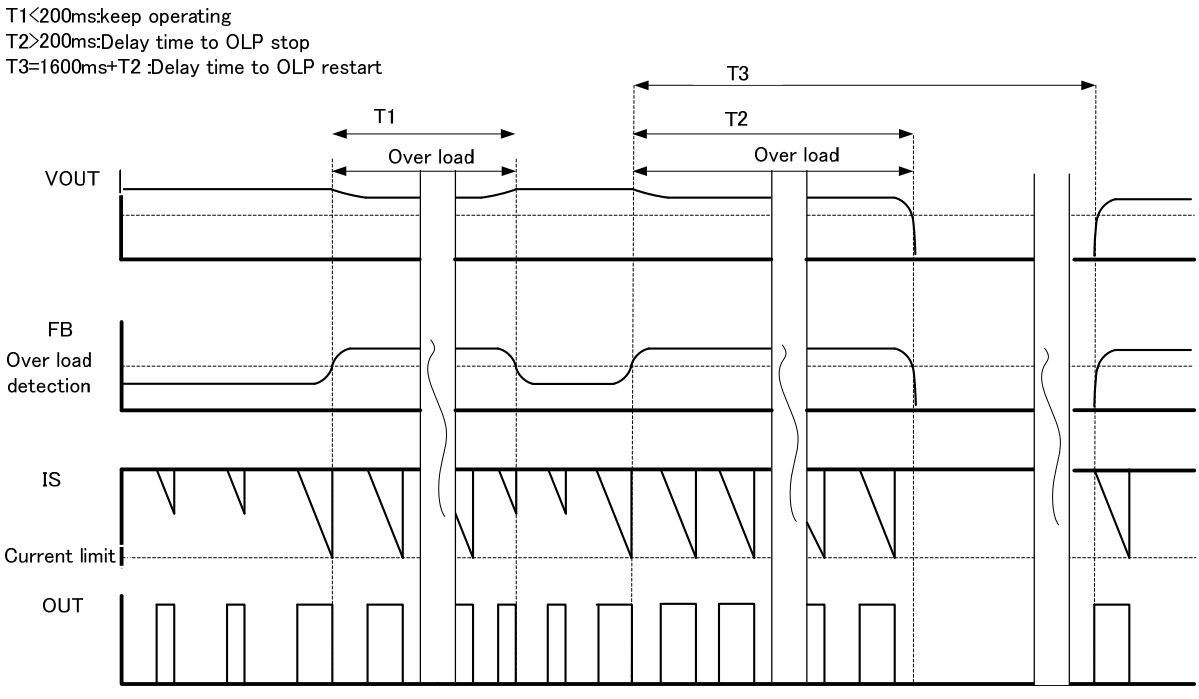


Fig. 11 Overload protection timing chart (auto restart)

(7) Overvoltage protection circuit (VCC pin)

FA5680/81 incorporates overvoltage protection circuit that monitors VCC voltage. (See Fig. 12.)

If VCC voltage rises and exceeds threshold voltage Vthovp: 26 V (typ.) of the comparator (OVP), comparator output is inverted to the high level, setting the latch circuit. At the same time, the startup circuit also starts operation and controls on/off of starting current to keep Vcc within the range of VCC pin voltage VCCLH: 13.0 V (typ.)/VCCLL: 12.0 V (typ.). This operation prevent to release of latch mode by drop of Vcc.The latch mode can be released by reducing the VCC pin voltage to the OFF threshold voltage VCCoff: 9.0 V (typ.) or less.

The delay time of TdOVP:65 us (typ.) is provided for set input of the latch circuit. Therefore, even if the VCC pin voltage momently reaches, such as noise, the detection voltage or becomes higher, transfer to the latch mode is not performed.

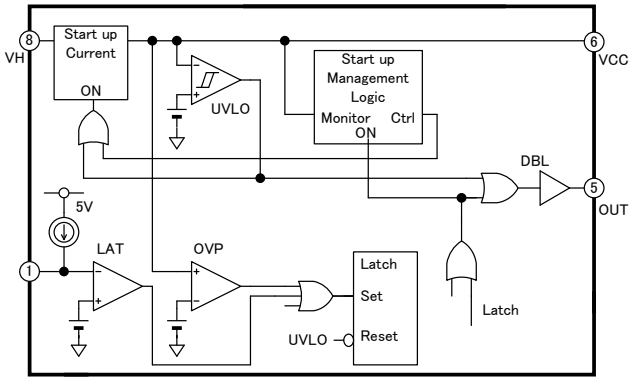


Fig. 12 Overvoltage protection circuit

(8) Latch off circuit by external signal

FA5680/81 is provided with latch off function in the LAT pin. (See Fig. 13.) Transfer to the latch mode is performed by lowering the LAT pin voltage to the external latch-stop threshold voltage level of VthLAT: 1.05 V (typ.) or less.

The latch mode can be released by reducing the VCC pin voltage to the OFF threshold voltage of VCCoff: 9.0 V (typ.) or less.

The latch function of the LAT pin operates only when the LAT pin voltage rises once up to the minimum pulse output voltage Vss1: 2.1 V (typ.) or more after the IC is started. Therefore, if the external latch cut-off function by the LAT pin is not used, connect only a capacitor.

(9) Under voltage lockout circuit (UVLO)

FA5680/81 incorporates a under voltage lockout circuit (UVLO) to prevent malfunction when Vcc voltage becomes low. When VCC voltage rises from 0˚ V, the IC starts operation at VCC = 18 V (typ.). When Vcc voltage decreases, the IC stops operation at VCC = 9.0 V (typ.). (VCCoff)

If UVLO operates and the IC stops operation, the OUT pin is forcibly kept in the low state. The latch mode of the protection circuit is also released.

(10) Output circuit

The output circuit is the push-pull structure and MOSFET can be driven directly. Output peak current of the OUT pin is 0.5 A for source and 1.0 A for sink in the absolute maximum rating. If the IC stops operation by UVLO or the latch mode function, the OUT pin becomes at the low level and MOSFET is cut off.

- **Overtemperature protection function –**

FA5680/81 can realize overtemperature protection function by connecting an NTC thermistor to the LAT pin. (See Fig. 13.) For details of this function, see Section 9-(4) “LAT pin”.

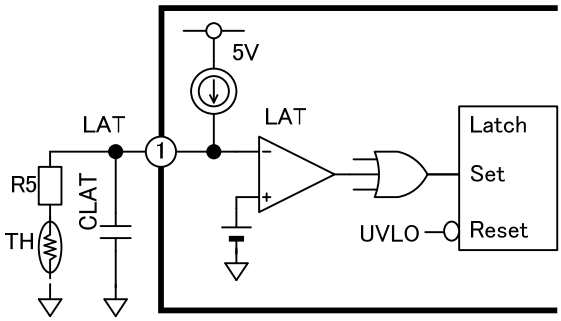


Fig. 13 Overtemperature protection function using thermistor

(11) Operation of Dynamic Self Supply (DSS)

This IC incorporates DSS function that operates the IC using startup circuit when no voltage is supplied from the auxiliary winding of transformer to the VCC pin. DSS operation is shown in Fig. 14. After the VCC pin UVLO is released, the LAT pin starts charging. When LAT pin voltage reaches to the minimum pulse output voltage Vss1: 2.1 V (typ.), switching is started and output voltage rises up to the specified value. Usually when power-supply output voltage Vo is started, VCC is supplied from the auxiliary winding of transformer. However, if output voltage becomes low due to change of it, supply cannot be made from auxiliary winding voltage. In that case, if the VCC pin voltage drops to the VCC hold voltage VCCDSSL: 10.5 V (typ.) , the IC internal signal VCC_SUST becomes H and the DSS operation mode is set. While DSS is operating, charge current flows from VH pin to VCC pin, the VCC pin voltage is kept between VCCDSSL: 10.5 V (typ.) and VCCDSSH: 12.5 V (typ.) and IC keeps operation. When the power-supply output voltage Vo returns, voltage is supplied from the auxiliary winding to the VCC pin. Subsequently, when VCC voltage rises up to 15 V (typ.), VCC_SUST becomes L and the DSS mode is ended.

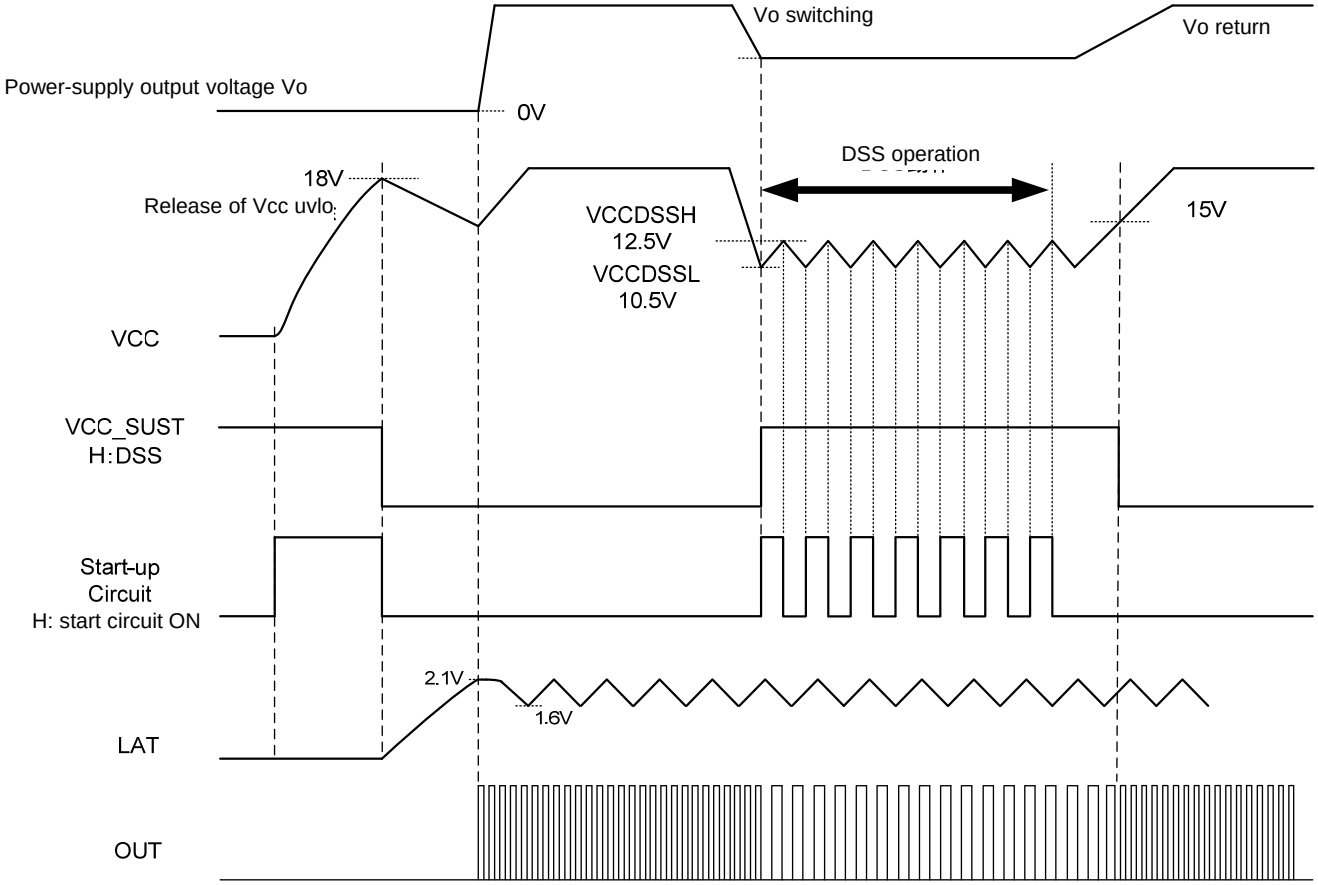


Fig. 14 Description of DSS operation

(12) Soft start

This IC can adjust the soft start time by the LAT pin capacity. Operation of soft start is shown in Fig. 15. The calculation method for soft start is described below. Areas ① to ② show the LAT pin waveform during start. Area ③ shows the soft-start period where the pulse width expands gradually. (Period where voltage drops from the soft-start start voltage Vss: 2.0 V (typ.) to the soft-start end voltage Vss3: 1.6 V (typ.)) Areas ① to ③ are explained below.
When the VCC voltage reaches the ON threshold voltage, the LAT pin voltage rises. When the LAT pin voltage reaches the minimum pulse output voltage Vss1: 2.1 V (typ.), switching is started.

During the period ①, the minimum ON width is forcibly output 32 times after switching is started. This period is about 500 us when operation is performed at 65 kHz. This forcible pulse output prevents Vds surge voltage of the power MOSFET during start.
During the period ②, the LAT pin voltage is discharged from Vss1: 2.1 V (typ.) to Vss: 2.0 V (typ.) at the constant current of the LAT pin source current Ilat: 70 uA (typ.). This is the output period of the minimum ON width.
The period ③ is the effective soft-start period where the pulse width expands gradually. In this soft-start period, the pulse width expands gradually from the minimum ON width. Soft-start time can be set by capacity of the capacitor connected to the LAT pin.
The effective soft-start period is the period in which the LAT pin voltage decreases from Vss: 2.0 V to Vss3: 1.6 V and can be found roughly by the following formula:

$Tss = 0.4 \times CLAT / Ilat$

where Tss = soft-start time [msec]
CLAT: latch pin capacitor capacity [uF]
Ilat: latch pin source current [uA] (70 uA typ.)

④ PWM operation start

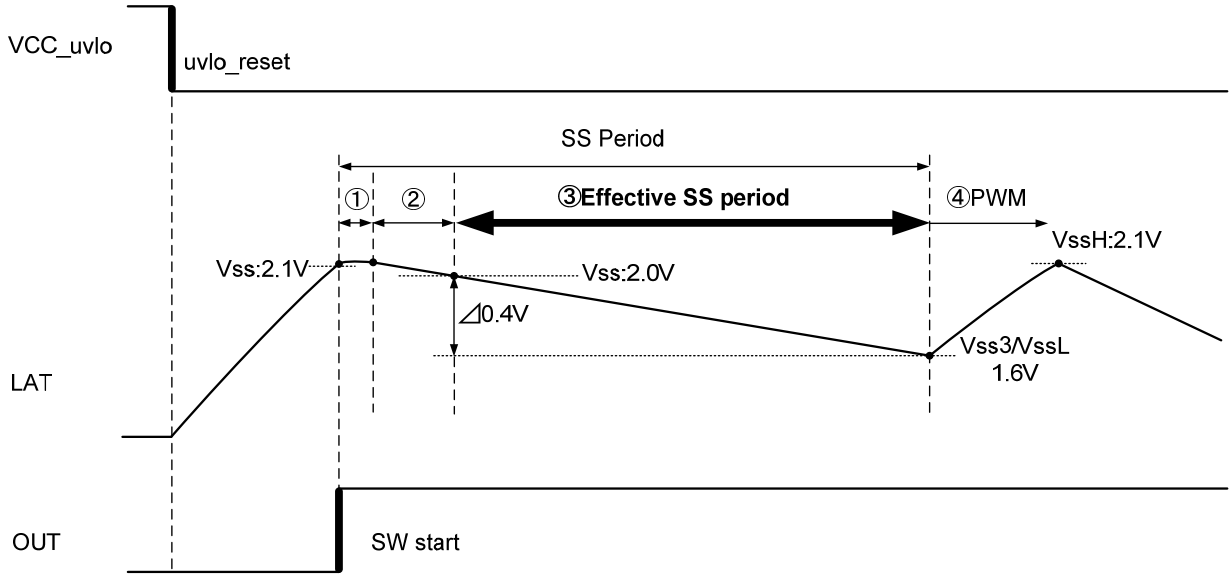


Fig. 15 Operation of soft start

In the case of FA5680, the LAT pin voltage rises up to the latch pin hold voltage Vss2: 2.5 V (typ.) while the overload protection is operating as shown in Fig. 16

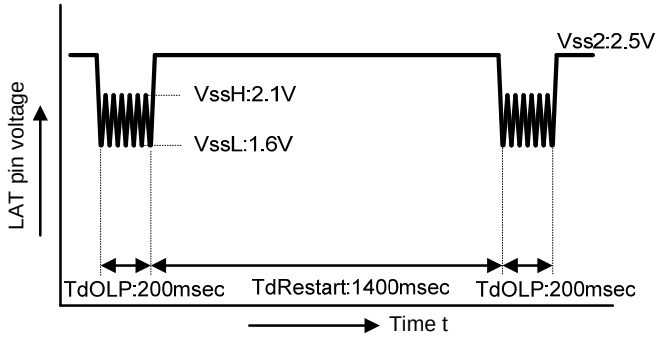


Fig. 16 LAT pin waveform while waiting for automatic reset during overload

9. Advice for design (The values in the following description are typical values unless otherwise specified.)

(1) Start up

To properly start and stop power supply, it is necessary to have proper capacitor connected to the VCC pin. Fig. 17 shows the VCC voltage during start when a proper capacitor is connected.

When AC line voltage is applied, the VCC capacitor is charged by the current supplied from the startup circuit and the voltage rises. Subsequently when VCC reaches the ON threshold voltage, the IC starts operation. Normally the IC is operated by the voltage supplied from the auxiliary winding. Just after the IC is started, however, VCC drops while the auxiliary winding voltage is rises enough. Select a proper VCC capacitor so that VCC does not drops to the OFF threshold voltage during this period. Specifically it is recommended to use a VCC pin capacitor that keeps the VCC higher than 11 V .

If the VCC capacitor value is too small, VCC drops to the startup circuit operating voltage of 10.5 V before the auxiliary winding voltage rises as shown in Fig. 18. In that case, VCC rises and drops repeatedly between VCCDSSL: 10.5 V (typ.) and VCCDSSH: 12.5 V (typ.) until the voltage from the auxiliary winding rises (DSS operation mode).

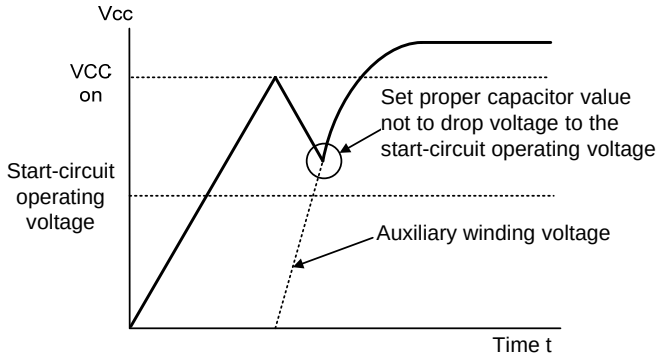


Fig. 17 VCC pin voltage at startup

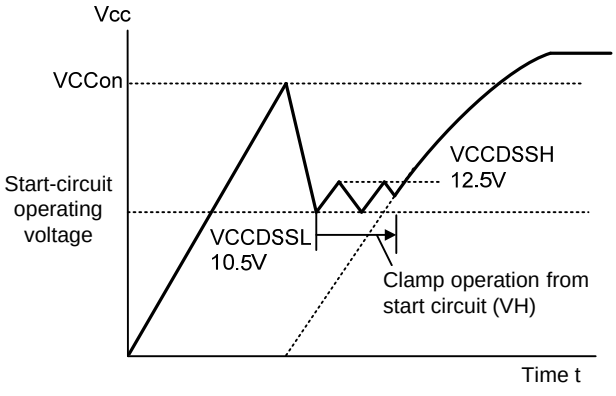


Fig. 18 VCC pin voltage at startup (when capacity value is too small)

(2) VH pin resistor

Generally as indicated in the explanation of each block operation, VH pin is connected via a resistor to DC voltage after half-wave rectification, full-wave rectification or rectification. Usually after power supply is started, the VCC voltage is supplied from the auxiliary winding, and the startup circuit is cut off. However, during overload detection (auto restart state) and use of DSS (state where the auxiliary winding voltage is lower due to output voltage change), the IC is operated by the current supplied from the VH pin. In that case, if the input line voltage is high, loss of the IC becomes large.

Therefore, if high voltage is applied to the VH pin, it is necessary to have proper VH pin resistor in order to satisfy the allowable loss of IC. (Lower limit value of starting resistance)

If VH pin resistor is too large, the operating current for the IC may not be kept. Especially in the usage where power-supply output current is used largely during DSS, operating frequency also becomes high and the MOSFET drive current increases. Therefore, it is necessary to increase current from the VH pin. (Upper limit value of start resistance)

For VH pin resistor, power consumption is small during normal operation, but large power is applied momentarily at startup. Therefore, it is advised to use a starting resistor which has sufficient rating power.

(3) Gate drive circuit

Usually resistors are installed between the MOSFET gate pin and the IC OUT pin to adjust switching speed and prevent parasitic oscillation at the gate pin. In some cases, drive current for turning on and off the MOSFET are decided independently. In that case, connect the gate drive circuit in Fig. 19 or 20 between the MOSFET gate pin and the IC OUT pin.

In the case of Fig. 19, current is limited by R1 + R2 when MOSFET is turned on, and it is limited by only R2 when MOSFET is turned off. In the case of Fig. 20, current is limited by only R1 when MOSFET is turned on, and it is limited by R1 and R2 connected in parallel when MOSFET is turned off.

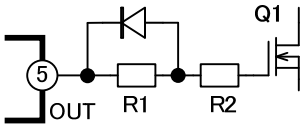


Fig. 19 Gate drive circuit (1)

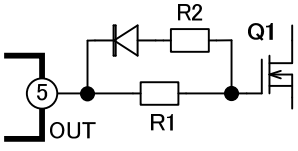


Fig. 20 Gate drive circuit (2)

(4) LAT pin

・Overtemperature protection using NTC thermistor

Overtemperature protection (latch cutoff) can be made by connecting thermistor TH1 to the LAT pin as shown in Fig. 21. The LAT pin source current is Ilat: 70 uA (Typ.). Therefore, select TH so that thermistor resistance Rth satisfies the following formula at the desired overtemperature protection operating temperature. Adjustment can be made by connecting R5 to thermistor TH in series.

$$Rth@LAT+R5 \leqq 1.05V / 70uA \fallingdotseq 15.0k\Omega$$

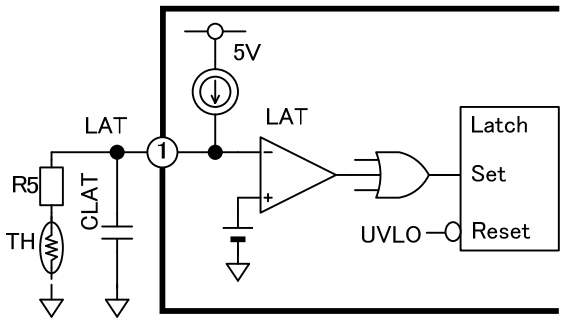


Fig. 21 Overtemperature protection function using thermistor

There is a certain correlation between the LAT pin source current (ILAT) and the external latch stop level (VthLAT). Therefore, each values of ILAT and VthLAT do not disperse between Min-Max. Dispersion of the detection values within the IC is specified by the resistance value (RLAT) decided by the current and voltage values.

・Latch off by external error detection signal

The NPN transistor Tr1 is connected to the LAT pin and detection signal is input to the Tr1 base to perform latch off as shown in Fig. 22. Correctly match the polarity so that the input signal becomes high when an error occurs. Constant current flows out from the LAT pin. Therefore, it is not necessary to use a circuit that pulls up the LAT pin voltage over the latch cutoff threshold voltage in the normal situation.

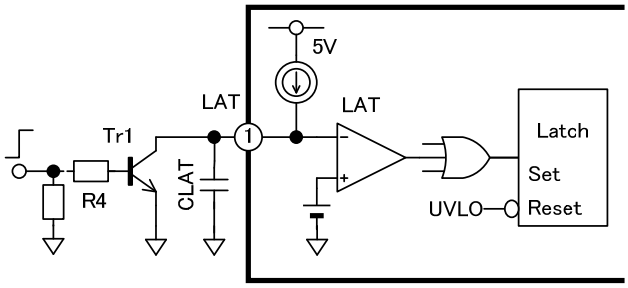


Fig. 22 Latch cutoff function by external signal

(5) Feedback circuit

The circuit of the FB pin is shown in Fig. 23. Photocoupler PC as feedback circuit is connected to monitor output voltage and perform PWM control. This signal gives the threshold voltage for the current comparator. Therefore, if noise is applied, pulse may be disturbed. Usually capacitor C3 is connected to prevent noise.

Connect the capacitor C3 as near the IC as possible so that it can operate efficiently, and carefully wiring.

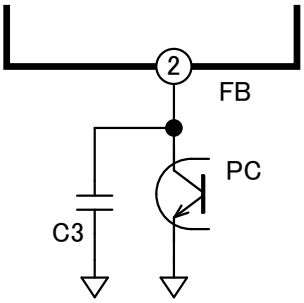


Fig. 23 Configuration of FB pin circuit

(6) Current sensing

As described in Section 8-(5) “One-shot circuit”, the minimum ON width is set in FA5680/81. Therefore, usually no malfunction is caused by surge current when the Power MOSFET is turned on. However, if surge current is large when the Power MOSFET is turned on or external noise is applied, malfunction may be caused. In such a case, add CR filters C6 and R7 to the IS pins as shown in Fig. 24.

It is advised to select CR filters according to cutoff frequency and time constant. Cutoff frequency can be found by the following formula:

$$fc = 1/(2 \times \pi \times C6 \times R7).$$

Set this frequency to be larger than the operating frequency of 65 kHz. Also set the CR time constant to be 500 nsec or less.

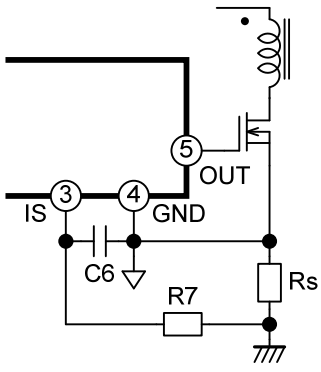


Fig. 24 IS pin filter

In addition, due to input bias current of IS pin, offset voltage is generated on resistor R7. Therefore, note that if large resistor is connected, overload output may fluctuate significantly. Also note that if the C6 capacity becomes large, delay time becomes large and overload detection value fluctuates.

Recommended values: R7 = 1 kΩ
C6 = 100 pF to 470 pF

Connect the capacitor C6 as near the IC as possible so that it can operate efficiently, and carefully wiring.

(7) Compensation for dependence of overload to AC line voltage

When the overload protection function is used, current value for overload detection differs because the gradient of transformer current differs according to the input voltage and there is delay time in the IS pin. (Fig. 25)

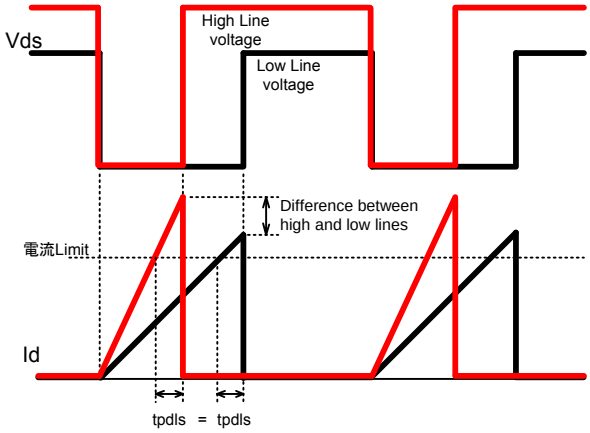


Fig. 25 Dependence of overload detection level to input voltage

This dependence of overload output to input voltage can be improved by connecting resistor R9 between the transformer auxiliary winding and the IS pin as shown in Fig. 26. (Fig. 27)

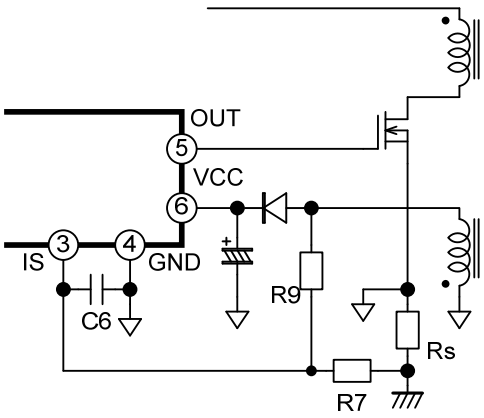


Fig. 26 compensation circuit for overload protection

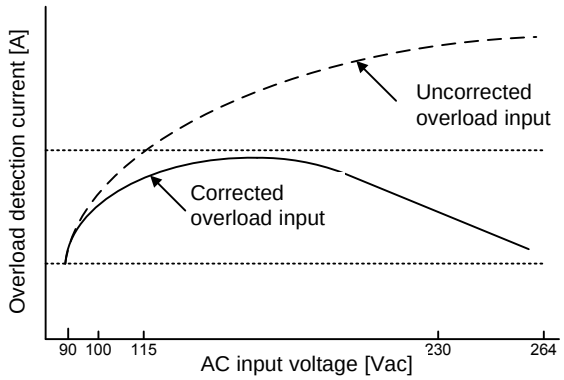


Fig. 27 Improved dependence of overload output to input voltage

This IC adopts the minus voltage method for current detection. Therefore, the minus voltage of the auxiliary winding proportionate to input voltage is used and the offset voltage is applied to the IS pin to compensate. Therefore, compensation can be made by relatively low voltage and the loss can be reduced.
For example, if resistor R7 is 1 kΩ, it is advised to use resistor R9 of 100 kΩ to 1 MΩ. The smaller the resistor R9 is, the larger the compensation amount is.

(8) Improvement of input power during light load

FA5680/81 incorporates a function for reduction of standby power by decreasing oscillating frequency during light load. In some cases, however, reduction of standby power by the built-in IC may be insufficient because load conditions differ according to power supply sets. In such a case, connect resistor R8 between the OUT pin and the IS pin as shown in Fig. 28. For example, if resistor R7 is 1 kΩ, use R8 of several hundred kΩ to 1 MΩ.

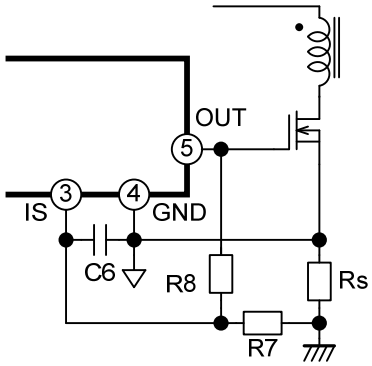


Fig. 28 Correction circuit for improvement of input power during light load

(9) Rough calculation of overload detection value

The following shows the rough calculation of overload detection value when CR filter is connected to the IS pin, input dependency (line compensation) is improved and input power is improved during light load.

When only CR filter is connected (Connection is shown in Fig. 24.)

Offset voltage Voffset1 is added on the IS pin voltage by the IS pin input bias current 45 uA (when IS = −0.5 V) and resistor R7 as shown in Fig. 29. Therefore, overload detection voltage value detected by the IS pin becomes − |VthlS1| + |Voffset1|

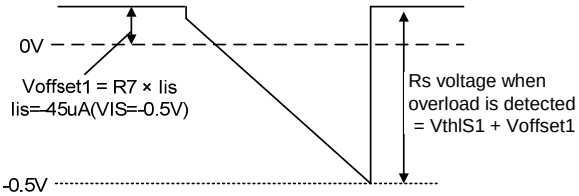


Fig. 29 IS pin voltage when only CR filter is connected

The design example of overload detection value in this state is shown below. (rough idea of current detection resistor Rs)

When AC input voltage Vin is minimum, primary current ILp becomes maximum. In this case, ILP can be found by the following formula:

$$D = \frac{\frac{Np}{Ns} \times Vo}{\sqrt{2} \times Vin + \frac{Np}{Ns} \times Vo}$$

$$ILp = \frac{Po}{\sqrt{2} \times Vin \times D \times \eta} + \frac{\sqrt{2} \times Vin \times D}{2 \times Lp \times fsw}$$

D: Duty, Vin: input voltage (rms)
Np1: primary winding (turn),
Ns: secondary winding (turn), Vo: output voltage,
Po: output power, η: efficiency,
Fsw: switching frequency
Lp = primary inductance of transformer

Example) When Vin = 85 V, Np = 28T, Ns = 5T, Lp = 340 uH, fsw = 65 kHz, μ = 0.9, Vo = 19 V,
Po = 100 W (overload detection power) and
R7 = 1 kΩ, calculation can be made as follows:

$$D = \frac{\frac{28}{5} \times 19}{\sqrt{2} \times 85 + \frac{28}{5} \times 19} = 0.47$$

$$ILp = \frac{100}{\sqrt{2} \times 85 \times 0.47 \times 0.9} + \frac{\sqrt{2} \times 85 \times 0.47}{2 \times 340u \times 65k} = 3.245A$$

$$Rs = |VthIS1 + Voffset1) / ILp$$

$$= |-0.5 + (-45u \times 1k)| / 3.245 = 0.168$$

Therefore, it is required to connect Rs = 0.17 Ω. However, since actually delay time occurs in the IC and MOSFET circuits, overload detection value is slightly larger than the value calculated above.

When resistor R9 for compensation of dependence to input voltage is connected (connection is shown in Fig. 26)

When resistor for compensation of dependence to input voltage is connected, IS pin voltage changes as shown in Fig. 30. In this case, overload detection voltage value detected by the IS pin becomes VthiS1 – Voffset2.

Example 1: When R7 = 1 kΩ, R9 = 330 kΩ, Vaux2 = 20 V,
Voffset2 = Voffset1 − ((Vaux2/R9) × R7)
= (−45 uA × 1 k) − ((−20 V/330 k) × 1 k) = 15.6 mV
Rs voltage when overload is detected = −0.5 V −(15.6 mV) = −0.516 V

Example 2: When R7=1 kΩ, R9=680 kΩ, Vau x 2 = 20 V = 20 V,
Voffset2 = (−45 uA × 1 k) − ((−20 V/680 k) × 1 k) = −15.6 mV
Rs voltage when overload is detected = −0.5 V − (−15.6 mV) = −0.484 V

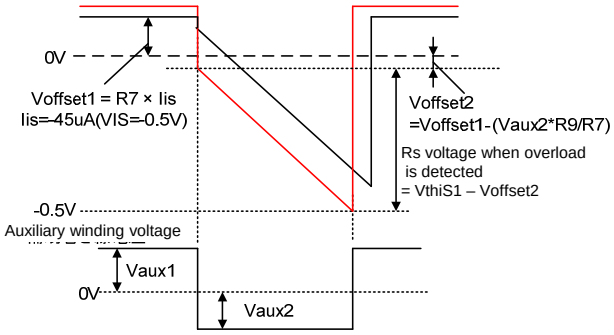


Fig. 30 IS pin voltage when correction circuit R9 is connected

When input power is improved during at load (Connection is shown in Fig. 28)

When input power is improved during at load, waveform of the IS pin voltage changes as shown in Fig. 31. In this case, overload detection voltage value detected by the IS pin becomes VthlS1 + Voffset1 + Voffset3.

Example: When R7 = 1 KΩ, R8 = 1.0 MΩ and VCC = 18 V,
Voffset1 = −45 mV
Voffset3= − (18/1.0 M) × 1 k= − 0.018 V
Rs voltage when overload is detected = −0.5 V − 45 mV − 0.018 V = − 0.563 V

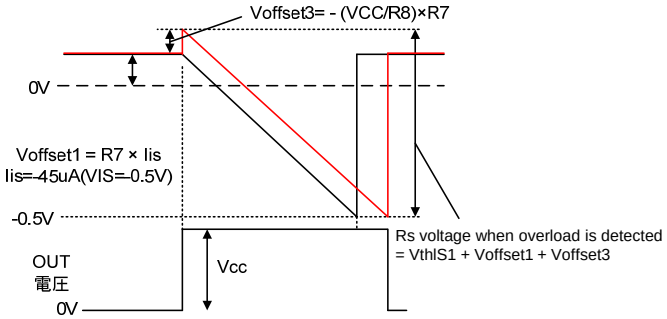


Fig. 31 IS pin voltage when correction resistor R8 is connected

When the dependence of overload to input voltage and the input power at light load are improved, operation is performed in the waveform made by adding the waveform in Fig. 30 to that in Fig. 31.

(10) Prevention of malfunction by negative voltage of each pin

If large minus voltage is applied to each pin of the IC, parasitic elements within the IC may operate and malfunction may result. Be careful so that voltage within the absolute maximum rating is applied to each pin.

If there is a possibility that negative voltage is applied to the VH pin depending on AC input voltage , improvement can be made by connect diode D1 between the VH – VCC. (Fig. 32)

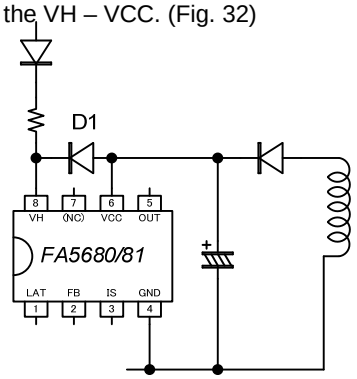


Fig. 32 Prevention of negative voltage applied to VH pin

(11) Loss calculation

To use the IC within the rating, it is necessary to check the IC loss. Since it is very difficult to directly measure the IC loss, the example of rough idea found by calculation is shown below.

When the voltage applied to the VH pin is VVH, the current flows to the VH pin is IHrun during operation, power-supply voltage is VCC, consumption current of the IC is ICCop1, gate input charge amount of the used MOSFET is Qg, and switching frequency is fsw, then the estimated value of IC total loss Pd can be found by the following formula:

$$Pd \approx VCC \times (ICCop1 + Qg \times fsw) + VVH \times IHrun$$

The estimated value can be found in this calculation. Total loss Pd found in this calculation is a little larger than the actual value. In addition, carefully consider temperature characteristics and tolerance in each characteristic value.

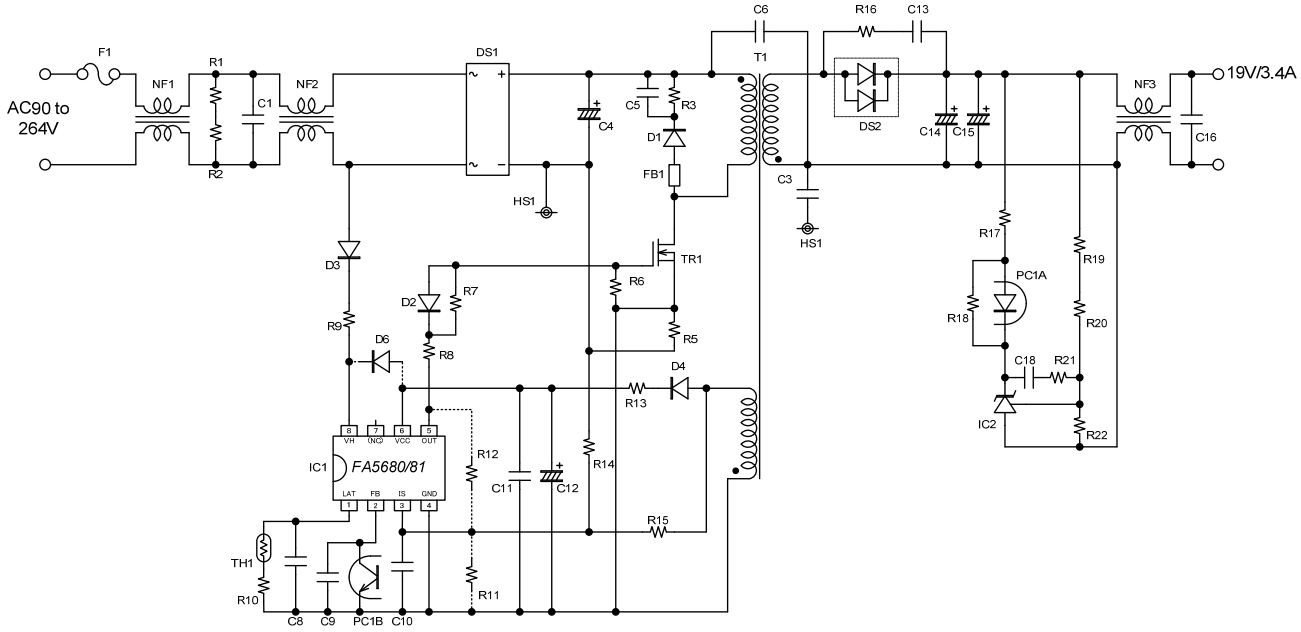
Example:

When the VH pin is connected to 100 V AC input in half-wave rectification waveform, the average voltage applied to the VH pin is about 45 V.
If it is assumed that FA5680/81 is operated at Tj = 25℃, VCC=18 V and Qg = 80 nC, then
IHrun = 15 uA (typ.), ICCop = 1.35 mA (typ.) and
fsw = 65 kHz (typ.)

Therefore, loss of the standard characteristic IC is calculated as follows:

$$Pd \approx 18V \times (1.35\ mA + 80\ nC \times 65\ kHz) + 45\ V \times 15\ uA$$
$$\approx 119\ mW$$

10. Application circuit



Note) This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.

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