

FMP60N133S2FDHF

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FUJI POWER MOSFET

Super J MOS[®] S2 series

N-Channel enhancement mode power MOSFET

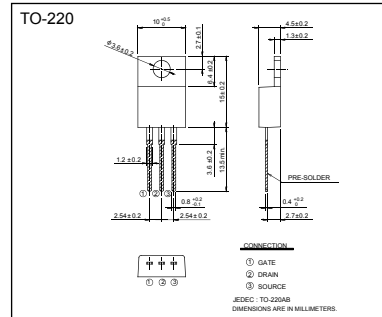
Features

- Pb-free lead terminal
- RoHS compliant
- uses Halogen-free molding compound

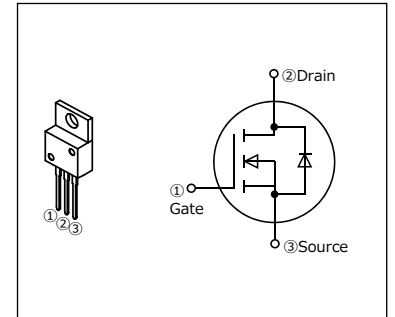
Applications

- For switching

Outline Drawings [mm]



Equivalent circuit schematic



Absolute Maximum Ratings at $T_{vj}=25^{\circ}\text{C}$ (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30\text{V}$
Continuous Drain Current	I_D	30.1	A	$T_{vj}=25^{\circ}\text{C}$ Note*1,2
		19	A	$T_{vj}=100^{\circ}\text{C}$ Note*1,2
Pulsed Drain Current	I_{DP}	90.8	A	Note *2
Gate-Source Voltage	V_{GS}	±30	V	
Non-Repetitive Maximum Avalanche Current	I_{AS}	3.5	A	Note *3
Non-Repetitive Maximum Avalanche Energy	E_{AS}	748	mJ	Note *4
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	V/ns	$V_{DS} \leq 600\text{V}$
Continuous Diode Forward Current	I_{SD}	30.1	A	$T_{vj}=25^{\circ}\text{C}$ Note*1,2
		19	A	$T_{vj}=100^{\circ}\text{C}$ Note*1,2
Pulsed Diode Forward Current	I_{SDP}	90.8	A	Note *2
Peak Diode Recovery dV/dt	dV/dt	30	V/ns	Note *3
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *4
Maximum Power Dissipation	P_D	2.02	W	$T_a=25^{\circ}\text{C}$
		160		$T_{vj}=25^{\circ}\text{C}$
Operating and Storage Temperature range	T_{ch}	150	°C	
	T_{slg}	-55 to +150	°C	

Note *1 : Maximum duty cycle D=0.65

Note *2 : Limited by maximum channel temperature.

Note *3 : $T_{ch} \leq 150^{\circ}\text{C}$, See Fig.1 and Fig.2

Note *4 : Starting $T_{ch}=25^{\circ}\text{C}$, $I_{AS}=2.1\text{A}$, $L=311\text{mH}$, $V_{DD}=60\text{V}$, $R_G=50\Omega$, See Fig.1 and Fig.2

E_{AS} limited by maximum channel temperature and avalanche current.

Note *5 : $I_{SD} \leq 22.7\text{A}$, $-di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DS \text{ peak}} \leq 600\text{V}$, $T_{ch} \leq 150^{\circ}\text{C}$.

Note *6 : $I_{SD} \leq 22.7\text{A}$, $dV/dt \leq 30\text{V}/\text{ns}$, $V_{DS \text{ peak}} \leq 600\text{V}$, $T_{ch} \leq 150^{\circ}\text{C}$.

■ Electrical Characteristics at $T_{vj}=25^{\circ}\text{C}$ (unless otherwise specified)

• Static Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$ $I_D=250\mu\text{A}$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ $I_D=3.5\text{mA}$	3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=600\text{V}$ $V_{GS}=0\text{V}$ $T_{ch}=25^{\circ}\text{C}$	-	-	25	μA
		$V_{DS}=480\text{V}$ $V_{GS}=0\text{V}$ $T_{ch}=125^{\circ}\text{C}$	-	36	-	
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0\text{V}$ $V_{GS}=\pm 30\text{V}$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$ $I_D=11.4\text{A}$	-	0.117	0.133	Ω
Gate resistance	R_G	$f=1\text{MHz}$, open drain	-	8.3	-	Ω

• Dynamic Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g_{fs}	$V_{DS}=25\text{V}$ $I_D=11.4\text{A}$	7.5	15	-	S
Input Capacitance	C_{iss}	$V_{DS}=400\text{V}$	-	1190	-	pF
Output Capacitance	C_{oss}	$V_{GS}=0\text{V}$	-	42	-	
Reverse Transfer Capacitance	C_{rss}	$f=250\text{kHz}$	-	5.8	-	
Effective output capacitance, energy related (Note *7)	$C_{o(er)}$	$V_{DS}=0\ldots 400\text{V}$ $V_{GS}=0\text{V}$	-	103	-	pF
Effective output capacitance, time related (Note *8)	$C_{o(tr)}$	$V_{DS}=0\ldots 400\text{V}$ $V_{GS}=0\text{V}$ $I_D=\text{constant}$	-	410	-	
Turn-On Time	$t_{d(on)}$	$V_{DD}=400\text{V}$, $V_{GS}=10\text{V}$ $I_D=11.4\text{A}$, $R_G=15\Omega$ See Fig.3 and Fig.4	-	20	-	ns
	t_r		-	65	-	
Turn-Off Time	$t_{d(off)}$		-	131	-	
	t_f		-	23	-	
Total Gate Charge	Q_G	$V_{DD}=400\text{V}$, $V_{GS}=10\text{V}$ $I_D=22.7\text{A}$ See Fig.5	-	59	-	nC
Gate-Source Charge	Q_{GS}		-	20	-	
Gate-Drain Charge	Q_{GD}		-	27	-	
Drain-Source crossover Charge	Q_{SW}		-	13	-	

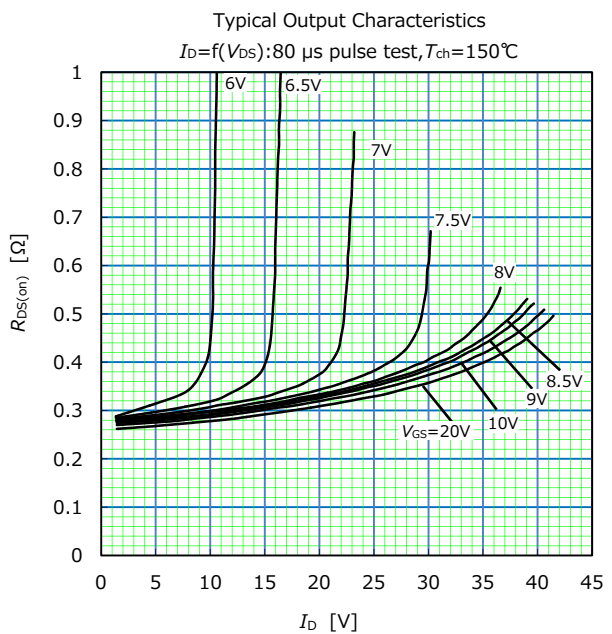
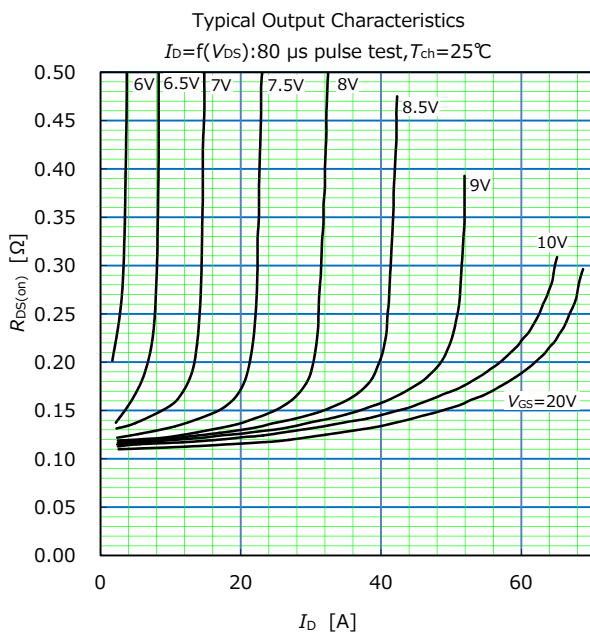
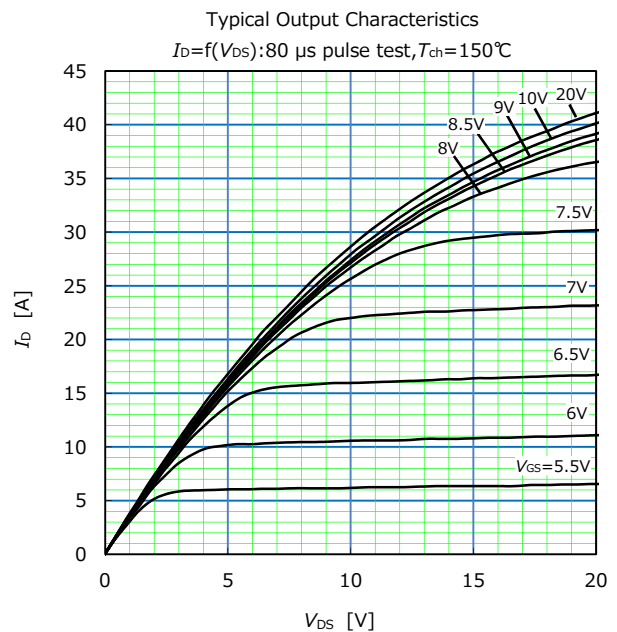
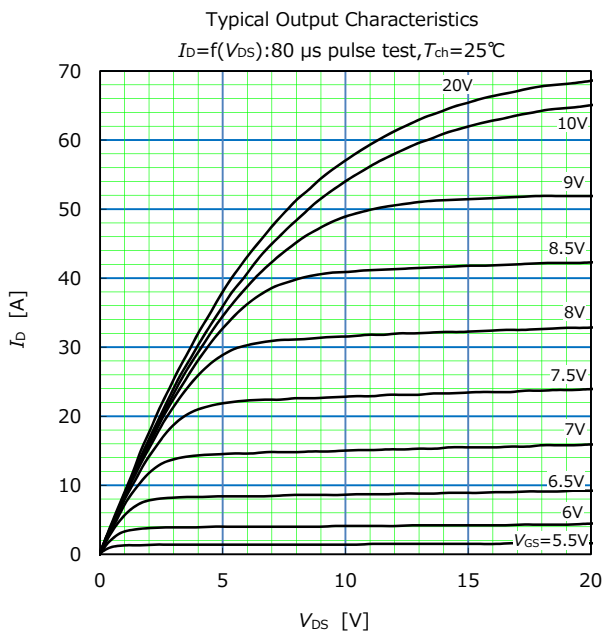
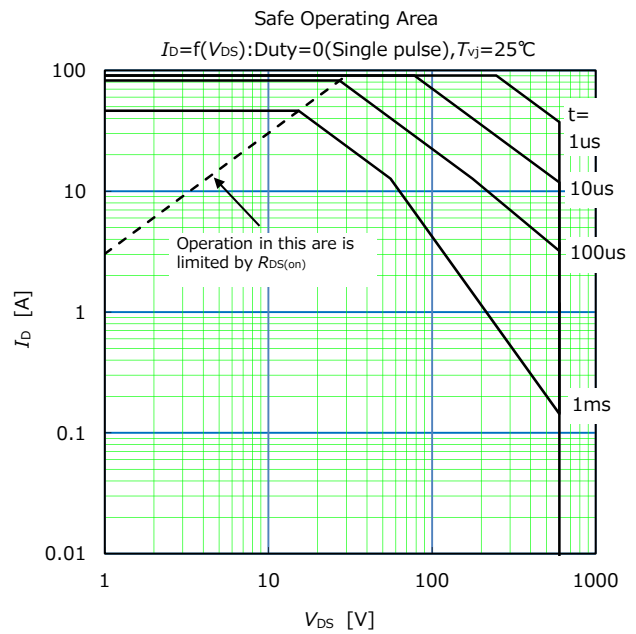
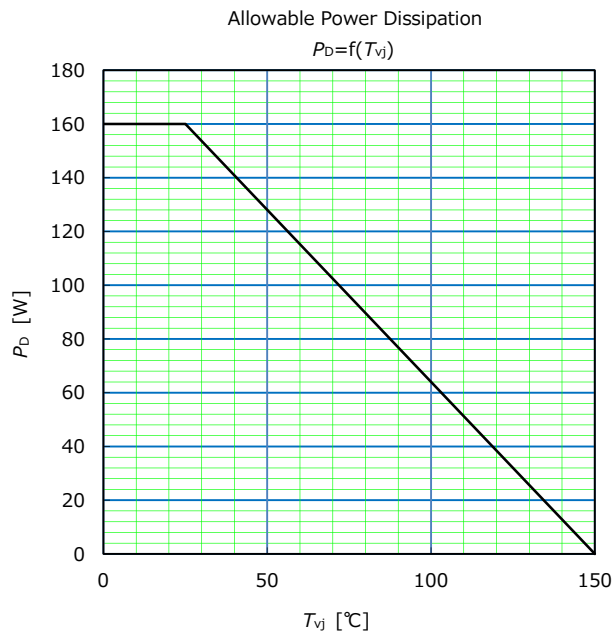
Note *7 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.Note *8 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

• Reverse Diode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	V_{SD}	$I_{SD}=22.7\text{A}$, $V_{GS}=0\text{V}$ $T_{ch}=25^{\circ}\text{C}$	-	0.95	1.35	V
Reverse Recovery Time	t_{rr}	$V_{DD}=400\text{V}$, $I_{SD}=22.7\text{A}$ $-di/dt=100\text{A}/\mu\text{s}$ $T_{ch}=25^{\circ}\text{C}$ See Fig.6 and Fig.7	-	160	-	ns
Reverse Recovery Charge	Q_{rr}		-	1.2	-	μC
Peak Reverse Recovery Current	I_{rp}		-	14.5	-	A

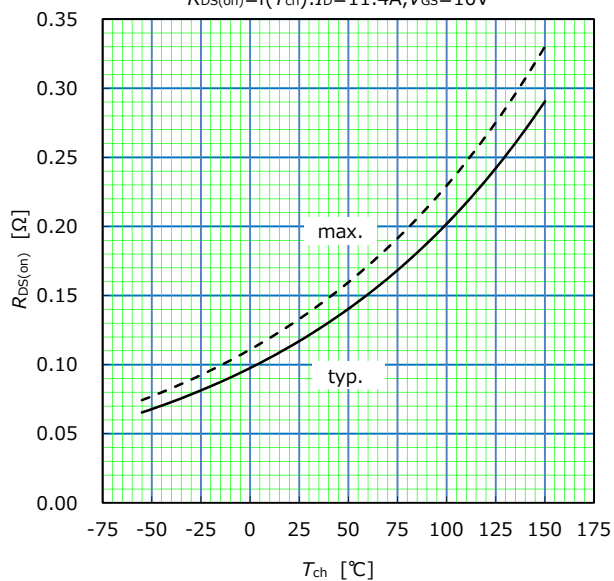
■ Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	0.781	$^{\circ}\text{C}/\text{W}$
Channel to Ambient	$R_{th(ch-a)}$	-	-	62	$^{\circ}\text{C}/\text{W}$

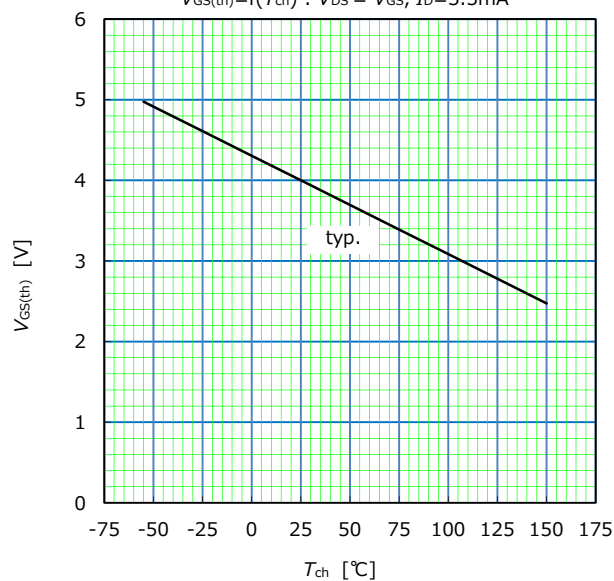


Drain-Source On-state Resistance

$$R_{DS(on)} = f(T_{ch}) : I_D = 11.4A, V_{GS} = 10V$$

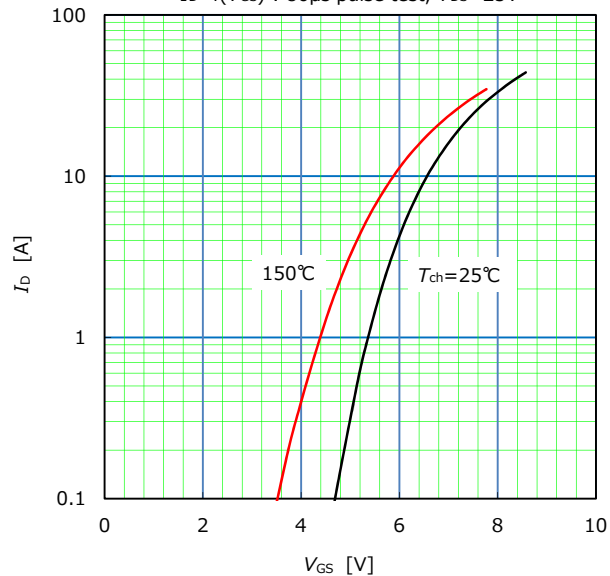
Gate Threshold Voltage vs. T_{ch}

$$V_{GS(th)} = f(T_{ch}) : V_{DS} = V_{GS}, I_D = 3.5mA$$



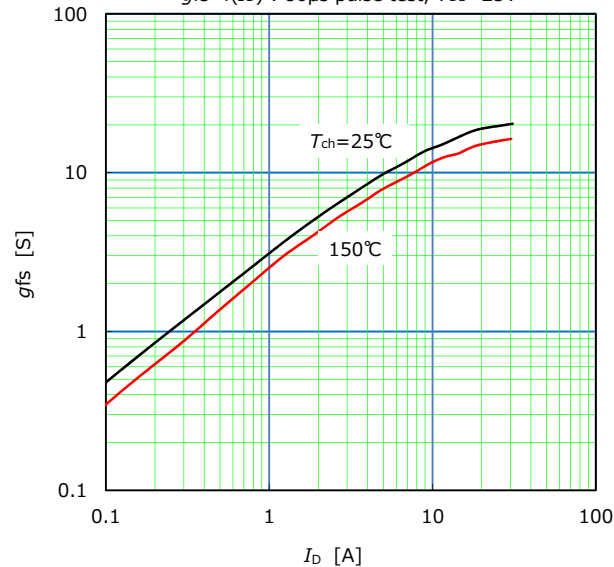
Typical Transfer Characteristic

$$I_D = f(V_{GS}) : 80\mu s \text{ pulse test, } V_{DS} = 25V$$



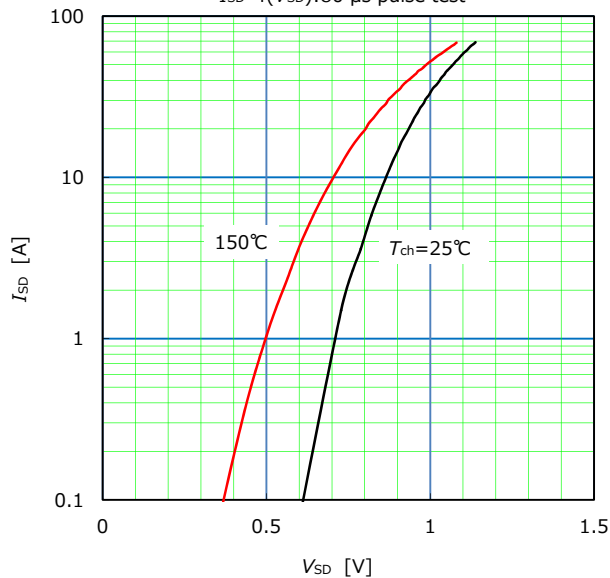
Typical Transconductance

$$g_{fs} = f(I_D) : 80\mu s \text{ pulse test, } V_{DS} = 25V$$



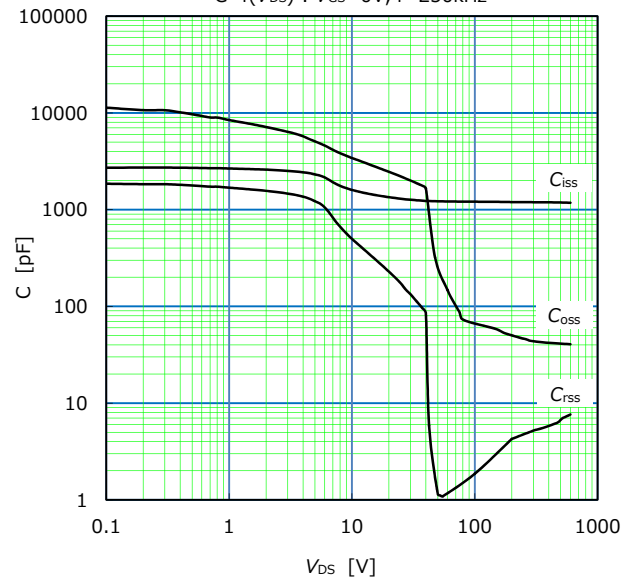
Typical Forward Characteristics of Reverse Diode

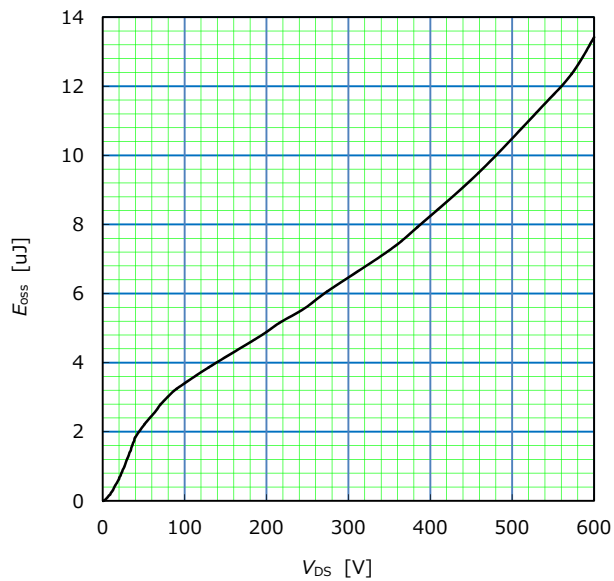
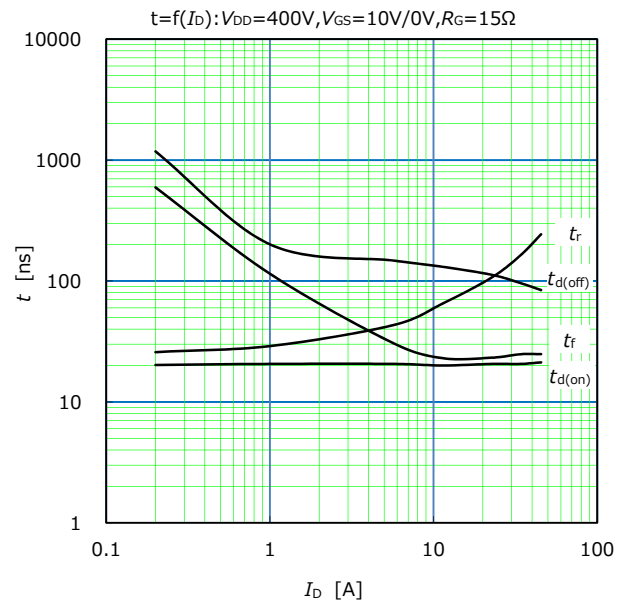
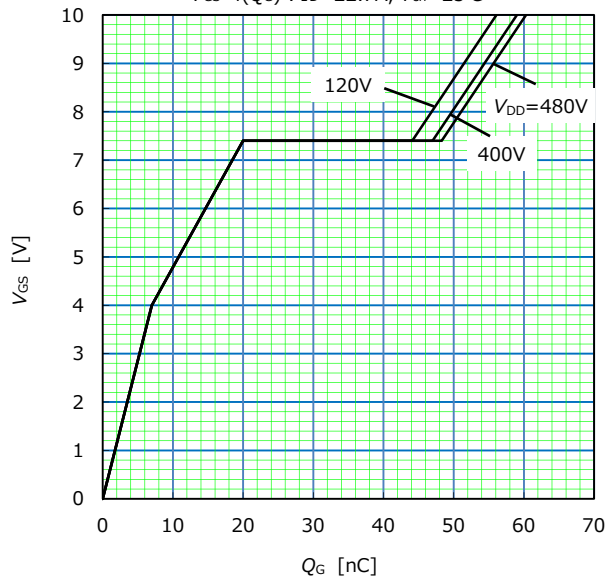
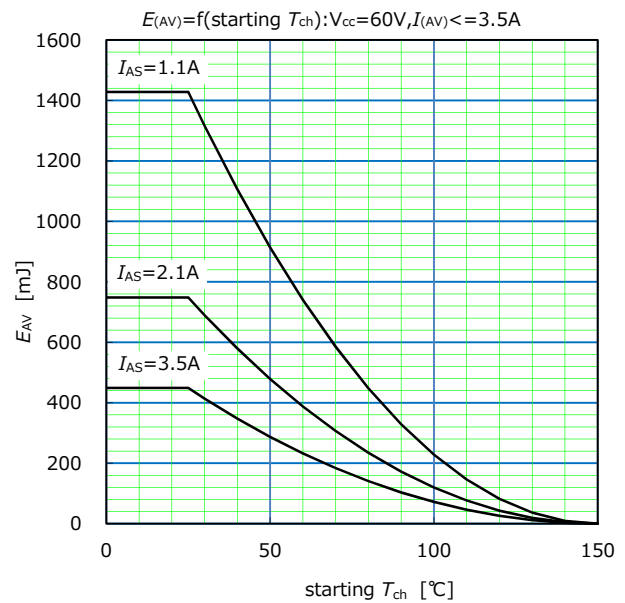
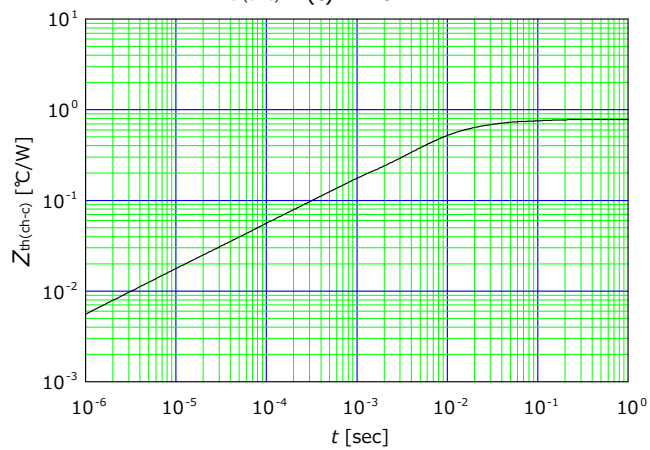
$$I_{SD} = f(V_{SD}) : 80\mu s \text{ pulse test}$$



Typical Capacitance

$$C = f(V_{DS}) : V_{GS} = 0V, f = 250kHz$$



Typical C_{oss} stored energyTypical Switching Characteristics vs. I_D $T_{ch}=25^\circ\text{C}$ Typical Gate Charge Characteristics
 $V_{GS}=f(Q_G): I_D=22.7\text{A}, T_{ch}=25^\circ\text{C}$ Maximum Avalanche Energy vs. starting T_{ch} Transient Thermal Impedance
 $Z_{th(ch-c)}=f(t): D=0$ 

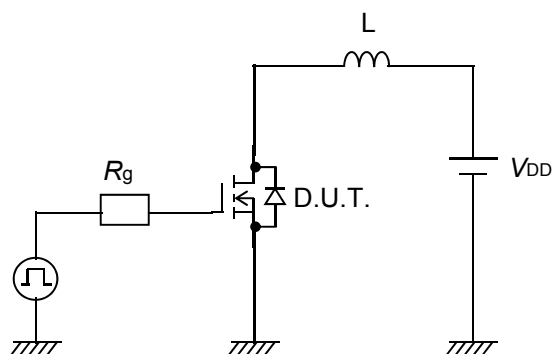


Fig.1 Avalanche Test circuit

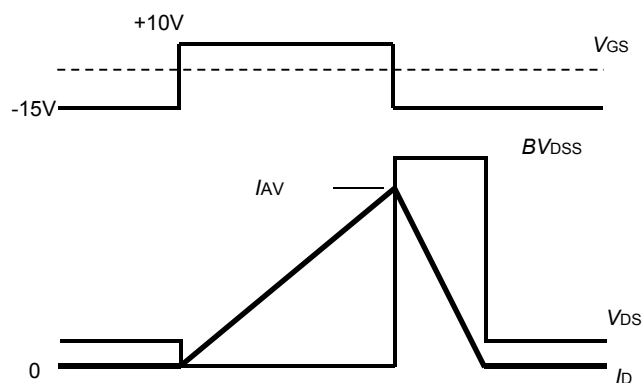


Fig.2 Operating waveforms of Avalanche Test

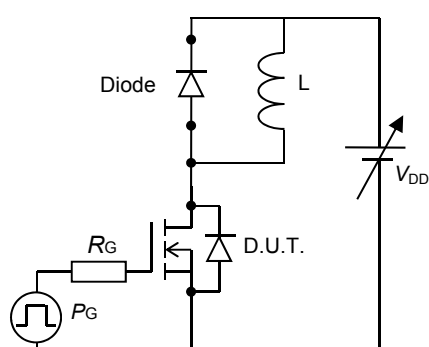


Fig.3 Switching Test circuit

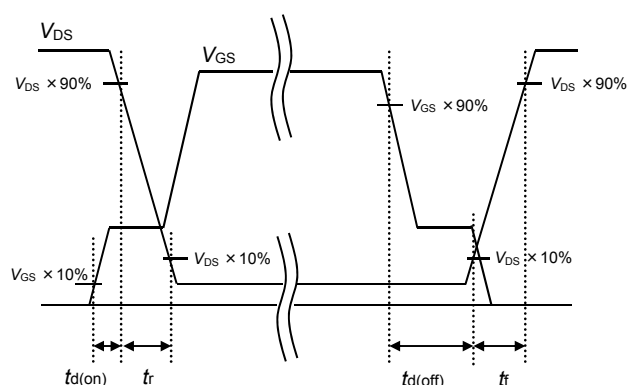


Fig.4 Operating waveform of Switching Test

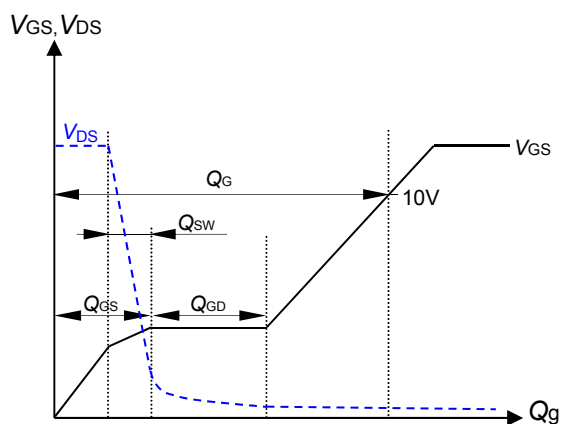


Fig.5 Operating waveform of Gate charge Test

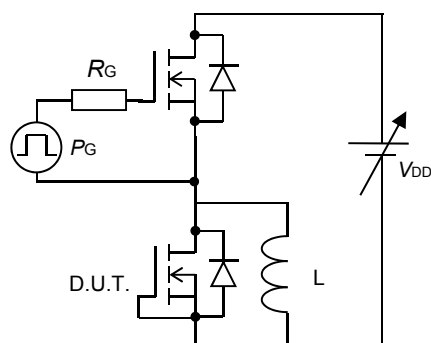


Fig.6 Reverse recovery Test circuit

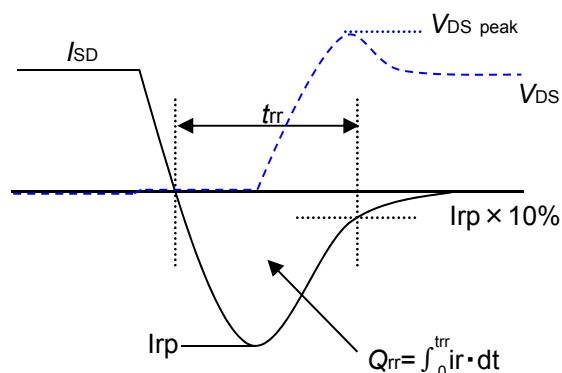
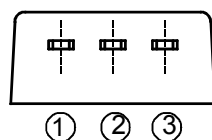
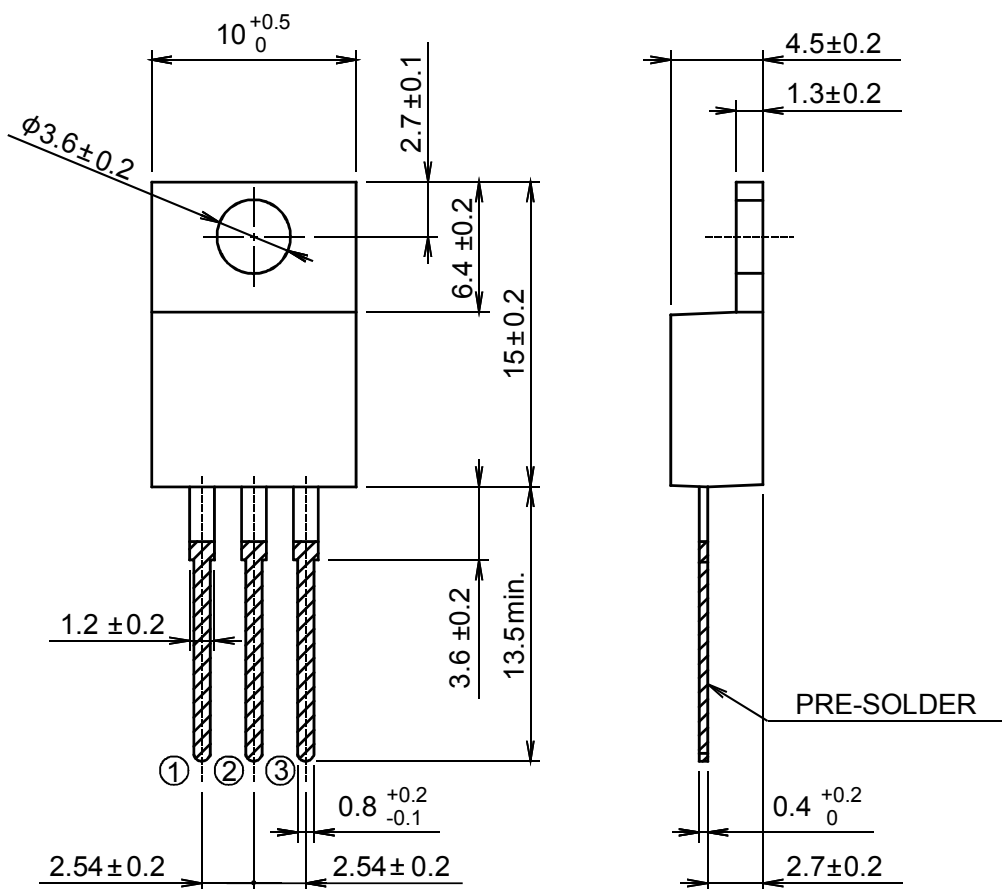


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-220 Package

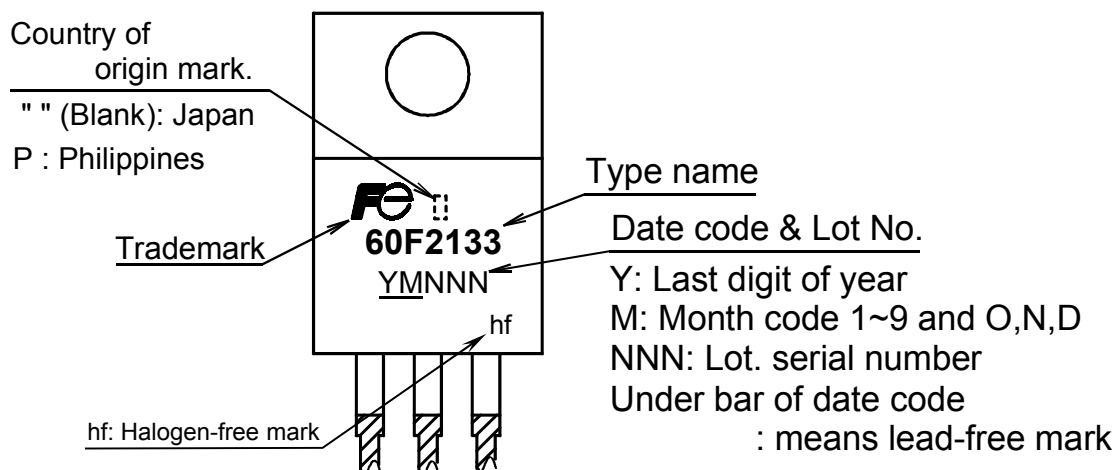
CONNECTION

- ① GATE
- ② DRAIN
- ③ SOURCE

JEDEC : TO-220AB

DIMENSIONS ARE IN MILLIMETERS.

■ Marking



* The font (font type,size) and the trademark-size might be actually different.

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