

# FMV60N084S2FDHF

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FUJI POWER MOSFET

## Super J MOS<sup>®</sup> S2 series

## N-Channel enhancement mode power MOSFET

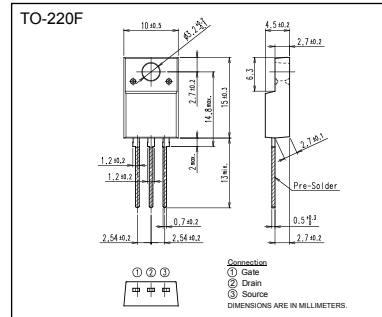
### Features

- Pb-free lead terminal
- RoHS compliant
- uses Halogen-free molding compound

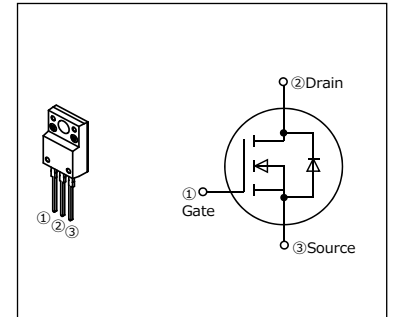
### Applications

- For switching

### Outline Drawings [mm]



### Equivalent circuit schematic



### Absolute Maximum Ratings at $T_{vj}=25^{\circ}\text{C}$ (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	$V_{DS}$	600	V	
	$V_{DSX}$	600	V	$V_{GS}=-30\text{V}$
Continuous Drain Current	$I_D$	47.9	A	$T_{vj}=25^{\circ}\text{C}$ Note*1,2
		30.3	A	$T_{vj}=100^{\circ}\text{C}$ Note*1,2
Pulsed Drain Current	$I_{DP}$	148	A	Note *2
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V	
Non-Repetitive Maximum Avalanche Current	$I_{AS}$	5.5	A	Note *3
Non-Repetitive Maximum Avalanche Energy	$E_{AS}$	1177	mJ	Note *4
Maximum Drain-Source dV/dt	$dV_{DS}/dt$	50	V/ns	$V_{DS} \leq 600\text{V}$
Continuous Diode Forward Current	$I_{SD}$	47.9	A	$T_{vj}=25^{\circ}\text{C}$ Note*1,2
		30.3	A	$T_{vj}=100^{\circ}\text{C}$ Note*1,2
Pulsed Diode Forward Current	$I_{SDP}$	148	A	Note *2
Peak Diode Recovery dV/dt	$dV/dt$	30	V/ns	Note *5
Peak Diode Recovery -di/dt	$-di/dt$	100	A/ $\mu\text{s}$	Note *6
Maximum Power Dissipation	$P_D$	2.16	W	$T_a=25^{\circ}\text{C}$
		95		$T_{vj}=25^{\circ}\text{C}$
Operating and Storage Temperature range	$T_{ch}$	150	$^{\circ}\text{C}$	
	$T_{stg}$	-55 to +150	$^{\circ}\text{C}$	
Isolation Voltage (TO-220F)	$V_{iso}$	2	kVrms	$t=60\text{sec}, f=60\text{Hz}$

Note \*1 : Maximum duty cycle  $D=0.60$

Note \*2 : Limited by maximum channel temperature.

Note \*3 :  $T_{ch} \leq 150^{\circ}\text{C}$ , See Fig.1 and Fig.2

Note \*4 : Starting  $T_{ch}=25^{\circ}\text{C}$ ,  $I_{AS}=3.3\text{A}$ ,  $L=198\text{mH}$ ,  $V_{DD}=60\text{V}$ ,  $R_G=50\Omega$ , See Fig.1 and Fig.2

$E_{AS}$  limited by maximum channel temperature and avalanche current.

Note \*5 :  $I_{SD} \leq 37.1\text{A}$ ,  $-di/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{DS \text{ peak}} \leq 600\text{V}$ ,  $T_{ch} \leq 150^{\circ}\text{C}$ .

Note \*6 :  $I_{SD} \leq 37.1\text{A}$ ,  $dV/dt \leq 30\text{V}/\text{ns}$ ,  $V_{DS \text{ peak}} \leq 600\text{V}$ ,  $T_{ch} \leq 150^{\circ}\text{C}$ .

■ Electrical Characteristics at  $T_{vj}=25^{\circ}\text{C}$  (unless otherwise specified)

## • Static Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V$ $I_D=250\mu A$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ $I_D=5.6mA$	3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=600V$ $V_{GS}=0V$ $T_{ch}=25^{\circ}\text{C}$	-	-	25	$\mu A$
		$V_{DS}=480V$ $V_{GS}=0V$ $T_{ch}=125^{\circ}\text{C}$	-	54	-	
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS}=0V$ $V_{GS}=\pm 30V$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V$ $I_D=18.6A$	-	0.073	0.084	$\Omega$
Gate resistance	$R_G$	f=1MHz, open drain	-	7.2	-	$\Omega$

## • Dynamic Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	$g_{fs}$	$V_{DS}=25V$ $I_D=18.6A$	12.5	25	-	S
Input Capacitance	$C_{iss}$	$V_{DS}=400V$	-	1950	-	$pF$
Output Capacitance	$C_{oss}$	$V_{GS}=0V$	-	67	-	
Reverse Transfer Capacitance	$C_{rss}$	f=250kHz	-	8.6	-	
Effective output capacitance, energy related (Note *7)	$C_{o(er)}$	$V_{DS}=0\ldots 400V$ $V_{GS}=0V$	-	160	-	$pF$
Effective output capacitance, time related (Note *8)	$C_{o(tr)}$	$V_{DS}=0\ldots 400V$ $V_{GS}=0V$ $I_D=\text{constant}$	-	660	-	
Turn-On Time	$t_{d(on)}$	$V_{DD}=400V, V_{GS}=10V$ $I_D=18.6A,$ $R_G=10\Omega$ See Fig.3 and Fig.4	-	25	-	ns
	$t_r$		-	97	-	
Turn-Off Time	$t_{d(off)}$		-	157	-	
	$t_f$		-	25	-	
Total Gate Charge	$Q_G$	$V_{DD}=400V, V_{GS}=10V$ $I_D=37.1A$ See Fig.5	-	93	-	nC
Gate-Source Charge	$Q_{GS}$		-	31	-	
Gate-Drain Charge	$Q_{GD}$		-	43	-	
Drain-Source crossover Charge	$Q_{SW}$		-	22	-	

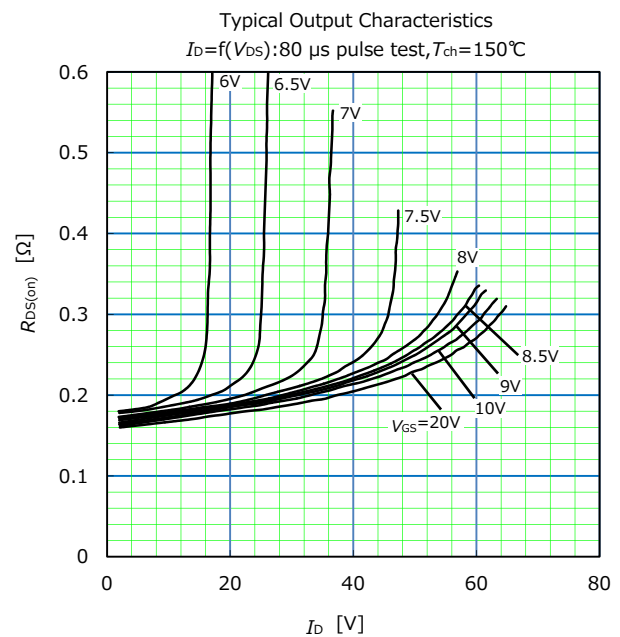
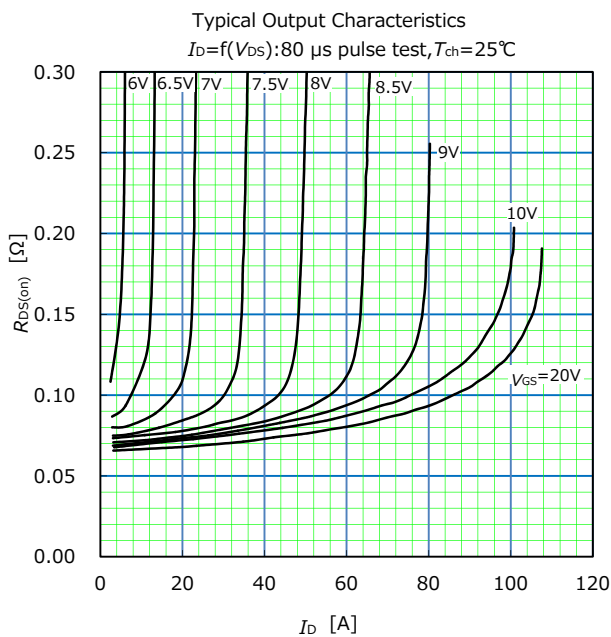
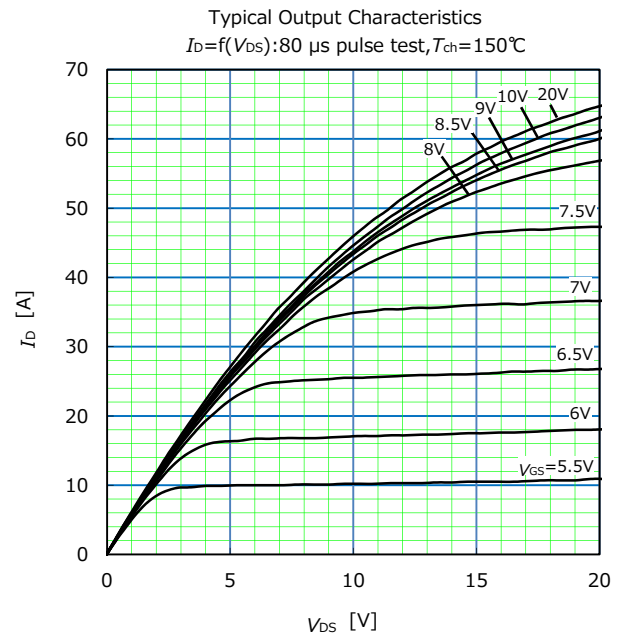
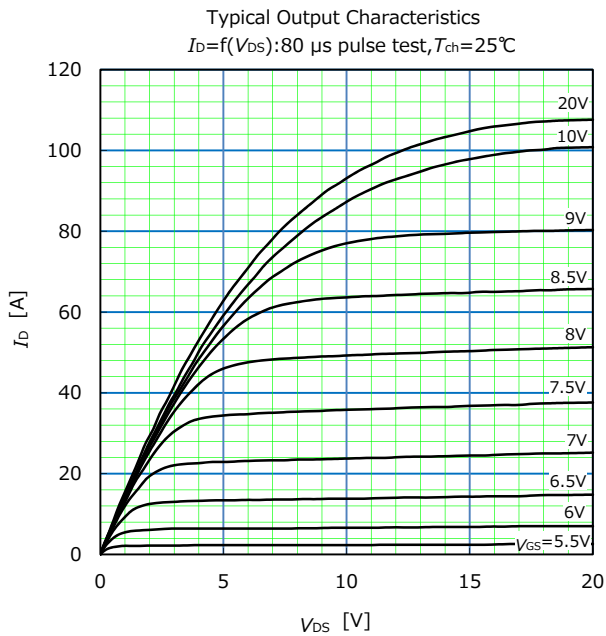
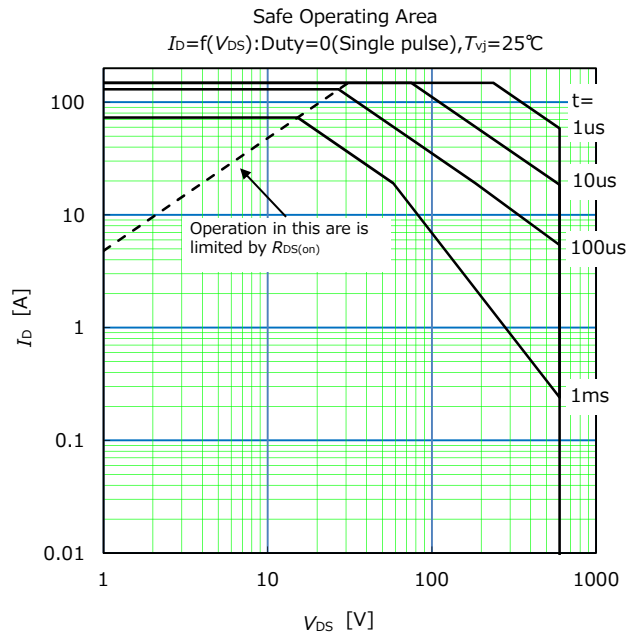
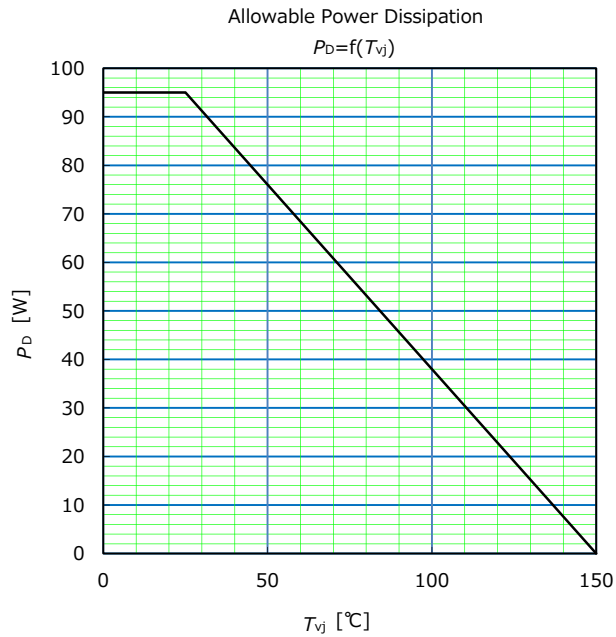
Note \*7 :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V.Note \*8 :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V.

## • Reverse Diode

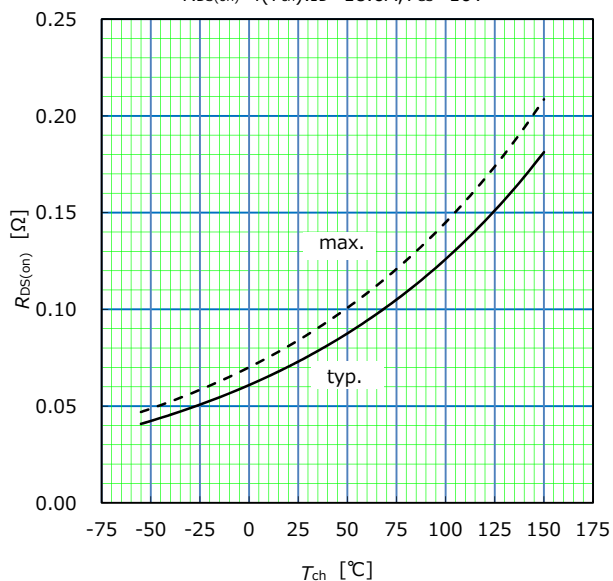
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	$V_{SD}$	$I_{SD}=37.1A, V_{GS}=0V$ $T_{ch}=25^{\circ}\text{C}$	-	0.95	1.35	V
Reverse Recovery Time	$t_{rr}$	$V_{DD}=400V, I_{SD}=37.1A$ -di/dt=100A/ $\mu s$ $T_{ch}=25^{\circ}\text{C}$ See Fig.6 and Fig.7	-	190	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	1.6	-	$\mu C$
Peak Reverse Recovery Current	$I_{rp}$		-	16	-	A

## ■ Thermal Resistance

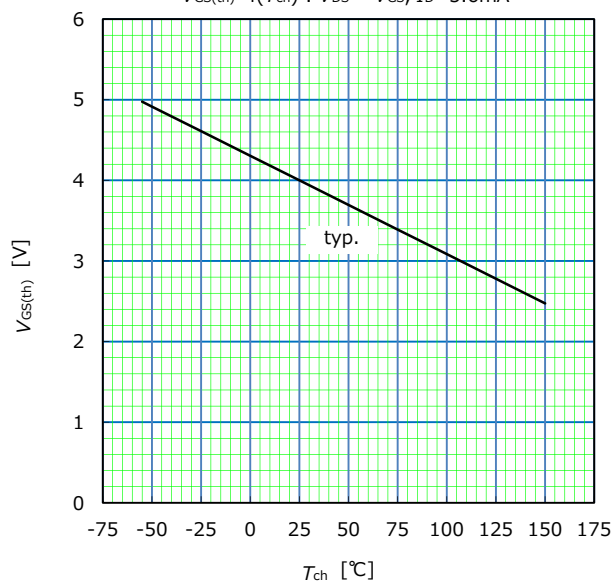
Parameter	Symbol	Min.	Typ.	Max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	1.316	$^{\circ}\text{C/W}$
Channel to Ambient	$R_{th(ch-a)}$	-	-	58	$^{\circ}\text{C/W}$



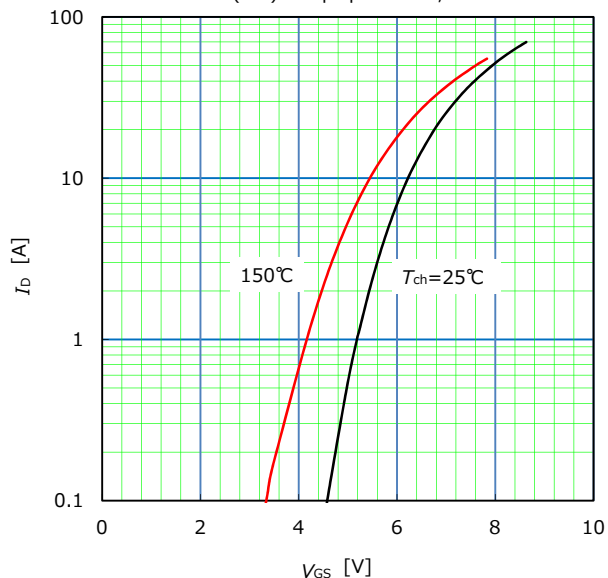
Drain-Source On-state Resistance  
 $R_{DS(on)} = f(T_{ch}) : I_D = 18.6A, V_{GS} = 10V$



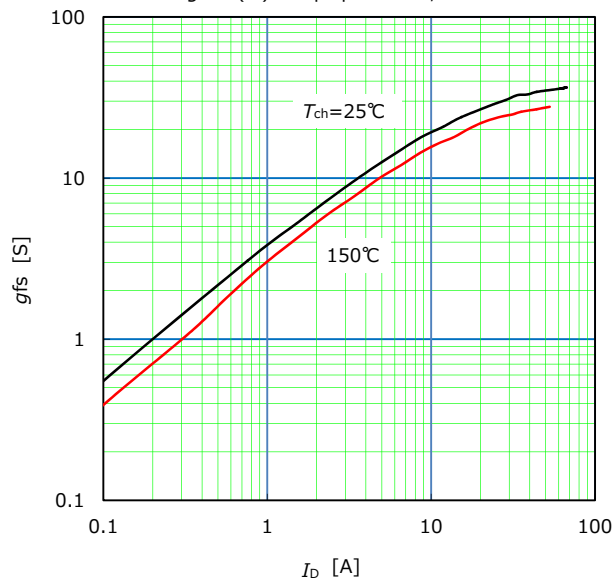
Gate Threshold Voltage vs.  $T_{ch}$   
 $V_{GS(th)} = f(T_{ch}) : V_{DS} = V_{GS}, I_D = 5.6mA$



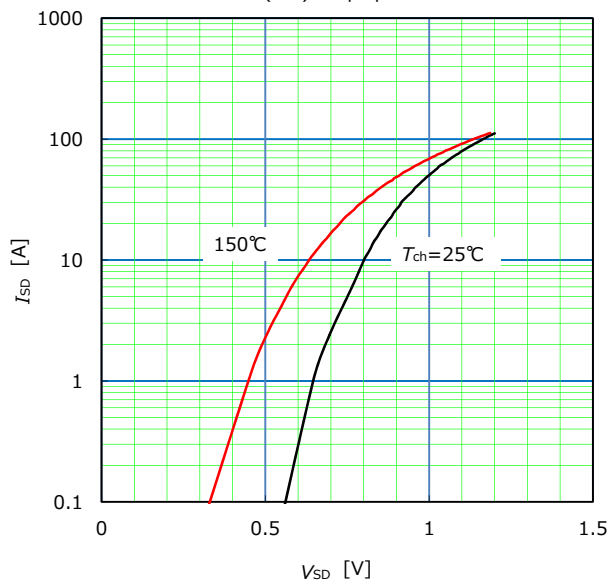
Typical Transfer Characteristic  
 $I_D = f(V_{GS}) : 80\mu s \text{ pulse test}, V_{DS} = 25V$



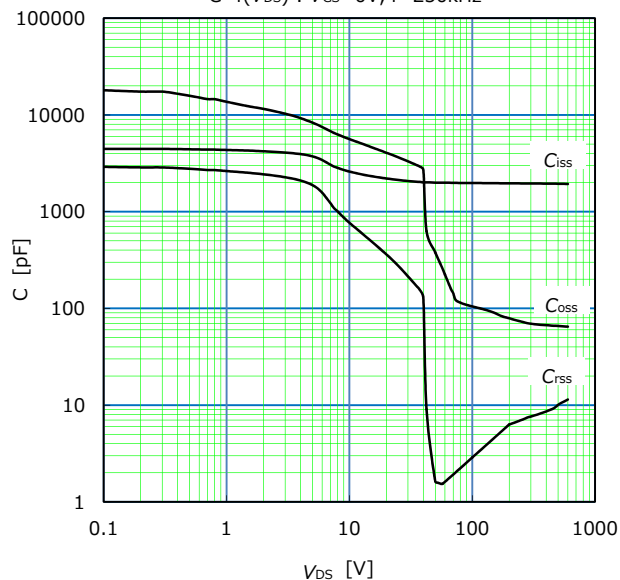
Typical Transconductance  
 $g_{fs} = f(I_D) : 80\mu s \text{ pulse test}, V_{DS} = 25V$



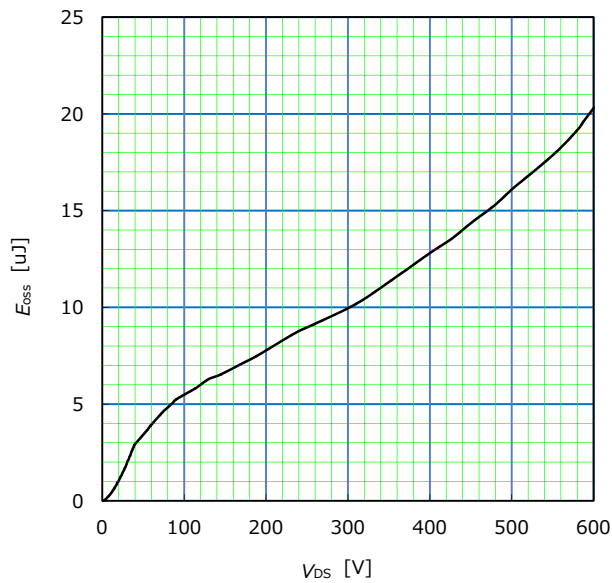
Typical Forward Characteristics of Reverse Diode  
 $I_{SD} = f(V_{SD}) : 80\mu s \text{ pulse test}$



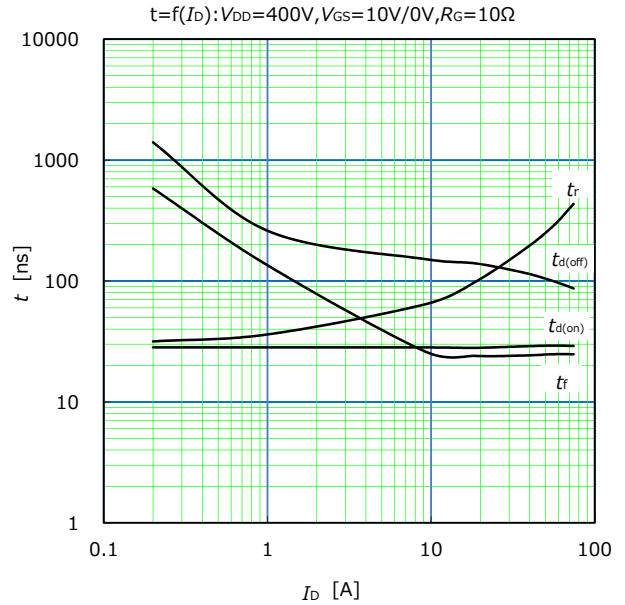
Typical Capacitance  
 $C = f(V_{DS}) : V_{GS} = 0V, f = 250kHz$



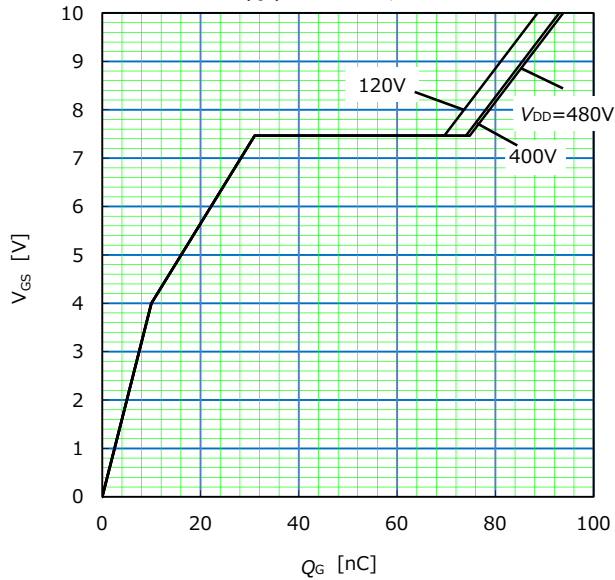
Typical  $C_{oss}$  stored energy



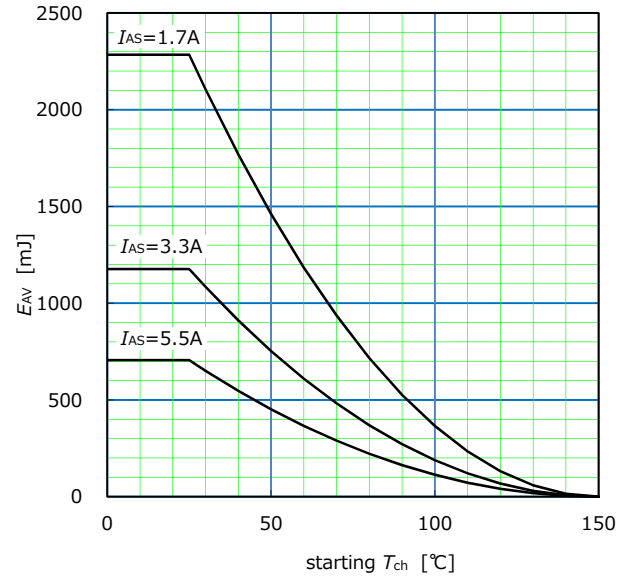
Typical Switching Characteristics vs.  $I_D$   $T_{ch}=25^\circ C$



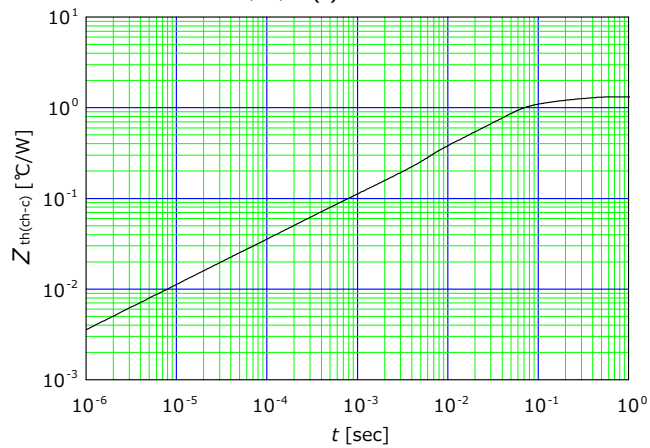
Typical Gate Charge Characteristics  
 $V_{GS}=f(Q_G) : I_D=37.1A, T_{ch}=25^\circ C$



Maximum Avalanche Energy vs. starting  $T_{ch}$   
 $E_{(AV)}=f(\text{starting } T_{ch}) : V_{CC}=60V, I_{(AV)} < 5.5A$



Transient Thermal Impedance  
 $Z_{th(ch-c)}=f(t):D=0$



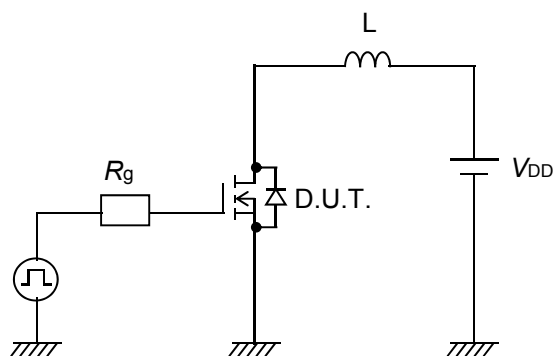


Fig.1 Avalanche Test circuit

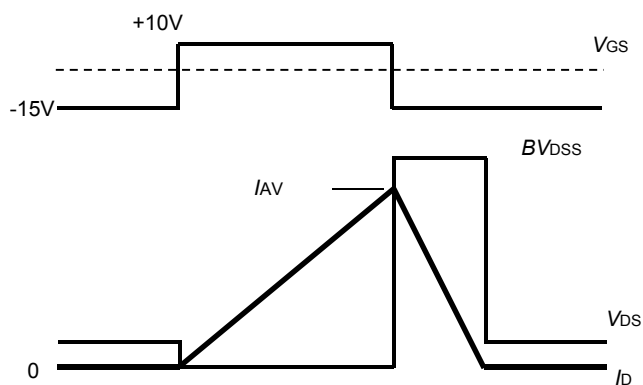


Fig.2 Operating waveforms of Avalanche Test

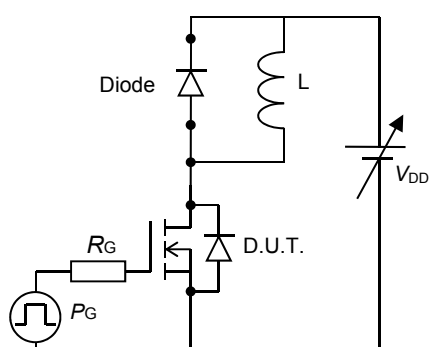


Fig.3 Switching Test circuit

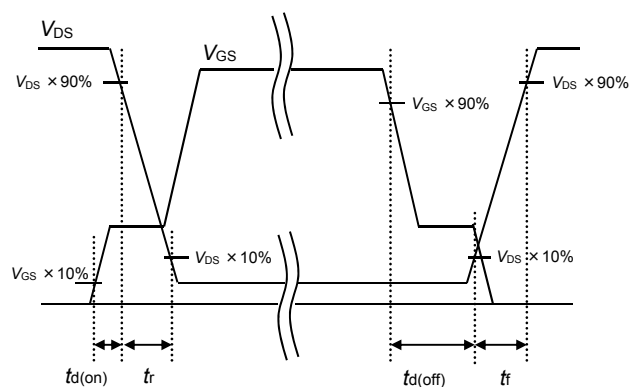


Fig.4 Operating waveform of Switching Test

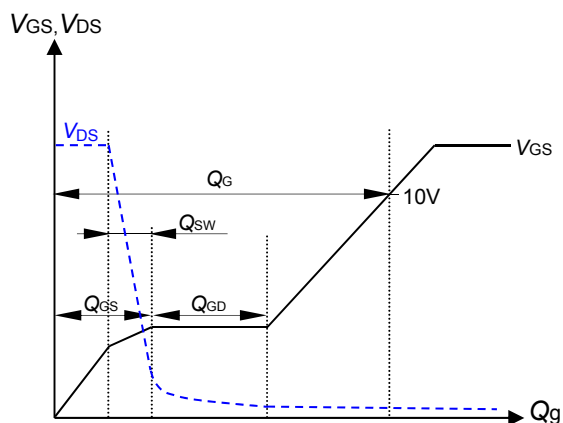


Fig.5 Operating waveform of Gate charge Test

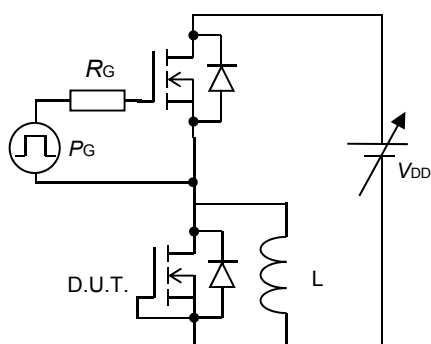


Fig.6 Reverse recovery Test circuit

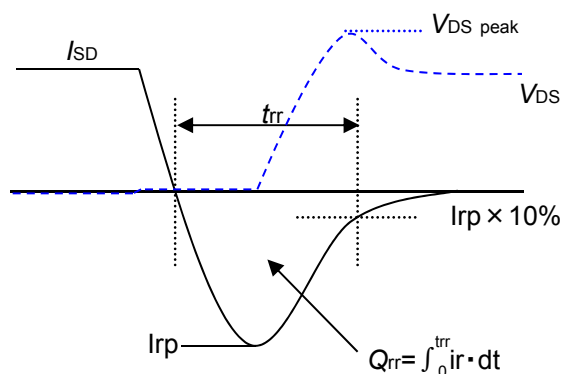
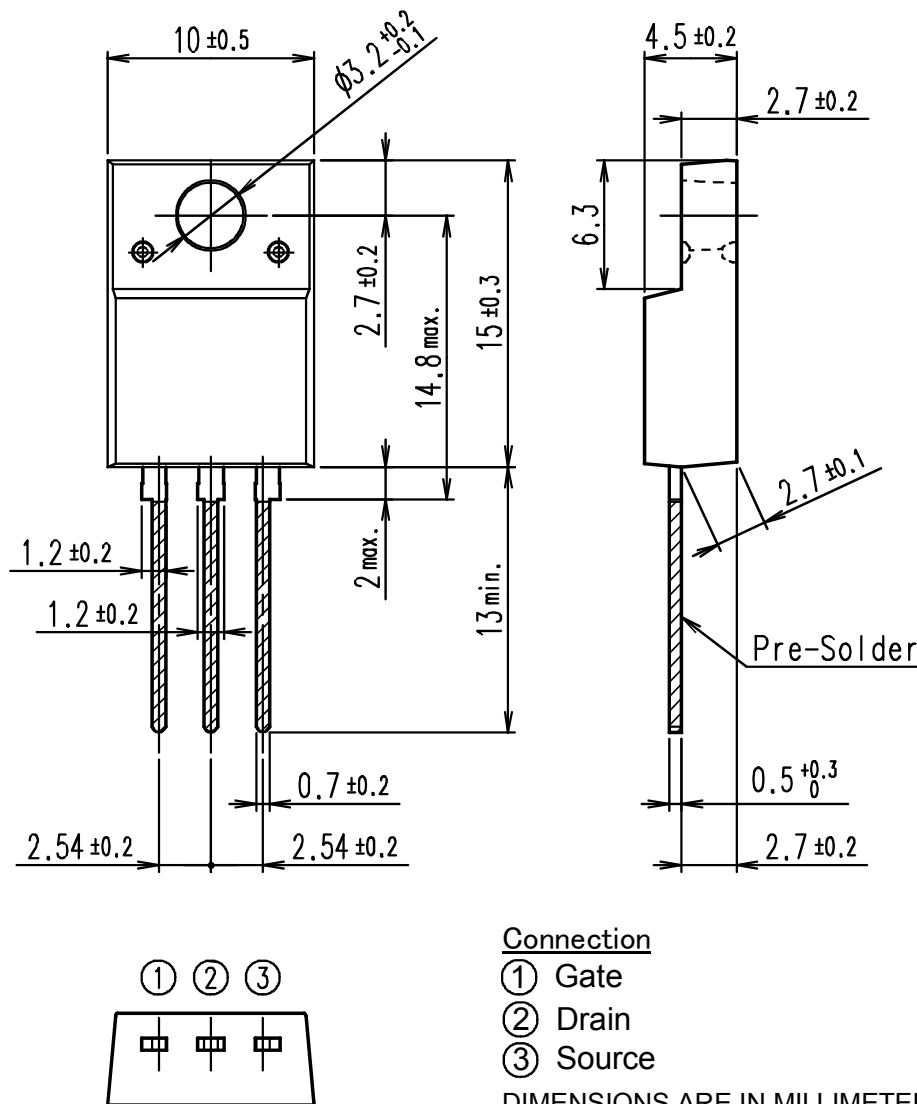
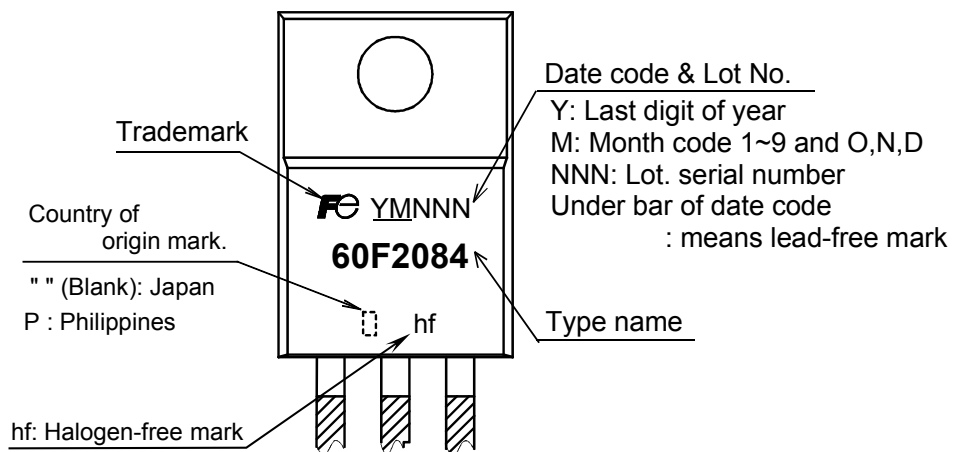


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-220F(SLS) Package



■ Marking



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