

**FMW60N027S2FDHF**

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FUJI POWER MOSFET

# Super J MOS<sup>®</sup> S2 series

## N-Channel enhancement mode power MOSFET

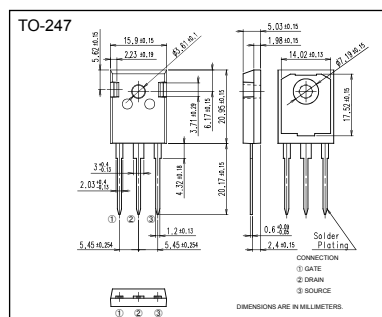
## ■ Features

Pb-free lead terminal  
RoHS compliant  
uses Halogen-free molding compound

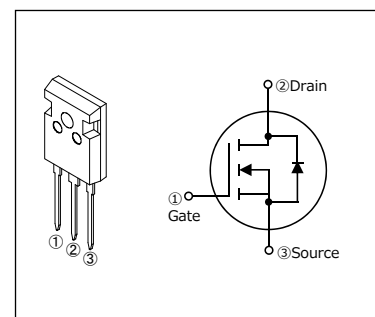
## ■ Applications

For switching

### ■ Outline Drawings [mm]



### ■ Equivalent circuit schematic



**■ Absolute Maximum Ratings at T<sub>c</sub>=25°C (unless otherwise specified)**

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V <sub>DS</sub>	600	V	
	V <sub>DSX</sub>	600	V	V <sub>GS</sub> =-30V
Continuous Drain Current	I <sub>D</sub>	95.5	A	Tc=25°C Note*1
		60.4	A	Tc=100°C Note*1
Pulsed Drain Current	I <sub>DP</sub>	286.5	A	Note *1
Gate-Source Voltage	V <sub>GS</sub>	±30	V	
Non-Repetitive Maximum Avalanche Current	I <sub>AS</sub>	8.5	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E <sub>AS</sub>	6074.3	mJ	Note *3
Maximum Drain-Source dV/dt	dV <sub>DS</sub> /dt	50	V/ns	V <sub>DS</sub> ≤ 600V
Continuous Diode Forward Current	I <sub>SD</sub>	95.5	A	Tc=25°C Note*1
		60.4	A	Tc=100°C Note*1
Pulsed Diode Forward Current	I <sub>SDP</sub>	286.5	A	Note *1
Peak Diode Recovery dV/dt	dV/dt	30	V/ns	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *5
Maximum Power Dissipation	P <sub>D</sub>	2.50	W	T <sub>a</sub> =25°C
		340		T <sub>c</sub> =25°C
Operating and Storage Temperature range	T <sub>ch</sub>	150	°C	
	T <sub>stg</sub>	-55 to +150	°C	

Note \*1 : Limited by maximum channel temperature.

Note \*2 :  $T_{ch} \leq 150^{\circ}\text{C}$ , See Fig.1 and Fig.2

Note \*3: Starting  $T_{ch}=25^{\circ}\text{C}$ ,  $I_{AS}=5.1\text{A}$ ,  $L=428\text{mH}$ ,  $V_{DD}=60\text{V}$ ,  $R_G=50\Omega$ , See Fig.1 and Fig.2

EAS limited by maximum channel temperature and avalanche current.

Note \*4:  $I_{SD} \leq 95.5A$ ,  $-di/dt \leq 100A/\mu s$ ,  $V_{DS\ peak} \leq 600V$ ,  $T_{ch} \leq 150^{\circ}C$ .

Note \*5:  $I_{SD} \leq 95.5A$ ,  $dV/dt \leq 30V/ns$ ,  $V_{DS\ peak} \leq 600V$ ,  $T_{ch} \leq 150^{\circ}C$ .

■ Electrical Characteristics at T<sub>c</sub>=25°C (unless otherwise specified)

## • Static Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	600	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =17.5mA	3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =600V V <sub>GS</sub> =0V T <sub>ch</sub> =25°C	-	-	25	μA
		V <sub>DS</sub> =480V V <sub>GS</sub> =0V T <sub>ch</sub> =125°C	-	150	-	
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V V <sub>GS</sub> = ± 30V	-	10	100	nA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V I <sub>D</sub> =47.8A	-	0.0235	0.0270	Ω
Gate resistance	R <sub>G</sub>	f=1MHz, open drain	-	2.7	-	Ω

## • Dynamic Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =25V I <sub>D</sub> =47.8A	45	90	-	S
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =400V	-	5500	-	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> =0V	-	193	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f=250kHz	-	21.2	-	
Effective output capacitance, energy related (Note *6)	C <sub>o(er)</sub>	V <sub>DS</sub> =0...400V V <sub>GS</sub> =0V	-	445	-	pF
Effective output capacitance, time related (Note *7)	C <sub>o(tr)</sub>	V <sub>DS</sub> =0...400V V <sub>GS</sub> =0V I <sub>D</sub> =constant	-	1950	-	
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =10V	-	38	-	ns
	t <sub>r</sub>	I <sub>D</sub> =47.8A, R <sub>G</sub> =5.6Ω	-	170	-	
Turn-Off Time	t <sub>d(off)</sub>	See Fig.3 and Fig.4	-	243	-	
	t <sub>f</sub>		-	25	-	
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =10V	-	256	-	nC
Gate-Source Charge	Q <sub>GS</sub>	I <sub>D</sub> =95.5A	-	79	-	
Gate-Drain Charge	Q <sub>GD</sub>	See Fig.5	-	130	-	
Drain-Source crossover Charge	Q <sub>SW</sub>		-	54	-	

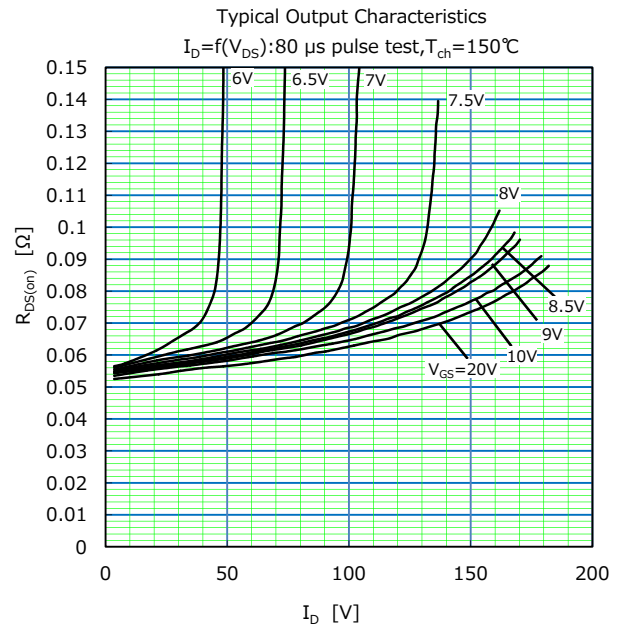
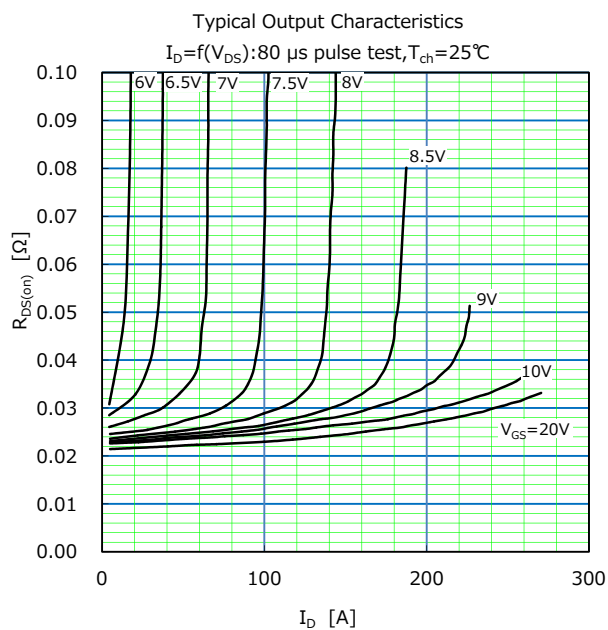
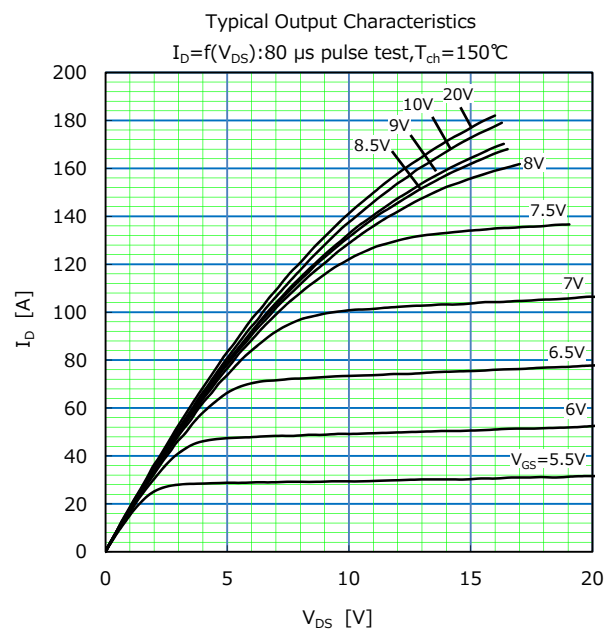
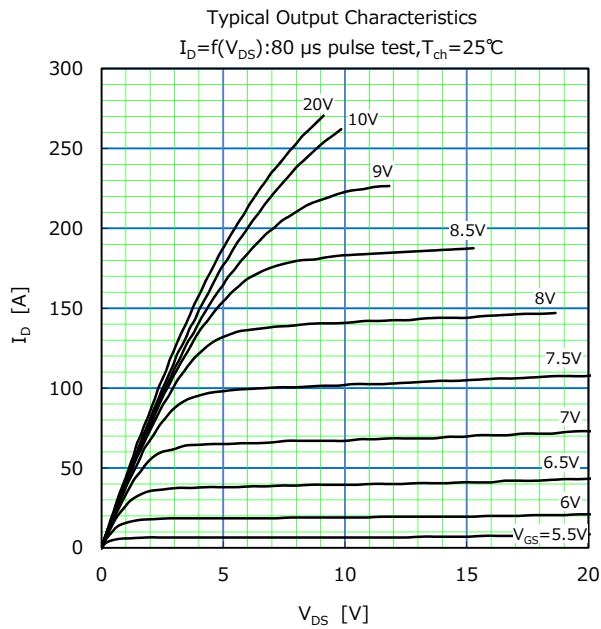
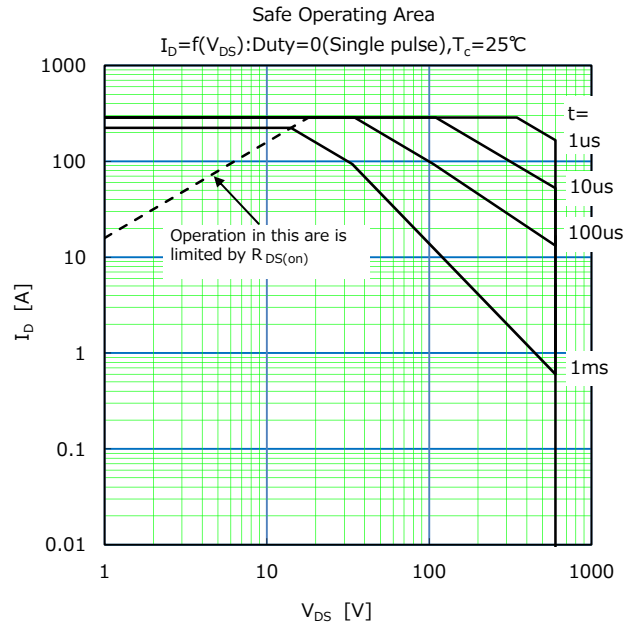
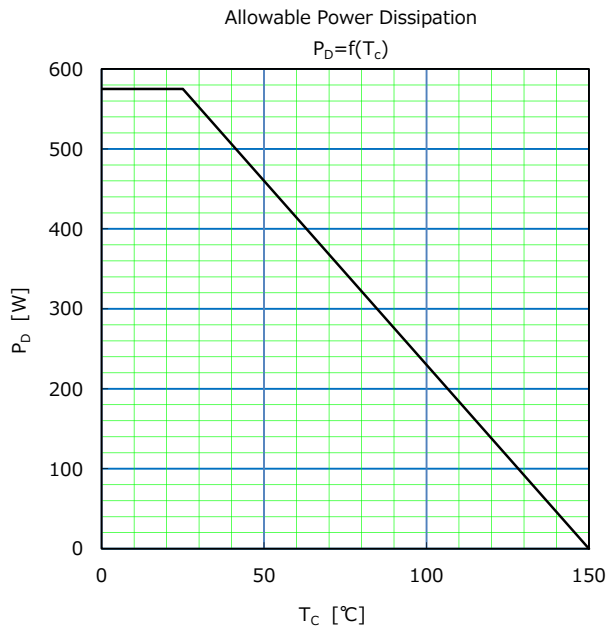
Note \*6 : C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 400V.Note \*7 : C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging times as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 400V.

## • Reverse Diode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	V <sub>SD</sub>	I <sub>SD</sub> =95.5A, V <sub>GS</sub> =0V T <sub>ch</sub> =25°C	-	0.95	1.35	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>DD</sub> =400V, I <sub>SD</sub> =95.5A	-	260	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	-di/dt=100A/μs T <sub>ch</sub> =25°C	-	2.9	-	μC
Peak Reverse Recovery Current	I <sub>rp</sub>	See Fig.6 and Fig.7	-	22	-	A

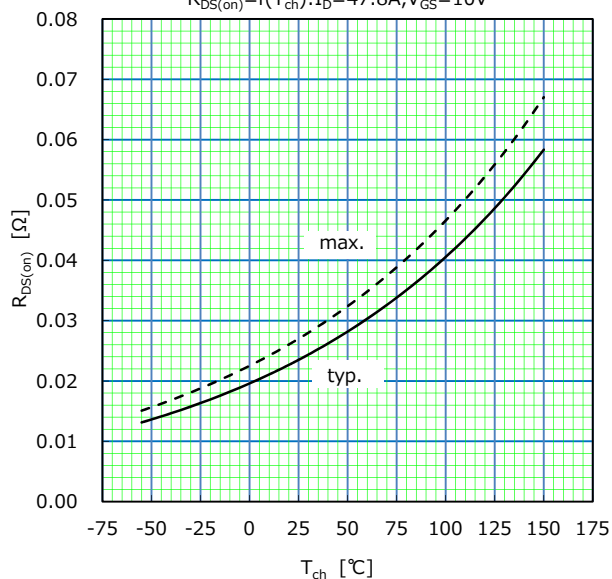
## ■ Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Channel to Case	R <sub>th(ch-c)</sub>	-	-	0.368	°C/W
Channel to Ambient	R <sub>th(ch-a)</sub>	-	-	50	°C/W

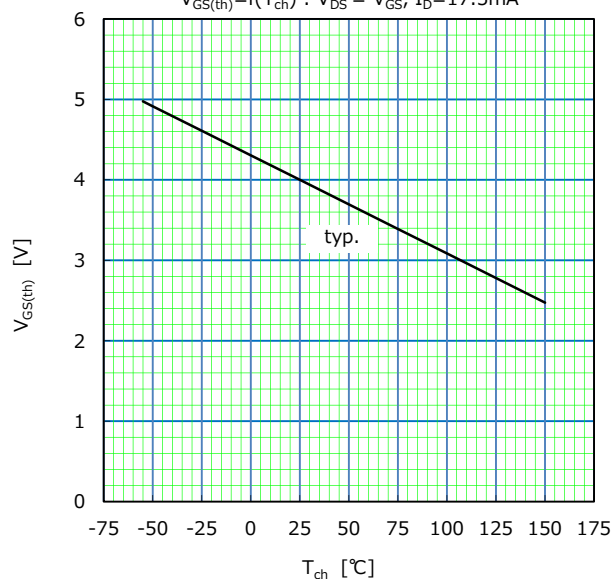


Drain-Source On-state Resistance

$$R_{DS(on)} = f(T_{ch}) : I_D = 47.8A, V_{GS} = 10V$$

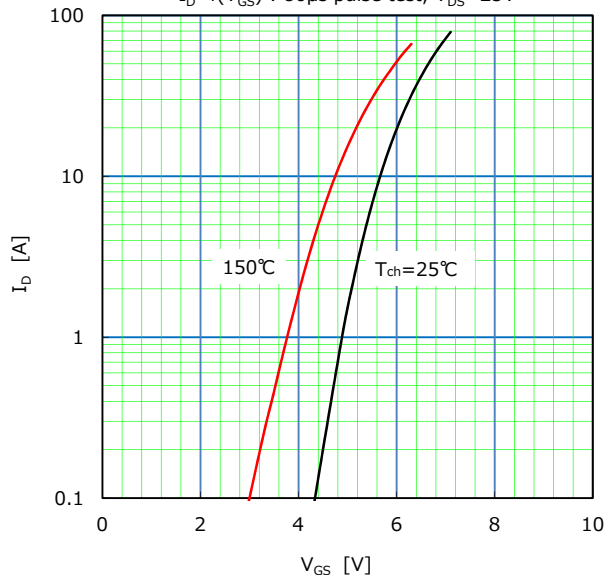
Gate Threshold Voltage vs.  $T_{ch}$ 

$$V_{GS(th)} = f(T_{ch}) : V_{DS} = V_{GS}, I_D = 17.5mA$$



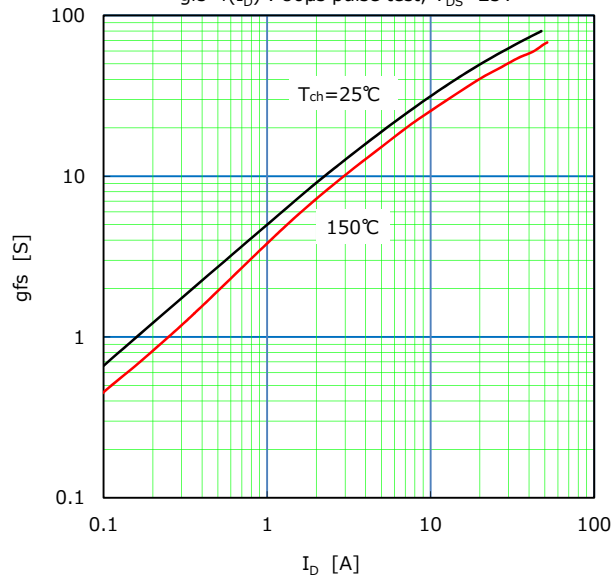
Typical Transfer Characteristic

$$I_D = f(V_{GS}) : 80\mu s \text{ pulse test}, V_{DS} = 25V$$



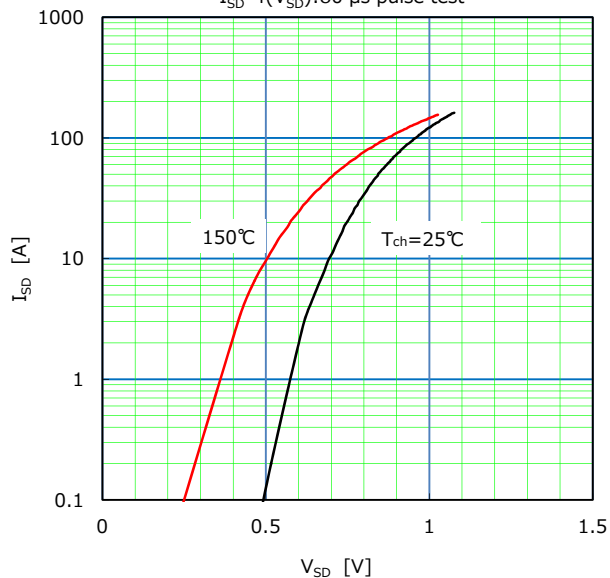
Typical Transconductance

$$g_{fs} = f(I_D) : 80\mu s \text{ pulse test}, V_{DS} = 25V$$



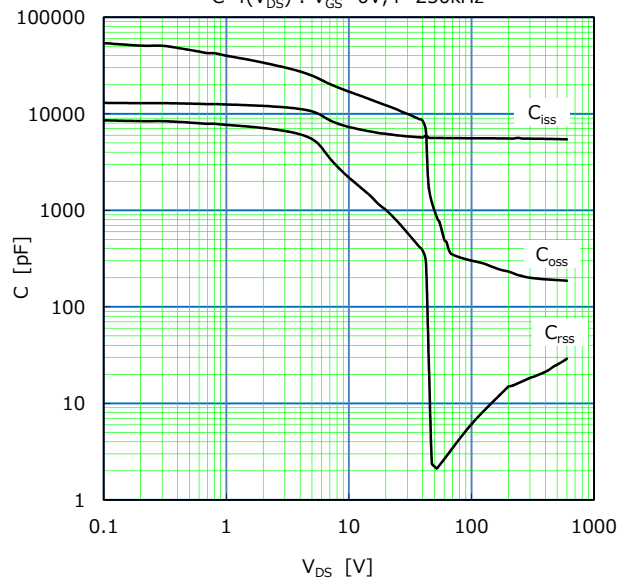
Typical Forward Characteristics of Reverse Diode

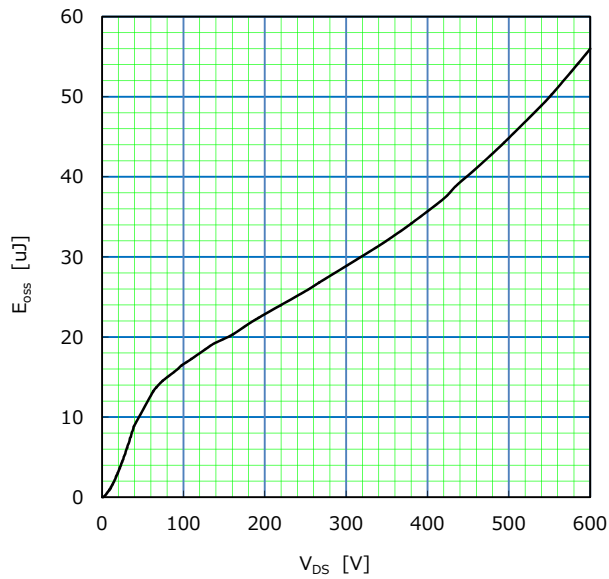
$$I_{SD} = f(V_{SD}) : 80\mu s \text{ pulse test}$$



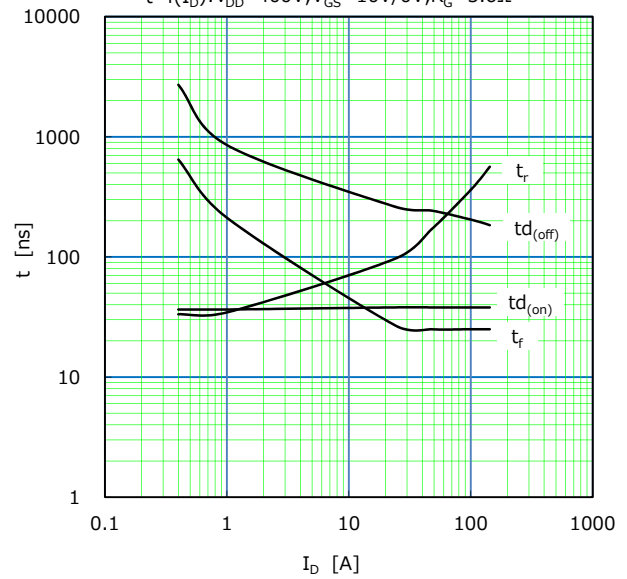
Typical Capacitance

$$C = f(V_{DS}) : V_{GS} = 0V, f = 250kHz$$



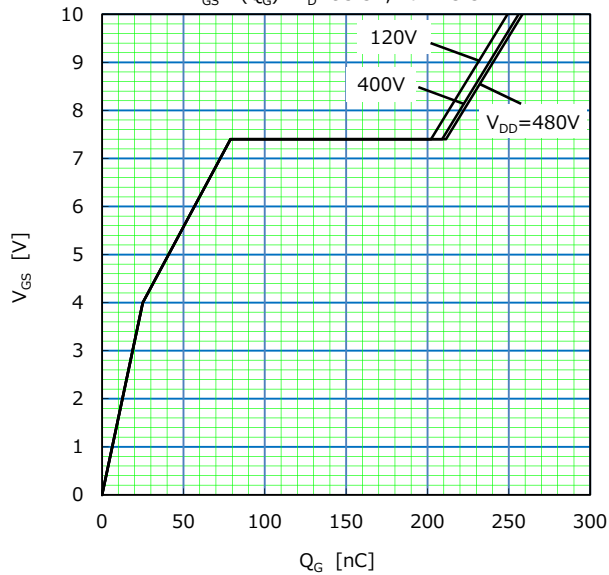
Typical  $C_{oss}$  stored energyTypical Switching Characteristics vs.  $I_D$   $T_{ch}=25^\circ C$ 

$$t=f(I_D): V_{DD}=400V, V_{GS}=10V/0V, R_G=5.6\Omega$$

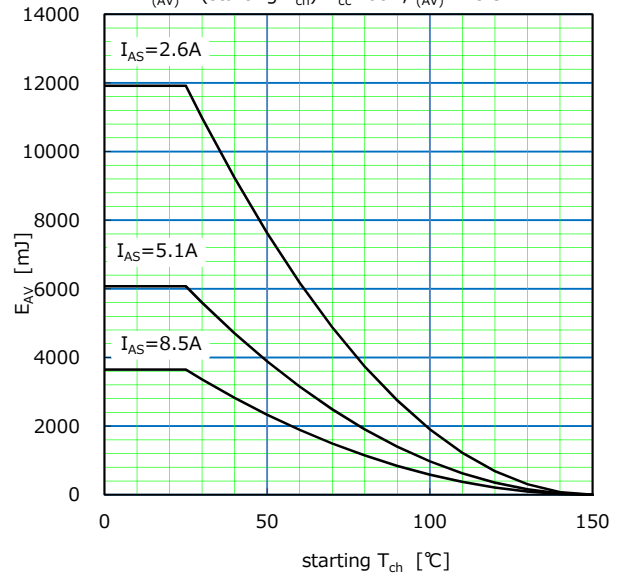


Typical Gate Charge Characteristics

$$V_{GS}=f(Q_G): I_D=95.5A, T_{ch}=25^\circ C$$

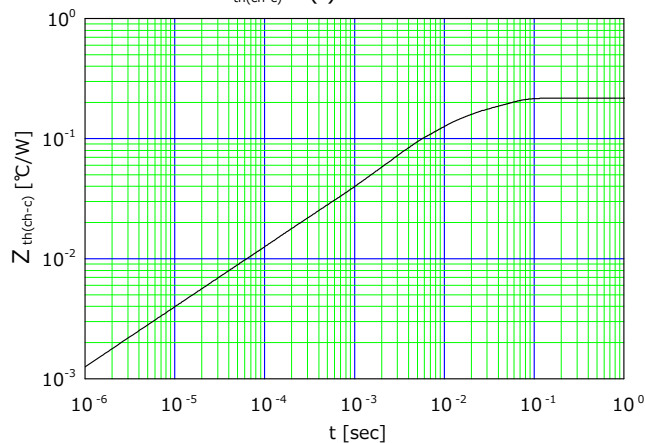
Maximum Avalanche Energy vs. starting  $T_{ch}$ 

$$E_{(AV)}=f(\text{starting } T_{ch}): V_{cc}=60V, I_{(AV)} \leq 8.5A$$



Transient Thermal Impedance

$$Z_{th(ch-c)}=f(t): D=0$$



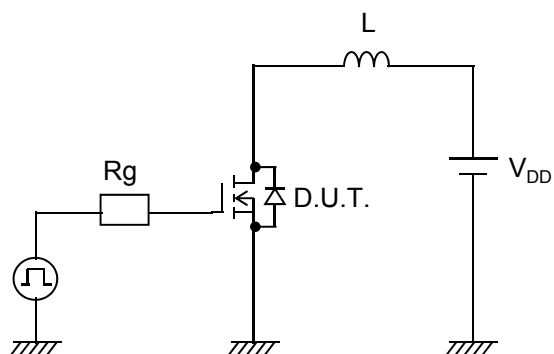


Fig.1 Avalanche Test circuit

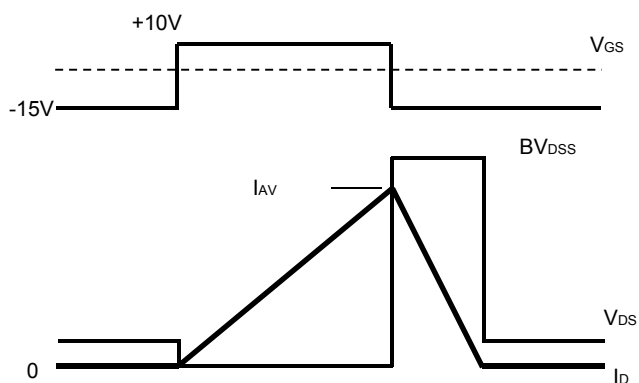


Fig.2 Operating waveforms of Avalanche Test

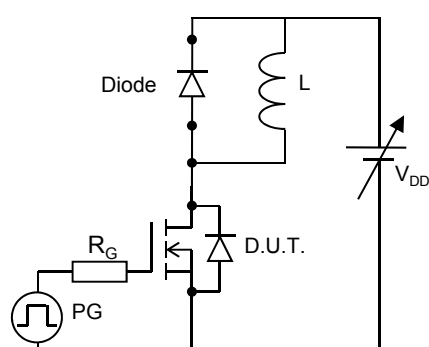


Fig.3 Switching Test circuit

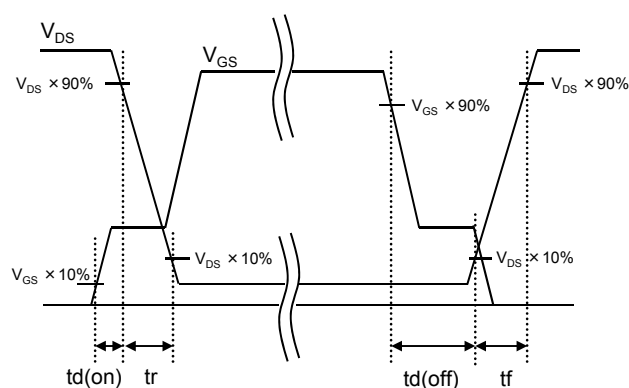


Fig.4 Operating waveform of Switching Test

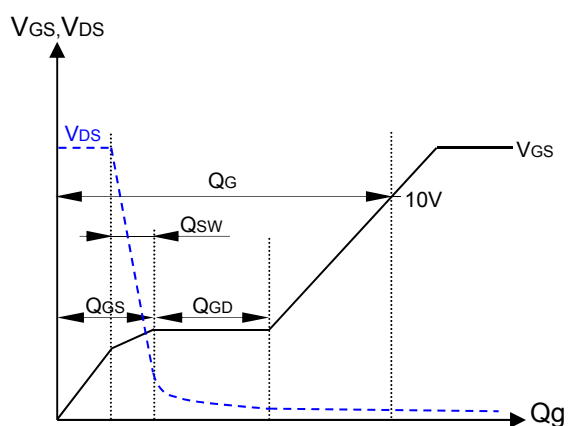


Fig.5 Operating waveform of Gate charge Test

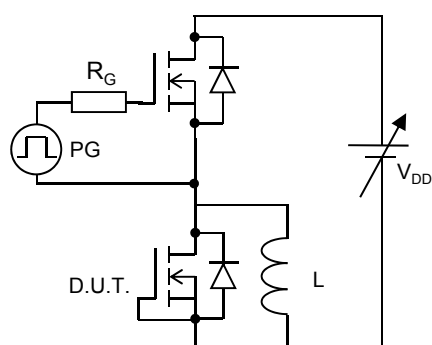


Fig.6 Reverse recovery Test circuit

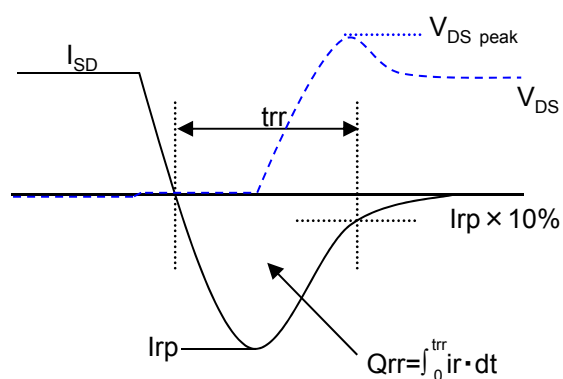
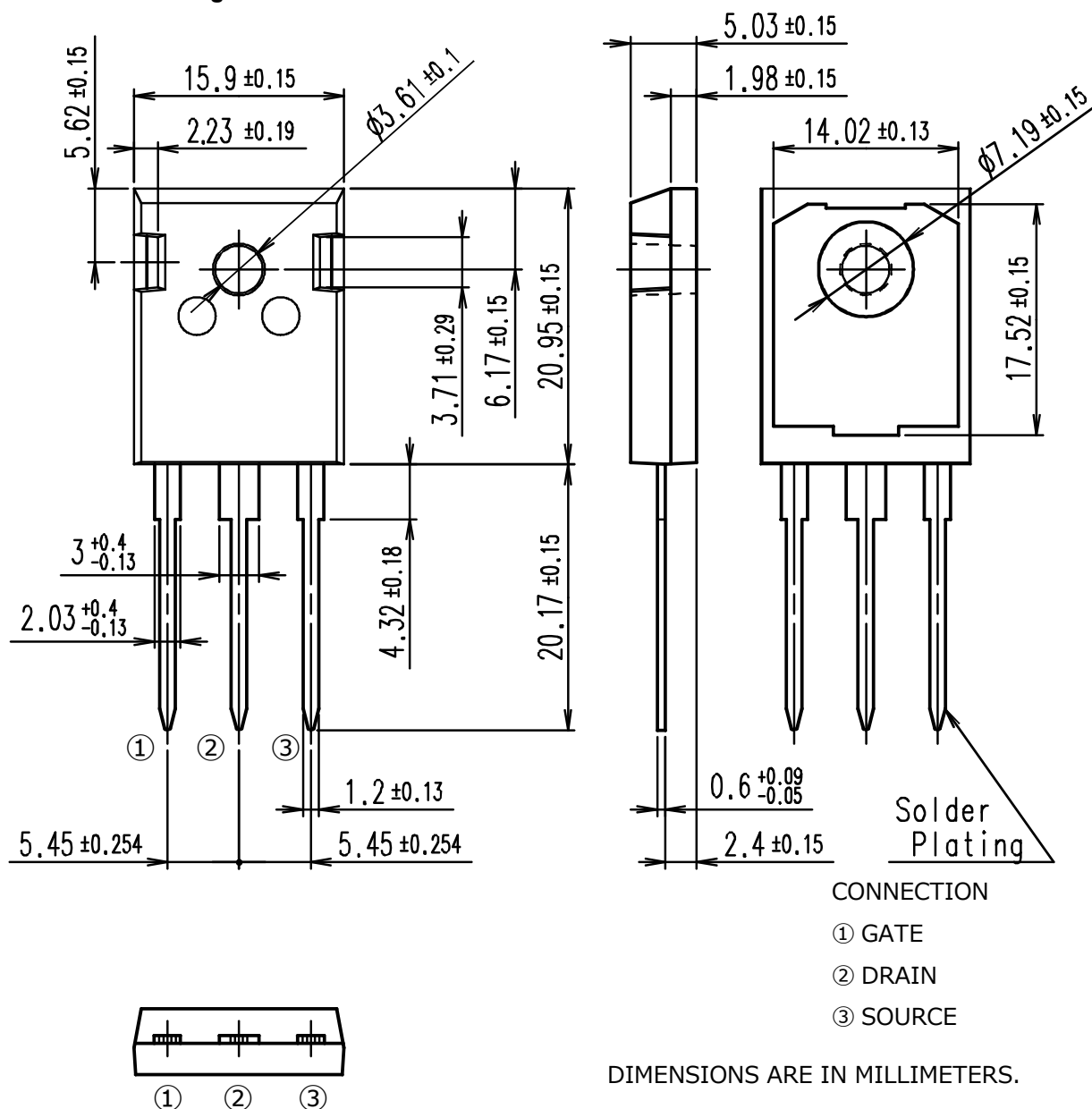
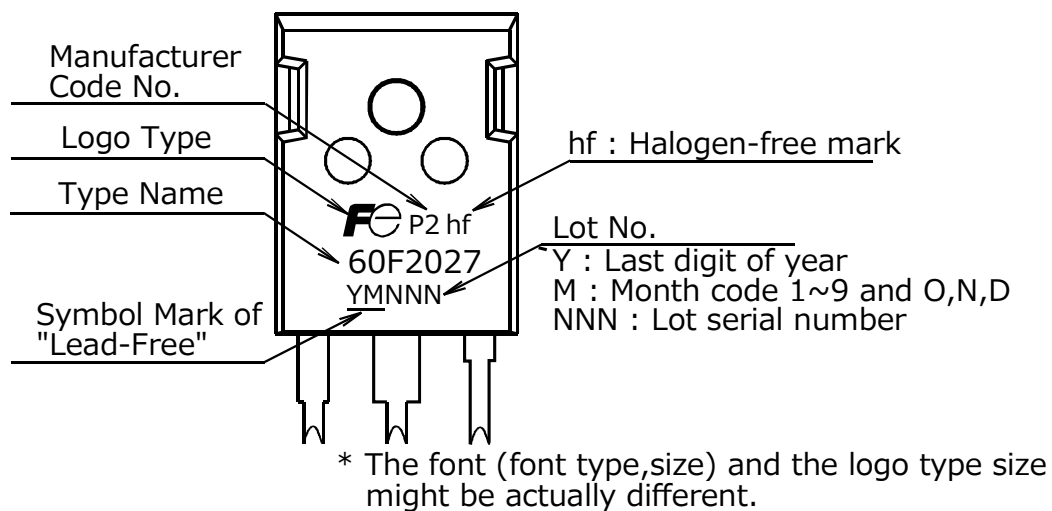


Fig.7 Operating waveform of Reverse recovery Test

# **Outview: TO-247 Package**



# **Marking**



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