2nd-Generation Low-Loss SJ-MOSFET "Super J MOS S2 Series"

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ABSTRACT

In order to use energy efficiently, there has been increasing demand for enhanced efficiency in power conversion equipment, and power metal-oxide-semiconductor field-effect transistors (MOSFETs) that are equipped with it have been required to be compact, low loss and low noise. Fuji Electric has developed the easy-to-use 2nd-generation low-loss SJ-MOSFET "Super J MOS S2 Series" that reduces on-resistance R_{on}·A, which is standardized by unit area, and improves the trade-off characteristic between turn-off switching loss E_{off} and the V_{DS} surge at turn-off switching. The adoption of this product is expected to improve the efficiency of power conversion equipment.

1. Introduction

In recent years, renewable energy sources such as photovoltaic power generation and wind power generation have been spreading against the background of global warming prevention and other concerns. On the other hand, energy consumption is increasing in the social infrastructure, automotive, industrial machinery, IT equipment and home appliance fields. In order to use energy more efficiently, power conversion technology has become of increasing importance. Various types of equipment have a power converter that uses semiconductor switching elements such as power metal-oxide-semiconductor field-effect transistors (MOSFETs). Such power converters are required to ensure high efficiency, high power density and low noise, and the semiconductor switching elements need to have characteristics of small size, low loss and low noise.

In order to meet such requirements, Fuji Electric developed the 1st-generation low-loss SJ-MOSFET "Super J MOS S1 Series" (S1 Series) in 2011. It achieved both low on-resistance and low switching loss by adopting a superjunction (SJ) structure and we have been establishing its product line[(1) to (3)].

This paper describes the 2nd-generation low-loss SJ-MOSFET "Super J MOS S2 Series" (S2 Series) that offers higher usability and improved conversion efficiency of power converters. This has been achieved by further improving the trade-off relationship between the withstand voltage of the element (BV_{DSS}) and the on-resistance normalized with a unit area (R_{on}・A) and through suppressing the V_{DS} surge at the time of turn-off switching.

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2. Design

2.1 Design policy

Improving the power conversion efficiency of a switching power supply requires a reduction in the conduction loss, switching loss and drive loss of the power MOSFET. There is a contradictory relationship among them: attempting to increase the switching speed and thus reduce the switching loss increases the V_{DS} surge at the time of turn-off switching, which generates noises and causes a malfunction. It is desirable to suppress the V_{DS} surge to 80% or less of the maximum rated voltage also in terms of reliability.

Consequently, we set the objective of developing the S2 Series to reduce the switching loss at turn-off (E_{off}) and suppress the V_{DS} surge and noises at the same time while reducing R_{on}・A so that it is lower than that of the conventional S1 Series.

2.2 Reducing the conduction loss

To reduce the conduction loss, we need to lower R_{on}・A. As Fig. 1 shows, the superjunction structure

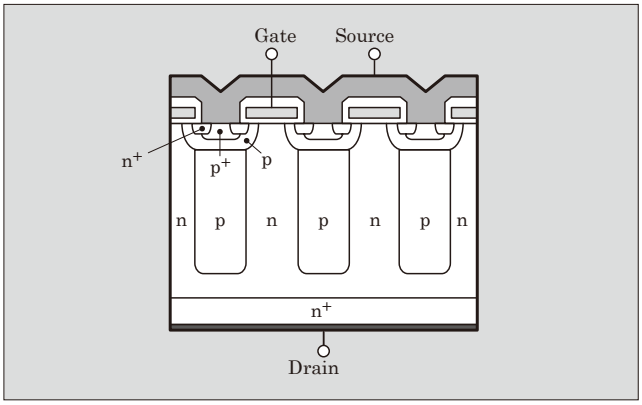

Fig. 1 Superjunction structure of SJ-MOSFET

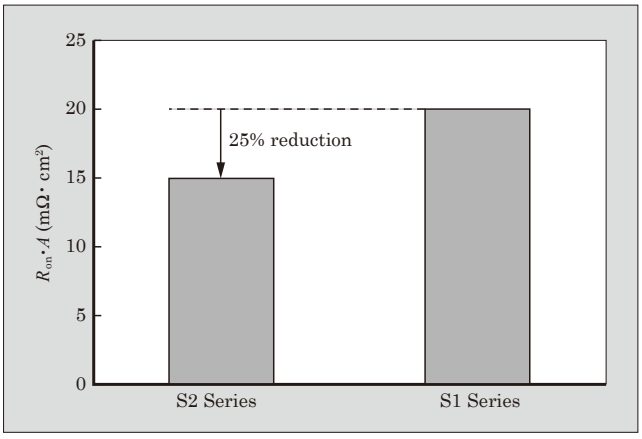

Fig. 2 R_{on}· A characteristics of 600-V rated products

has p-type regions and n-type regions arranged alternately in the drift layer. In this way, the depletion layers of p-n junctions connect horizontally when voltage is applied and a withstand voltage is provided on the entire surface[4 to 8].

To reduce R_{on} • A, we need to increase the impurity concentration of the n-type region to lower the resistance. For the S2 Series, we improved the impurity diffusion process and maintained a high impurity concentration in the n-type region to allow resistance to be reduced[9].

Figure 2 shows the R_{on} • A characteristics of the 600-V rated products of the S1 and S2 Series. We have reduced the resistance of the S2 Series by 25% to 15 mΩ • cm² from 20 mΩ • cm² of the S1 Series. As a result, in the TO-247 package, the S2 Series can mount up to 600-V/25.4-mΩ chips, whereas the S1 Series was limited to up to 600 V/40 mΩ.

2.3 Reducing the switching loss and suppressing the V_{DS} surge

We evaluated the power supply shown in Fig. 3 by mounting 600-V/70-mΩ products of the S1 and S2 Series in a MOSFET of a continuous conduction mode power-factor control circuit (CCM-PFC circuit). The conversion efficiency of the power supply against the external gate resistance R_g at 100-V input and

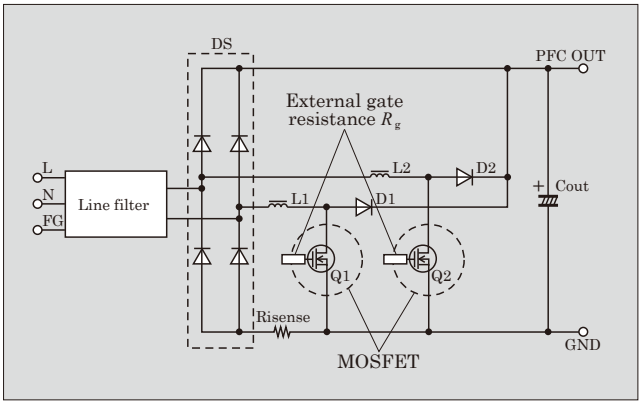

Fig. 3 CCM-PFC circuit of power supply

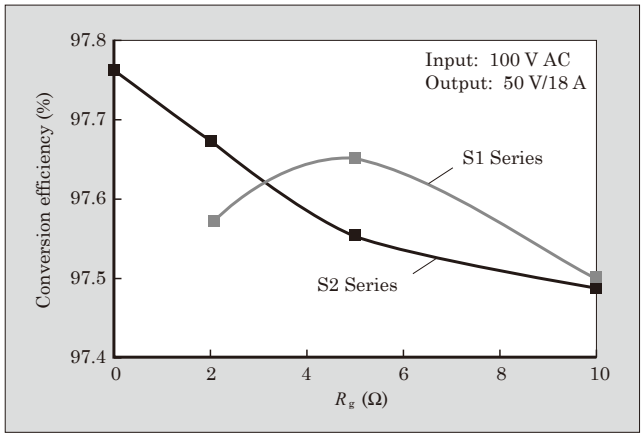

Fig. 4 Power supply conversion efficiency against external gate resistance R_g

50-V/18-A output is shown in Fig. 4. As the figure shows, the power supply efficiency normally increases when R_g is reduced. However, the efficiency decreases with the S1 Series. This is caused by erroneous ON due to the large wiring inductance of the source. In general, it is necessary to suppress such erroneous ON to prevent loss.

It is, however, impossible to eliminate the wiring inductance of the source completely because a power supply circuit is sometimes designed by reusing previous design patterns and its design is restricted by various factors such as the part layout. We thus took measures for the device so that we did not have to change the pattern design or parts circuit constant. The S2 Series attempts to suppress erroneous ON by increasing the threshold voltage $V_{GS(th)}$. For this purpose, increasing $V_{GS(th)}$ alone makes the turn-off speed faster. This might cause erroneous ON caused by gate vibration and the V_{DS} surge at turn-off switching. Therefore, we took measures including the optimization of $V_{GS(th)}$ and R_g.

Figure 5 shows the turn-off waveforms when R_g of the S1 and S2 Series is 2 Ω. Compared with the S1 Series, the S2 Series produces a smaller gate vibration and V_{DS} surge to suppress erroneous gate ON. This makes it possible to improve the power supply efficiency without changing the customer's R_g.

Figure 6 shows the trade-off characteristics between E_{off} and V_{DS} surge. When the V_{DS} surge is the same, the E_{off} value of the S2 Series is smaller than that of the S1 Series. This shows there is an improvement in the trade-off characteristic between E_{off} and V_{DS} surge. The S2 Series suppresses the V_{DS} surge and erroneous gate ON in this way. Figure 4 shows the conversion efficiency of a power supply against R_g when the S2 Series is mounted in the CCM-PFC circuit of the power supply. The S1 Series shows low conversion efficiency when R_g is small, but the S2 Series shows an improvement in the conversion efficiency when R_g is decreased.

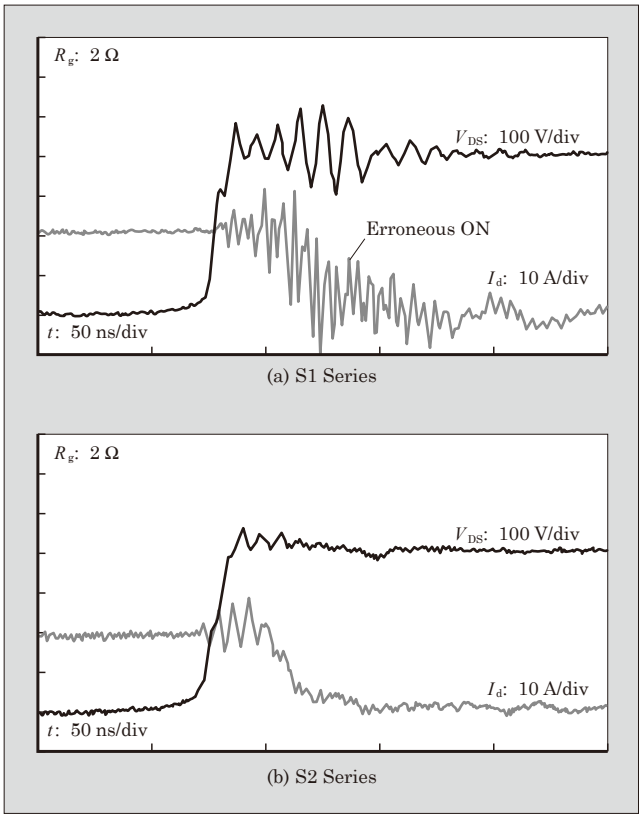

Fig. 5 Turn-off waveforms

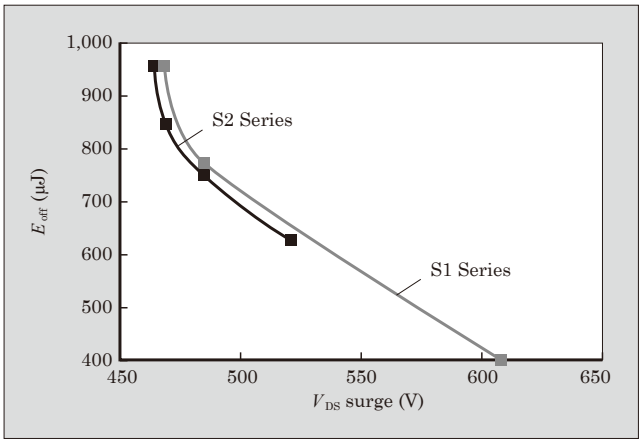

Fig. 6 E_{off}-V_{DS} trade-off characteristics

2.4 Reducing the loss under light load

When a light load is applied to a power supply, the current flowing in the MOSFET is small. Consequently, the proportion of the conduction loss in the total loss decreases. This results in an increase in the proportion of the drive loss and the loss generated when the output capacitance C_{oss} is charged/discharged (E_{oss}). We hence optimized the surface structure and reduced the total gate charge Q_g that is an index of the drive loss by approximately 30% compared with the S1 Series, achieving a reduction of $R_{on} \cdot Q_g$ by approximately 20%. Figure 7 shows the result of comparing Q_g between the S1 and S2 Series.

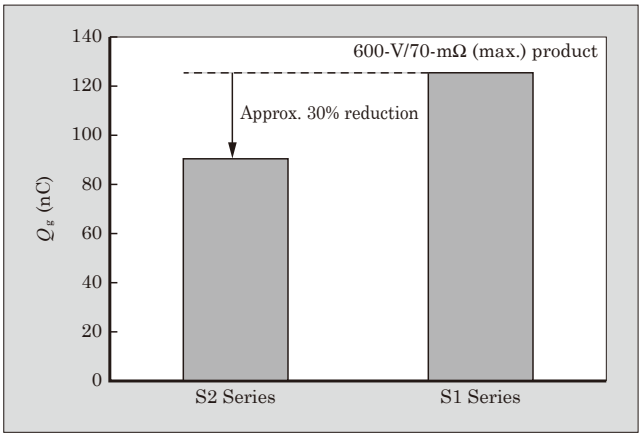

Fig. 7 Q_g characteristics

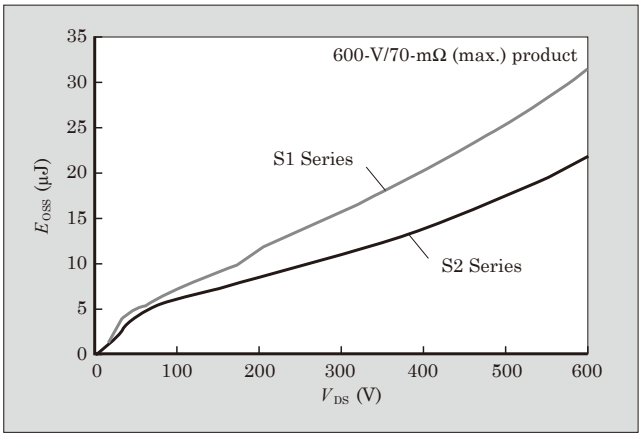

Fig. 8 E_{oss} characteristics

Figure 8 shows the result of comparing E_{oss} against V_{DS} between the S1 and S2 Series. When V_{DS} is 400 V, E_{oss} is approximately 30% less than that of the S1 Series.

3. Application Effect

We conducted a comparative evaluation by mounting the 600-V/70-mΩ products of the S1 and S2 Series in the CCM-PFC circuit of the power supply shown in Fig. 3 (see Fig. 9). The I/O conditions for the evalua-

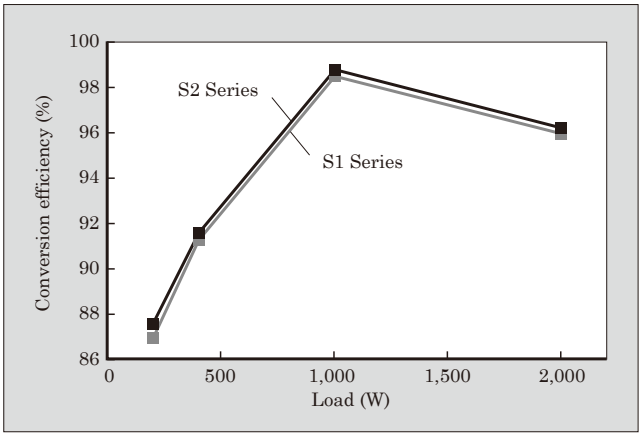

Fig. 9 Conversion efficiency−load characteristics

Table 1 Product lineup and major characteristics of “Super J MOS S2 Series”

V_{DS} (V)	$R_{DS(on)}$ max. (mΩ)	I_D (A)	Product lineup			
			TO-247 package 	TO-3P package 	TO-220 package 	TO-220F package 
600	25.4	95.5	FMW60N025S2	–	–	–
	40	66.2	FMW60N040S2	–	–	–
	55	49.9	FMW60N055S2	–	–	–
	70	39.4	FMW60N070S2	–	–	FMV60N070S2
	79	37.1	FMW60N079S2	–	FMP60N079S2	FMV60N079S2
	88	32.8	FMW60N088S2	–	FMP60N088S2	FMV60N088S2
	99	29.2	FMW60N099S2	–	FMP60N099S2	FMV60N099S2
	125	22.7	FMW60N125S2	–	FMP60N125S2	FMV60N125S2
	160	17.9	FMW60N160S2	–	FMP60N160S2	FMV60N160S2
	190	15.5	FMW60N190S2	FMH60N190S2	FMP60N190S2	FMV60N190S2
	280	10.4	–	FMH60N280S2	FMP60N280S2	FMV60N280S2
	380	8.1	–	–	FMP60N380S2	FMV60N380S2

tion includes input voltage of 200 V, output voltage of 53.5 V and R_g of 2 Ω. The S2 Series ensures higher efficiency than the S1 Series in the entire load region by suppressing erroneous ON by gate vibration, improving the trade-off characteristics between E_{off} and V_{DS} surge and reducing Q_g and E_{oss}. As a result, we can expect a power supply design offering higher efficiency and reliability by applying the S2 Series to a switching power supply.

4. Product Lineup

Table 1 lists the product lineup and major characteristics of the S2 Series. The lineup includes products rated at $R_{DS(on)}$ 25.4 to 160 mΩ for relatively large-capacity power supplies and those rated at 190 to 380 mΩ for small-capacity power supplies.

5. Postscript

The 2nd-generation low-loss SJ-MOSFET “Super J MOS S2 Series” is a product achieving both low power dissipation and V_{DS} surge suppression. The evaluation of a prototype mounted in a CCM-PFC circuit showed that the product could achieve higher efficiency than the conventional products. The developed device could make a great contribution to the efficiency improvement and miniaturization of switching power supplies.

In order to provide the better performance required by the market, we will continue to expand the lineup of high-breakage products and the products for high-speed switching of built-in diodes. At the same time, we will improve performances such as $R_{on} \cdot A$ reduction.

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