Simulation Technologies for Product Development: Current Status and Future Outlook

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1. Introduction

Along with the recent progress of computational science brought about by improved computer performance and software versatility, simulation technologies are now widely applied in various phases from R&D to product design.

At Fuji Electric, simulation technologies are applied in a wide variety of fields. For semiconductor devices, we are working to make use of molecular simulation and analysis technologies to clarify phenomena at the atomic level as well as analysis and estimation of electrical characteristics. In addition, we are taking an approach to use simulation technologies for clarifying material properties, which was something that mostly depended on rules of thumb in the past, to make efficient use of materials. Furthermore, approaches to achieving the optimum design of electrical equipment by taking advantage of simulation technologies such as electromagnetic noise analysis, acoustic noise analysis and fluid analysis are also becoming widespread.

In any case, we aim to provide customers with high-performance, high-reliability products with short delivery times. We will do this by making use of computational science to accurately identify physical phenomena, which form the basis of functions and performance of products, and grasping the mechanisms scientifically and quantitatively to apply them to the design of products.

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2. Simulation Technologies to Support Development of Devices and Materials

2.1 SiC power semiconductor devices

Simulation technologies, which are already being used to develop silicon (Si) devices, are also important in the development of silicon carbide (SiC)*1 devices. They are used to reduce the number of prototypes required, grasp physical phenomena and optimize the device structures to improve the development efficiency and offer higher-performance products.

SiC as a substrate material may have varying mobility, interface charges and the impact ionization rate depending on the crystal surface*2. Hence, it was difficult to have highly accurate prediction of device characteristics that are affected by them, including the on-state voltage, threshold and withstand voltage. To deal with this issue, Fuji Electric has collaborated in research with the National Institute of Advanced Industrial Science and Technology to build a simulation model based on the actual measured values to predict characteristics of a trench metal-oxide-semiconductor field-effect transistor (MOSFET)*3. We have also met the demands for energy saving and miniaturization of power electronics equipment and developed a low-loss 1.2 kV-class trench MOSFET (see Fig. 1). Trench MOSFETs have the gate formed on the sides of the trench and this allows cell pitch to be reduced more easily than planar MOSFETs and the on-resistance $R_{on}{\cdot}A$ is lower.

With trench MOSFETs, the a-face and m-face

***1: SiC**

A compound of silicon (Si) and carbon (C). With many structural polymorphisms of crystals existing such as 3C, 4H and 6H, SiC is known as a wide gap semiconductor with a band gap ranging from 2.2 to 3.3 eV depending on the structure. Because of its properties that are advantageous as power devices such as the high breakdown voltage and thermal conductivity, it is applied to practical applications for its capability to realize devices with high withstand voltage, low loss and high-temperature operation.

***2: Crystal surface**

Refer to Supplemental explanation 1: "SiC Crystal Types and Crystal Surface" on page 62.

***3: Trench MOSFET**

Trench metal-oxide-semiconductor field-effect transistor (MOSFET) is a type of power MOSFET. While planar MOSFETs have the gate formed on the semiconductor surface, trench MOSFETs are characterized by formation of the gate in a trench made in the direction of depth of the semiconductor. Because the channel is formed in the direction of depth, the trench gate structure allows easy planar miniaturization and hence improvement of the channel density, which makes it possible to reduce the on-resistance per area.

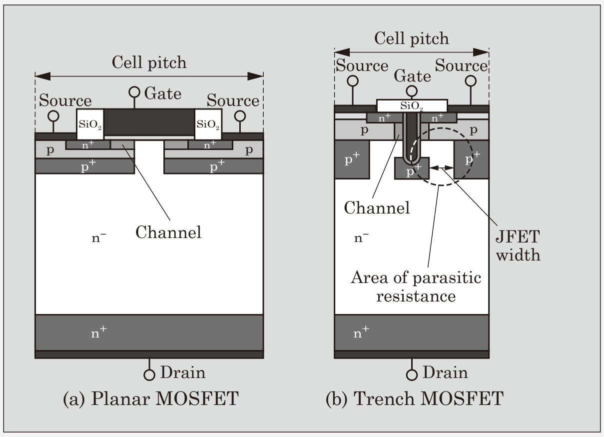


Fig.1 MOSFET cross-sectional view

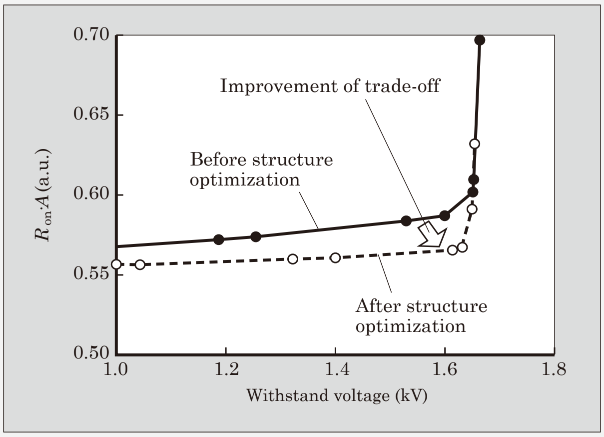


Fig.2 Trade-off between $R_{on}{\cdot}A$ and withstand voltage before and after structure optimization

are used for the trench sides and a model of mobility that accommodates these faces is required. Accordingly, we have focused on the fact that the device operates in the region that the mobility depends on the gate voltage and Coulomb scattering[*4]. We thus incorporated into simulation a Coulomb scattering model, allowing the mobility in low electric field to match the measured mobility. For withstand voltage, because the avalanche breakdown[*5] of SiC is affected by the lateral electric field in addition to the crystal surface, we used a Hatakeyama model, which takes the lateral electric field into consideration. And we have made corrections by the a-face and m-face to restructure the parameters. As a result, the simulated $R_{on}{\cdot}A$ and withstand voltage showed good agreement with the measured values. In addition, we confirmed that potential distribution analysis of $R_{on}{\cdot}A$ could be used to optimize the structure and the impurity concentration of the n-type layer in the junction field-effect transistor (JFET) portion. This made it possible to further improve the trade-off between $R_{on}{\cdot}A$ and withstand voltage (see Fig. 2) (Refer to "Simulation Based Prediction of SiC Trench MOSFET Characteristics" on page 12).

In addition to unipolar devices such as Schottky barrier diodes (SBDs)[*6] and MOSFETs, Fuji Electric has developed bipolar devices such as PiN diodes and insulated gate bipolar transistors (IGBTs)[*7]. Bipolar devices make it possible to easily increase the current and withstand voltage and we are currently conducting research on 13 kV PiN diodes and IGBTs. With bipolar devices, the mobility of electrons and holes, lifetime and the injection efficiency of carriers of the p-type collector greatly affect the device characteristics. However, these parameters, which may also be caused by crystal defects and activation rate of the p-type region, are difficult to apply to a simulation model. Accordingly, Fuji Electric has identified problems with real elements by using simulation to estimate ideal characteristics and comparing them with measured values. We have also attempted to improve the accuracy by fitting measured values to a simulation so as to improve the characteristics.

We combined a device simulator and a circuit simulator to conduct switching simulation in view of inductive load and predicted losses at a bus voltage of 6.6 kV. Figure 3 shows a comparison of the generated losses between the current and improved structures. The current structure has high injec-

***4: Coulomb scattering**

Refer to Supplemental explanation 2: "MOSFET Carrier Scattering" on page 62.

***5: Avalanche breakdown**

If reverse voltage is applied to a semiconductor device, free electrons and holes are accelerated in the electric field and collide with lattice atoms of silicon, etc. When the electric field intensity is sufficiently large, it causes collisional ionization. This results in repetition of the process of free electrons and holes being released and accelerated again and the number of free electrons and holes are increased like an avalanche to cause a large current to flow. This phenomenon is referred to as avalanche withstand and constitutes a factor that determines the breakdown voltage of a semiconductor device.

***6: SBD**

Stands for Schottky barrier diode. It is a diode providing rectifying action by using a Schottky barrier created by junction between a metal and a semiconductor. It is being applied to the FWDs of SiC-SBDs because of its excellent electrical characteristics. As compared with a P-intrinsic-N (PiN) diode, which also uses minority carriers, an SBD, which operates only on majority carriers, offers a higher reverse recovery speed and smaller reverse recovery loss.

***7: IGBT**

Stands for insulated-gate bipolar transistor. An IGBT is a voltage-controlled device that has a gate insulated with an oxide insulating film, the same gate structure as that of a MOSFET. It combines the strengths of a MOSFET and a bipolar transistor. Its bipolar operation, which allows use of conductivity modulation, makes it possible to realize both a switching speed sufficient for application to inverters and high withstand voltage combined with low on-resistance.

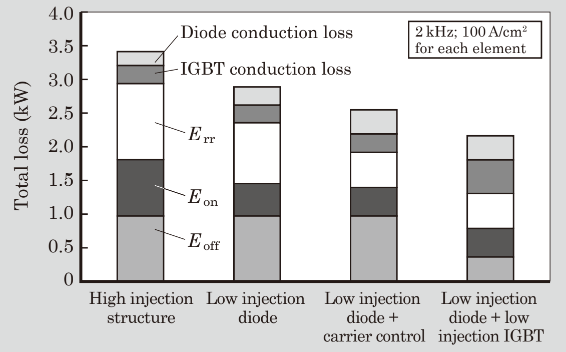


Fig.3 Results of estimation of losses with improved structure

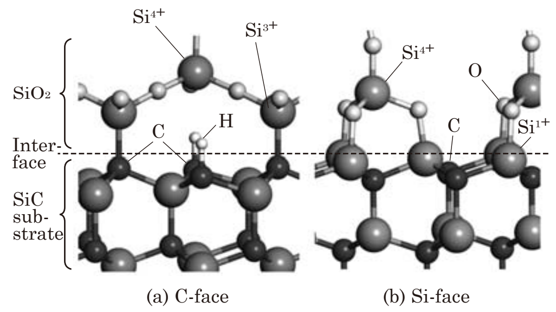


Fig.4 Estimated structural model of dry oxide film interface with ideal interface assumed

tion of carriers in the p-type collector and the p-type anode of the diode, which causes a large switching loss. Accordingly, we attempted to reduce the switching loss by incorporating a low-injection structure and other measures. As compared with the high-injection structure, a reduction to 44% has been confirmed in the switching loss and a 37% improvement in the total loss including the conduction loss at an operating frequency of 2 kHz (Refer to "Development of SiC Bipolar Devices Using Simulation" on page 17).

2.2 Clarification of MOSFET interface phenomena by first-principles calculation

The interface phenomena of SiC devices are still mostly unclear and the C (carbon) face, Si (silicon) face, a-face and m-face have different interface phenomena respectively. Accordingly, there are needs to clarify the interface phenomena for the respective face orientations. Currently, Fuji Electric is working on clarifying phenomena on interfaces and inside crystals at the atomic level by utilizing computational scientific techniques including the first-principles calculation in addition to using electrical characteristics and making analytical observations. The first-principles calculation is a technique of solving the electronic state in a substance based on quantum mechanics by using numerical calculations. It makes it possible to estimate properties of unknown substances and physical and chemical phenomena at the atomic level that cannot be measured by way of experiment.

Figure 4 shows an example of modeling by using first-principles calculation assuming the ideal interface structure of the SiC/SiO_2 interface after the dry oxidation process respectively for the C-face and Si-face. This leads to an estimation that Si existing on the interface is in the chemical state Si^{3+} on the C-face and Si^{1+} on the Si-face. X-ray photoelectron spectroscopy (XPS) analysis of the interface has actually shown Si^{3+} on the C-face and Si^{1+} on the Si-face, which supports the validity of this model. In this way, assuming the ideal interface structure makes it possible to estimate the origin of the suboxide (incomplete SiO_2) obtained by XPS analysis, and the choice of measures for realizing an ideal interface can be narrowed down.

The results of study of the interface structure with the ideal interface structure of the Si-face provided with a dangling bond (DB) of Si are shown in Fig. 5. The calculation shows that the interface state of the DB is formed in the band gap of SiC. An interface state like this traps a charge and causes a reduction in mobility due to Coulomb scattering, leading to a variation of V_{th}. A similar calculation of the bonding state of atoms other than the DB makes it possible to calculate various interface states. They can then be compared with the ac-

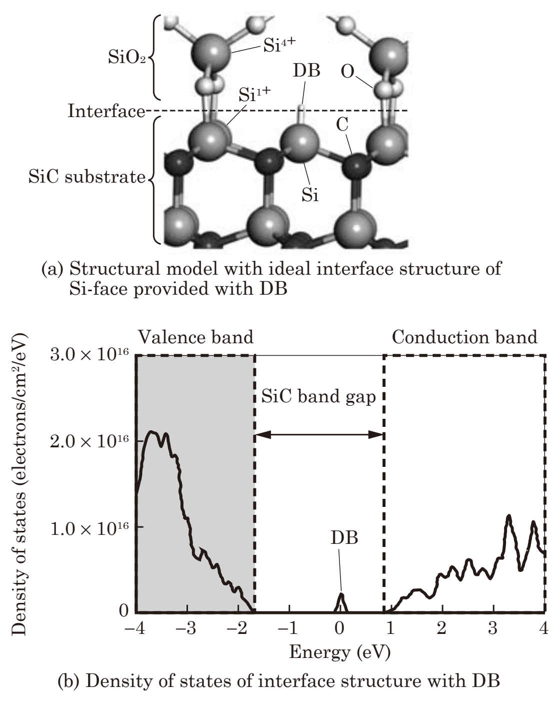


Fig.5 Results of study of interface structure with ideal interface structure of Si-face provided with DB

tual electrical characteristics and analysis results to clarify interface phenomena that are not actually visible.

In the future, we intend to make use of clarifying phenomena at the atomic level using a simulation including first-principles calculation in addition to measured values and analysis results. We will incorporate it in a device simulator, and thereby help to improve the performance of SiC-MOSFET (Refer to "Atomic Level Analysis of SiC Devices Using Numerical Simulation" on page 23).

2.3 Resin material characteristics

With products that use power semiconductor devices, it is important to improve the performance of semiconductor devices as well as the encapsulation resin. In particular, encapsulation resin has a significant influence on the long-term reliability. Therefore, resin materials must be selected in view of the impact of residual stress due to actual molding and the like. In order to meet this need, we are conducting simulation with resins modeled at the atomic level by first-principles calculation and molecular dynamics calculation. The aim is to grasp the mechanical characteristics and adhesion of resins so that a resin framework and adhesion aid can be selected. We are also working to gain an understanding of resin behavior. This is done with the resin flow and curing rate distribution during the actual molding process taken into consideration, by using 3D fluid analysis coupled with thermal stress analysis.

The adhesion between resin and metal may involve complicated factors. And the study of encapsulation resin conducted up to now has adopted a method of actually testing candidate materials so as to narrow down the choice. In order to improve the efficiency of this material selection, we are working on the development of technology to predict characteristics. It utilizes simulation technologies such as first-principles calculation and molecular dynamics calculation.

Adhesion of resin is assumed to depend mainly on the chemical bond between the component and resin, the anchor effect or presence of dirt on the surface and mechanical characteristics such as the coefficient of elasticity and coefficient of linear expansion of the resin. Of these, the anchor effect is a factor that depends on the component and the first thing to consider in design of the resin is the chemical bond between the component and resin and mechanical characteristics of the resin.

Mechanical characteristics of a resin and the chemical bonding force with the component to be adhered to can now be calculated from the molecular structure of the resin framework and adhesion aid. As shown in Fig. 6, energy in the state of adhesion between the base material and resin and that in the

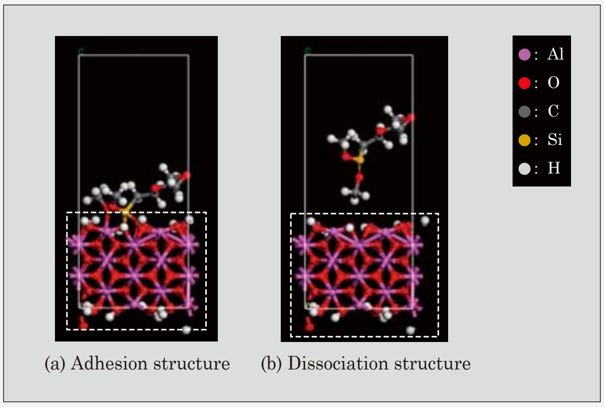


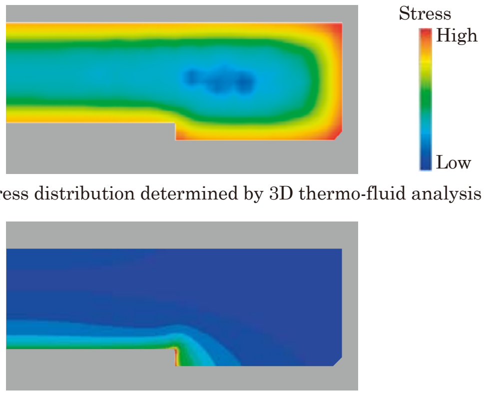
Fig.6 Molecular structures of epoxysilane and aluminum after structure optimization calculation

state of separation can be determined and the energy difference between them indicates the chemical bonding force in the ideal state. The actual adhesion can be estimated by using the chemical bonding force in this ideal state as the basis and considering external factors such as the anchor effect and dirt and the interfacial stress due to mechanical characteristics.

At this point, we are not ready to completely account for the measured values of adhesion from the results of simulation. But in the future, we aim to further improve the reliability of semiconductor modules encapsulated with resin by predicting characteristics including resin framework, adhesion aid and reliability (Refer to "Study of Adhesion of Resin Materials by Molecular Simulation" on page 28).

Computer-aided engineering (CAE) analysis, which has been used for structurally designing semiconductor modules up to now, handles resin cured after molding as a single elastic body without distribution. And it sometimes caused a deviation from the results of reliability evaluation. One possible factor in this is that, with actual resin moldings, a distribution is generated in the curing rate because of temperature unevenness during molding arising from the differences in the thermal conductivity, structure and heating method of the component. This causes residual stress due to a variation of the volume shrinkage factor depending on the location. Accordingly, for the purpose of improving the analytical precision of resin moldings, Fuji Electric has developed a simulation technology that takes into consideration the viscosity change due to heating and volume shrinkage behavior at the time of solidification from liquid.

By using 3D thermo-fluid analysis software, the irreversible change of resin from liquid to solid can be represented and, even for a product with a complicated shape, residual stress distribution can be visualized by performing a calculation from its heat distribution. This method takes into consideration the resin material properties including the density,



(a) Stress distribution determined by 3D thermo-fluid analysis

(b) Stress distribution determined by 3D finite element method structural analysis

Fig.7 Results of stress distribution analysis in resin curing

coefficient of elasticity and temperature dependence and shear velocity dependence of viscosity together with the curing reaction rate and heat of reaction of the resin. Figure 7 shows the stress distribution inside resin where a copper block is encapsulated with the resin, as an example of calculation results. The calculation result using the conventional 3D finite element method structural analysis software Fig. 7(b) shows a high stress region only on the boundary of the component. Meanwhile, Fig. 7(a) for 3D thermo-fluid analysis reflects the temperature distribution at the time of molding. It shows the presence of a high-stress region on the circumference of the resin rather than inside it, which is a result closer to the reality of the system. In this way, we are making it possible to conduct product development with even higher reliability by applying high-precision structural design (Refer to "Residual Stress Distribution and Adhesive Interface Strength Analysis of Thermosetting Resin Molding" on page 32).

3. Simulation Technologies to Support Development of Machinery and Equipment

3.1 Electromagnetic noise

Power electronics equipment is used at the core of equipment and facilities for energy conservation to ensure efficient use of electric energy and energy creation such as photovoltaic power generation and wind power generation. Power semiconductors used in power electronics equipment feature high-speed switching that allows electricity to be freely converted into easy-to-use forms. At the same time, however, they may emit large amounts of electromagnetic noise during operation.

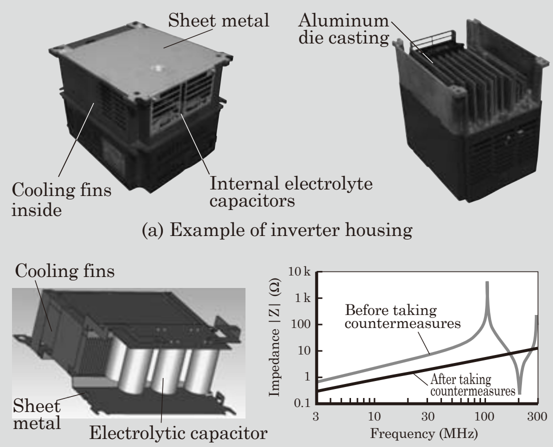
One traditional measure to reduce electromagnetic noise was to repeat cycles of trial and error after prototyping equipment. In contrast, at Fuji Electric, we have been developing electromagnetic noise simulation technologies for power electronics equipment. Our aim is to explore measures starting in the design phase, and such measures are being widely used for clarifying electromagnetic noise phenomena and reducing noise during product development.

Electromagnetic noise is generated as conduction noise if it is radiated outside through I/O cables and as emission noise if emitted as radio waves from various locations.

For simulation of conduction noise, rough analysis by a simplified model is performed in the initial stage of development. In later stages of development, detailed analysis by a more precise model and simulations with different levels of analytical precision according to the process are appropriately applied to product development.

For simulation of emission noise, simulation with part of the equipment extracted, rather than analysis of the entire equipment, is conducted and the results are applied to structural design (see Fig. 8). Such simulation with part of the equipment extracted features simple modeling and short analysis time, and it makes it possible to search for a better equipment configuration while analysis is repeated.

We are also working on simulation technology intended for preventing electromagnetic noise failure on sites where power electronics equipment is installed. The electromagnetic noise that is radiated through the grounding electrode when power electronics equipment is operated affects external equipment. Clarification of this mechanism and proposal of methods to reduce the noise is included in the fields that mainly depended on know-how without theoretical approaches taken up to now. We are expanding the scope of application of electromagnetic noise simulation in this area (Refer to "Electromagnetic Noise Simulation Technology for Power Electronics Equipment" on page 37).



(a) Example of inverter housing

(b) Modeling of ground potential (c) Analysis example

Fig.8 Housing analysis example

3.2 Aerodynamic noise

The demands for miniaturization of various types of electrical equipment have caused a tendency toward a yearly increase in the heat generation density of products. With air-cooled products that use fans, an increase in heat generation density causes the required air volume to increase as well, and aerodynamic noise generated from cooling air may become an issue.

At Fuji Electric, we are working on technology for simulating aerodynamic noise to gain an understanding of the mechanism of noise generation. This can be done by visualizing flow and pressure change, which becomes a source of aerodynamic noise, and studying the structure for noise reduction.

For simulation of aerodynamic noise, we have realized estimation of variation in the flow that provides a source of noise and the sound level by calculation of the flow of a fan (see Fig. 9) with massively parallel computing by using large eddy simulation (LES), which is capable of high-precision reproduction of turbulence phenomena.

Use of this simulation has made it possible to estimate the peak frequency and sound pressure level for noise arising from rotation of the vanes of a cooling fan and flow around the casing. In addition, we have confirmed that the tendency of noise being caused by the positional relationship between a cooling fan and the surrounding structure can be reproduced through comparison with a model simulating an air cooling structure of power electronics equipment. At present, we are working to apply this simulation to a study on a design for reducing the noise of products (Refer to “Aerodynamic Noise Simulation Technology for Developing Low Noise Products” on page 42).

3.3 Switchgear internal arcs

In the development of switching devices used for power transmission, reception and distribution systems, arc analysis for predicting performance at the time of current cutoff has been used mainly to quantify phenomena in the vicinity of contacts up to now. For example, such analysis has been used to predict arc elongation and movement in the breaking chamber of low-voltage equipment. The results are then used to determine the structure and arrangement of arc extinguishing grids in order to reduce wear of contactors and improve breaking performance. For high-voltage circuit breakers, the analysis has been used for insulation design by predicting the reduction in dielectric strength due to a decrease in gas density of the high-temperature gas that is generated by arc heat generation and that diffuses inside.

For improving the analytical precision, modeling relating to the atmospheric gas generated by temperature increase to a few thousand Kelvin of the arc generated between contacts in view of complicated physical phenomena including dissociation and ionization is essential. Fuji Electric has applied this technology to develop design technology for ensuring safety in the event of arc fault inside switchgears. To switchgear for overseas markets, an IEC standard (IEC 62271-200) is applied. This standard contains strengthened approaches to safe structures such as classification of structures relating to operation continuity during failure and maintenance and classification relating to protection of people in the surrounding areas, which has made development of new technology necessary in order to meet these requirements. One major issue is to avoid increase in analysis time due to expansion of the analysis domain and increase of computational load in relation to prediction of pressure rises in the event of internal arc faults, which required reconsideration of the analysis method. To that end, we aimed to realize both reduced computation time and ensured analytical precision and measured the behavior during pressure relief operation, which involves high computational load, and reflected the results to analysis, thereby developing an analysis method specialized in prediction of pressure rises in the event of in-

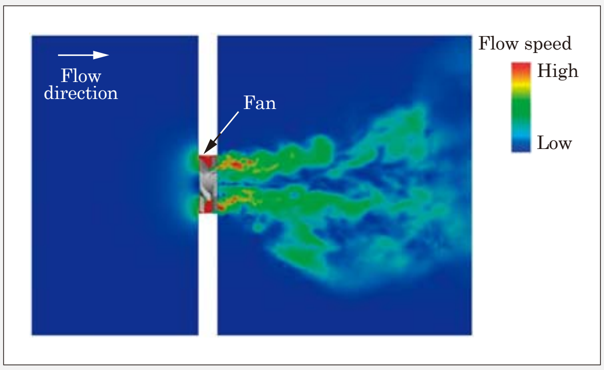


Fig.9 Fan flow speed distribution (instantaneous value)

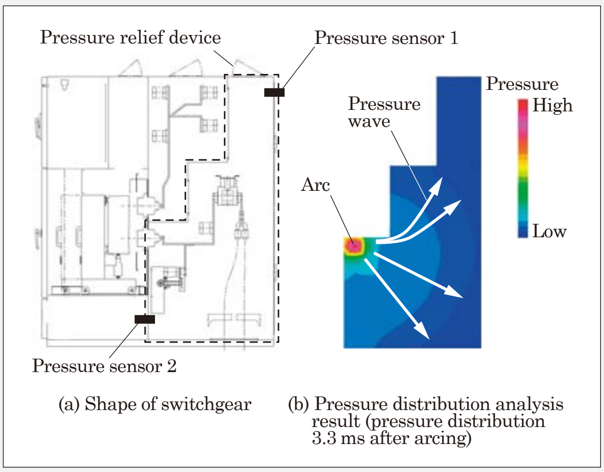


Fig.10 Example of switchgear shape and pressure analysis result

ternal arc faults (see Fig. 10). By using this method, we have developed a product that ensures safety in the event of internal arc faults in switchgears (Refer to “Analysis of Pressure Rise During Internal Arc Faults in Switchgear” on page 47).

3.4 Thermo-fluid simulation

Fuji Electric offers “smart stores” that make efficient use of energy at stores such as supermarkets and convenience stores. In these stores, freezing-refrigerating equipment including open showcases consume the most energy. For energy saving of open showcases, performance improvement of air curtains by reduction of heat entering through them is required. Frosting of the evaporator that generates cold air causes deterioration of the circulating air volume and characteristics of an air curtain. To address this issue, we have developed a thermo-fluid simulation technology that allows prediction of chronological variations of air curtain performance caused by frost formation and used this technology to develop a new air curtain system.

For simulation with frost formation taken into consideration, we have built a calculation model that allows estimation of the wind speed decrease of the evaporator due to growth of frost and temperature and humidity variations, which has made it possible to predict the average temperature rise over time in a showcase. In addition, we have built a showcase design tool (see Fig. 11) capable of automatic creation of simulation models and developed an optimization design technology for balancing between the many design factors for open showcases.

The new air curtain system developed by the optimization design technology has achieved a reduction in the supply air flow speed of an air curtain by gradually mixing the cold air from the back with the air curtain. It has been confirmed to offer an energy saving effect of over 30% from the conventional system through evaluation with a demonstration model (Refer to “Thermo-Fluid Simulation Technique for Achieving Energy Saving in Open Showcases” on page 53).

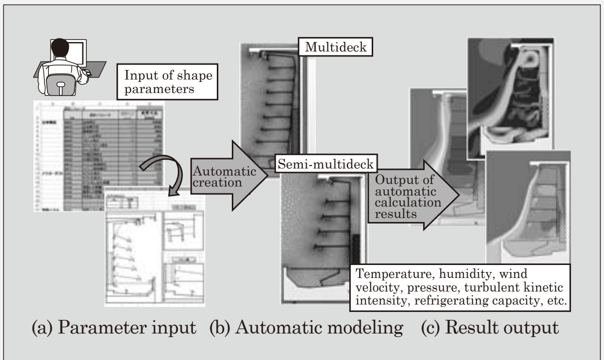


Fig.11 Showcase design tool

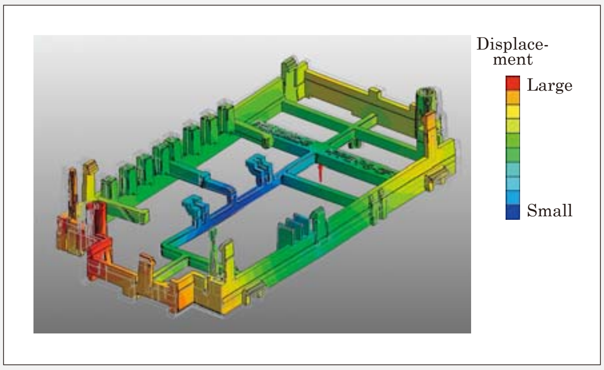


Fig.12 Example of warpage analysis

3.5 Resin flow in molding

Plastic, which has excellent electrical insulating properties and is often provided with kinetic properties and functions that can be used for industrial parts, is used in many products. In molding of plastic parts, it is important to build quality in the initial phase of development, when the degrees of freedom of the product shapes and mold structures are high and modification costs are low.

Fuji Electric is also working to raise the quality of injection molded parts by utilizing resin flow simulation and other simulation technologies with the focus given to resin, which is the principal ingredient of plastic materials.

For warping of moldings, which affects the functions of parts, fit with other parts and feasibility of automatic assembly, we use a 3D printer to output the shape after deformation obtained by resin flow simulation for verifying assemblability (see Fig. 12). In addition, to avoid the formation of welds in high-stress areas and achieve a structure that discharges the corrosive gas generated as resin decomposition gas, we have applied a filling simulation to study product shapes and gate locations.

To improve productivity by decreasing the cool time for injection molded parts, we have established high-speed molding technology that significantly reduces the molding cycle time while ensuring high quality by actively controlling the mold temperature in the molding cycle. We have combined this technology with a prediction of resin temperature distribution by resin flow simulation and used a 3D printer to produce parts with a 3D cooling channel formed inside. In this way, we have realized uniform mold temperature (Refer to “Simulation Technologies Supporting Quality Improvement in Injection Molding” on page 57).

4. Postscript

This paper has described the current status and future outlook of simulation technologies for product development. In the future, we intend to improve the efficiency of research and development and product design by adopting ever-advancing simulation technologies before others and applying them to a wider range of fields and applications for providing products that meet customer needs in a timely manner.

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