# Simulation Based Prediction of SiC Trench MOSFET Characteristics

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#### ABSTRACT

The development of semiconductor devices that use SiC (silicon carbide) based materials has been increasing as a means of achieving further energy savings in power electronic products. SiC trench MOSFET are capable of reducing loss even more than conventional planar types. Fuji Electric is implementing simulation based characteristic prediction in order to improve the efficiency of new SiC device development. It is necessary to consider the newly utilized crystal surface characteristics for the simulation of the trench-type because the characteristics of SiC differ by its crystal surfaces. We have established a convenient method for incorporating the parameters into the simulation model, which enabled reproduction of actual observations and prediction of performance improvements.

## 1. Introduction

There has been an increasing need for energy conserving products that can contribute to achieving a low carbon society. In addition, semiconductor devices for use in power electronics equipment are also being required to deliver energy savings. In recent years, there has been frequent development and commercialization of semiconductor devices that adopt silicon carbide (SiC) as a material capable of dissipating less power.

Fuji Electric has also commercialized energy-conserving power electronics equipment that utilizes SiC metal-oxide-semiconductor field-effect transistor (SiC-MOSFET) and SiC Schottky barrier diode (SiC-SBD) such as its power conditioning sub-systems for largecapacity mega solar facilities<sup>(1)</sup>.

In order to reduce loss in SiC devices, it is useful to understand the internal state of devices at the time of applying a voltage, and then improve on the device structure. The use of device simulations can make it easier to understand the internal state of devices, while also making it possible to know with high efficiency the improvement effect of changing multiple design parameters.

## 2. SiC Trench MOSFET

Currently, the mainstream type of SiC-MOSFET is the planar MOSFET. It forms a gate on the substrate surface. In order to respond to the market demand for further energy savings and cost reductions, it has been effective to decrease on-resistance  $R_{\rm on}$ : A during MOSFET conduction. As such, trench MOSFET have been attracting attention as a next-generation structure (see Fig. 1). Since the trench MOSFET embeds



Fig.1 MOSFET cross-sectional view

the gate in the trench, it is expected to reduce on-resistance via cell pitch reduction as compared with the planar MOSFET<sup>(2)</sup>. However, when attempting to make use of high breakdown electric field intensity, which is a characteristic of SiC, there is concern that breakdown could occur as a result of a high electric field being applied to the oxide film on the bottom of the trench<sup>(3)</sup>. Therefore, in order to ease the electric field intensity of the oxide film, we have been developing a trench MOSFET that equips the bottom of the trench with a p<sup>+</sup> type layer.

In order to reduce on-resistance, a structure design that minimizes parasitic resistance after accurately estimating channel resistance is very important. Parasitic resistance can be reduced by expanding the width of the n-type layer that is enclosed by the  $p^+$  type layer and by intensifying the impurity concentration, but withstand voltage will drop due to the simultaneous concentration of electric field in the corner of the deep  $p^+$  type layer. As a result, design must be imple-

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mented so as to minimize parasitic resistance in consideration of the trade-off between on-resistance and withstand voltage.

# 3. SiC Trench MOSFET Simulation

## 3.1 Simulation tasks

The use of simulations makes it possible to clarify the optimum structure and dimensions for on-resistance and withstand voltage, while increasing the potential for shortening development time by decreasing the number of trial productions. Furthermore, making use of high-precision simulations can lead to the analysis of unexpected phenomena. However, since current device simulations are configured based on data acquired from silicon, they may not always yield the accuracy required for SiC. For example, attention needs to be paid to how the electrical behavior of SiC differs based on the crystal surface<sup>\*1</sup>. The crystal surface orientation and atomic arrangement of SiC is shown in Fig. 2. Either a carbon face (C-face) or silicon face (Si-face) is used for the channel component of the planar MOSFET (see Fig. 1), whereas either an a-face or m-face of the side wall of the created trench is used as a channel for the trench MOSFET. Since the channel characteristics differ from the planar MOSFET, new simulation parameters need to be created. In addition, the impact ionization coefficient<sup>(4)</sup> is also different for SiC as a result of the crystal surface, thus making the withstand voltage of the a-face and m-face lower than that of the Si-face and C-face. Since the depletion layer extends from the p<sup>+</sup> type layer, the place enclosed by the  $p^+$  type layer of the bottom of the trench and the p<sup>+</sup> type layer below the source functions as a junction field-effect transistor (JFET) parasitic element. The place of concentration of electric field when retaining the withstand voltage depends on the width of JFET, and since the cell pitch and the width of JFET are more narrow for the trench MOSFET than the planar MOSFET, there will be a subtle change in withstand voltage with respect to the dimensions, enabling highprecision calculation of withstand voltage for both the a-face and the m-face.



Fig.2 SiC crystal surface and atomic arrangement

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In this regard, it can be thought that simulation models and parameter adjustments are not currently being sufficiently implemented for SiC with respect to actual experimental data. In order to accomplish these tasks, we utilized SenTaurus<sup>\*2</sup> by Synopsys to improve the accuracy of simulations<sup>(5)</sup>.

#### 3.2 Adoption of Coulomb scattering model

We studied mobility in order to consider the crystal surface dependence of the channel characteristic via simulation. As shown in Fig. 3, it can be seen that dominant factors differ for channel mobility, namely, Coulomb scattering, phonon scattering and surface roughness scattering<sup>\*3</sup> as a result of electric field intensity of the gate oxide film<sup>(6)</sup>. Furthermore, since SiC is characterized by a large number of defects for the oxide film and interface, low electric field mobility decreases<sup>(7)(8)</sup>. By introducing defects into the simulation, the poor convergence of calculation creates the problem of there being a need to adjust many parameters. Therefore, we matched up maximum mobility with the actual values by adjusting the high electric field mobility parameters. However, channel resistance is determined by integrating mobility as shown in Fig. 4, and in addition, it is necessary to make adjustment for the low electric field mobility curve in order to improve calculation precision. Therefore, we used a Coulomb scattering model that was capable of adjusting the low electric field mobility to implement a means of reproduction. As shown in Fig. 4, the new model has decreased the error between the simulation results and the actual mobility integration. In this manner, we have constructed a high-precision simulation capable of calculating channel resistance. The simulation



Fig.3 Universal curve of channel mobility

- \*1: Crystal surface: Refer to "Supplemental explanation 1" on page 62.
- \*2: SenTaurus is a trademark of Synopsys, Inc. in the U.S. and/or other countries.
- \*3: Coulomb scattering, phonon scattering and surface roughness scattering: Refer to "Supplemental explanation 2" on page 62.



Fig.4 Comparison between channel mobility actual measurement values and simulation

makes it easy to implement adjustments and exhibits good calculation convergence.

#### 3.3 Optimization of the impact ionization coefficient

We have studied the parameters related to the crystal surface of the impact ionization coefficient and have improved the accuracy of the withstand voltage calculation. The electric field distribution inside the device when retaining the withstand voltage is shown in Fig. 5. This suggests that an electric field concentrates in the corner of the p-type layer and that the various characteristics of the crystal surface compound to determine the withstand voltage. By adopting a Hatakeyama model<sup>(4)</sup> in the simulation, it is possible to reproduce the differences in the impact ionization coefficient by means of the SiC crystal surface. Since current parameters are set to the values obtained based on the actual values of low withstand voltage devices, it is necessary to improve calculation precision for high withstand voltage. The actual high withstand voltage parameter values for the Si-face and C-face are as reported<sup>(9)</sup>, and by adopting these into the simulator, it is possible to improve precision<sup>(10)</sup>.

We estimated the parameter error for the a-face



Fig.5 Electric field intensity distribution inside device when retaining withstand voltage



Fig.6 Withstand voltage JFET width dependence



Fig.7 Ron A JFET width dependence

and m-face and reconstructed the setting values. It was learned that the simulation results of the JFET width dependence of the withstand voltage after reconstructing the parameters closely matched the actual measurement values (see Fig. 6). In addition, Fig. 7 shows the JFET width dependence for  $R_{on}$ :A. When the withstand voltage is high, there is a tendency for the on-resistance to rise due to the parasitic resistance of the JFET, and it can be seen that there is a trade-off relationship between  $R_{on}$ :A and withstand voltage. By using the high-precision simulation that we constructed during this study, it has become easy to optimize device structure in consideration of trade-off.

## 4. Improvement of Device Characteristics via Simulation

By taking into account the new model introduced in Chapter 3, we studied how to improve device characteristics by using a precision enhanced simulation.

## 4.1 Improvement of trade-off between on-resistance and withstand voltage

In order to improve the trade-off between  $R_{on}$  A and withstand voltage, we investigated particularly large areas of JFET parasitic resistance. The elec-



Fig.8 Electric potential distribution inside device when "ON"



Fig.9 Trade-off between  $R_{on}$ ·A and withstand voltage before and after device structure optimization

tric potential distribution inside the device when on is shown in Fig. 8. Since parasitic resistance is large for areas with thick potential lines, optimizing device structure with priority given to these areas increases expectation that the trade-off between  $R_{\rm on}$  A and withstand voltage can be improved. Figure 9 shows the trade-off between  $R_{\rm on}$  A and withstand voltage before and after device structure optimization. We learn that the trade-off can be improved by optimizing the impurity concentration of the n-type layer and the device structure.

#### 4.2 Channel shortening

The relationship between the  $R_{\rm on}$  A of a channellength shortened trial production and threshold voltage  $V_{\rm th}$  is shown in Fig. 10.  $R_{\rm on}$  A can be reduced as a result of shortening the channel length to reduce channel resistance. However, since the threshold value decreases at the same time, the relationship between  $R_{\rm on}$  A and  $V_{\rm th}$  becomes nearly a straight line. The cause was analyzed by simulation.

Figure 11 shows the conduction band of the channel. The height of the peak of the convex part of the conduction band determines the  $V_{\rm th}$ , but we learned



Fig.10 Relationship between  $R_{on}$ ·A and threshold voltage



Fig.11 Conduction band figure of channel

that the height of the convex part decreases as a result of channel shortening. We also learned that this is due to one of the effects of channel shortening, namely, drain induced barrier lowering (DIBL), for which  $V_{\rm th}$  is affected by the depletion layer that extends from the drain side.

## 5. Future Tasks

The construction of high-precision simulations plays a role in shortening the development time of high-quality, high-performance devices. Since SiC is a new material compared with conventional silicon, it is necessary to improve precision even for calculations other than on-resistance and withstand voltage. For example, a few items requiring improvement would include the reproduction of temperature dependence, reproduction of impurity concentration dependence, reproduction of the impact of the number of defects caused by the creation of simplified types, reproduction of leakage current characteristics and reproduction of device reliability.

## 6. Postscript

In order to predict the characteristics of SiC trench MOSFET, we studied simulation models and parameters related to SiC crystal surface dependence, thus enabling us to reproduce actual measurement values, verify performance improvement methods and analyze physical phenomena. Since the construction of highprecision simulations plays a role in shortening the development time of high-quality, high-performance power devices, we will continue our efforts to improve the precision of SiC simulations, while striving to contribute to the realization of an energy-conserving society.

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