

FMW60N025S2HF

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FUJI POWER MOSFET

Super J MOS[®] S2 series

N-Channel enhancement mode power MOSFET

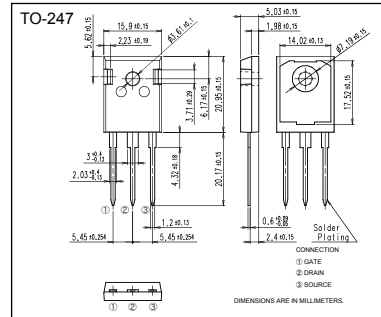
Features

- Pb-free lead terminal
- RoHS compliant
- uses Halogen-free molding compound

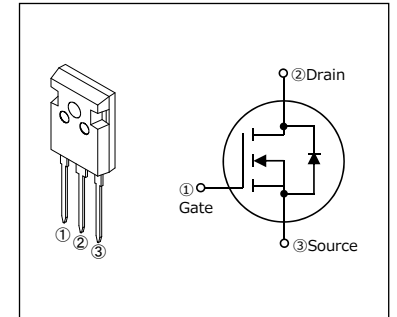
Applications

- For switching

Outline Drawings [mm]



Equivalent circuit schematic



Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V _{DS}	600	V	
	V _{DSX}	600	V	V _{GS} =-30V
Continuous Drain Current	I _D	95.5	A	T _c =25°C Note*1
		60.4	A	T _c =100°C Note*1
Pulsed Drain Current	I _{DP}	286.5	A	Note *1
Gate-Source Voltage	V _{GS}	±30	V	
Non-Repetitive Maximum Avalanche Current	I _{AS}	8.5	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E _{AS}	6074	mJ	Note *3
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	V/ns	V _{DS} ≤ 600V
Continuous Diode Forward Current	I _{SD}	95.5	A	T _c =25°C Note*1
		60.4	A	T _c =100°C Note*1
Pulsed Diode Forward Current	I _{SDP}	286.5	A	Note *1
Peak Diode Recovery dV/dt	dV/dt	15	V/ns	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *5
Maximum Power Dissipation	P _D	2.50	W	T _a =25°C
		575		T _c =25°C
Operating and Storage Temperature range	T _{ch}	150	°C	
	T _{stg}	-55 to +150	°C	

Note *1 : Limited by maximum channel temperature.

Note *2 : T_{ch} ≤ 150°C, See Fig.1 and Fig.2

Note *3 : Starting T_{ch}=25°C, I_{AS}=5.1A, L=428mH, V_{DD}=60V, R_G=50Ω, See Fig.1 and Fig.2

E_{AS} limited by maximum channel temperature and avalanche current.

Note *4 : I_{SD} ≤ 95.5A, -di/dt ≤ 100A/μs, V_{DS peak} ≤ 600V, T_{ch} ≤ 150°C.

Note *5 : I_{SD} ≤ 95.5A, dV/dt ≤ 15V/ns, V_{DS peak} ≤ 600V, T_{ch} ≤ 150°C.

■ Electrical Characteristics at T_c=25°C (unless otherwise specified)

• Static Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =6.07mA	2.5	4.0	4.5	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =600V V _{GS} =0V T _{ch} =25°C	-	-	25	μA
		V _{DS} =480V V _{GS} =0V T _{ch} =125°C	-	-	250	
Gate-Source Leakage Current	I _{GSS}	V _{DS} =0V V _{GS} = ± 30V	-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V I _D =47.8A	-	0.0230	0.0254	Ω
Gate resistance	R _G	f=1MHz, open drain	-	2.7	-	Ω

• Dynamic Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g _{fs}	V _{DS} =25V I _D =47.8A	38	77	-	S
Input Capacitance	C _{iss}	V _{DS} =400V	-	5700	-	pF
Output Capacitance	C _{oss}	V _{GS} =0V	-	192	-	
Reverse Transfer Capacitance	C _{rss}	f=250kHz	-	22.2	-	
Effective output capacitance, energy related (Note *6)	C _{o(er)}	V _{DS} =0...400V V _{GS} =0V	-	440	-	pF
Effective output capacitance, time related (Note *7)	C _{o(tr)}	V _{DS} =0...400V V _{GS} =0V I _D =constant	-	1865	-	
Turn-On Time	t _{d(on)}	V _{DD} =400V, V _{GS} =10V I _D =47.8A, R _G =5.6Ω See Fig.3 and Fig.4	-	38	-	ns
	t _r		-	170	-	
Turn-Off Time	t _{d(off)}		-	193	-	
	t _f		-	25	-	
Total Gate Charge	Q _G	V _{DD} =400V, V _{GS} =10V I _D =95.5A See Fig.5	-	222	-	nC
Gate-Source Charge	Q _{GS}		-	76	-	
Gate-Drain Charge	Q _{GD}		-	101	-	
Drain-Source crossover Charge	Q _{SW}		-	49	-	

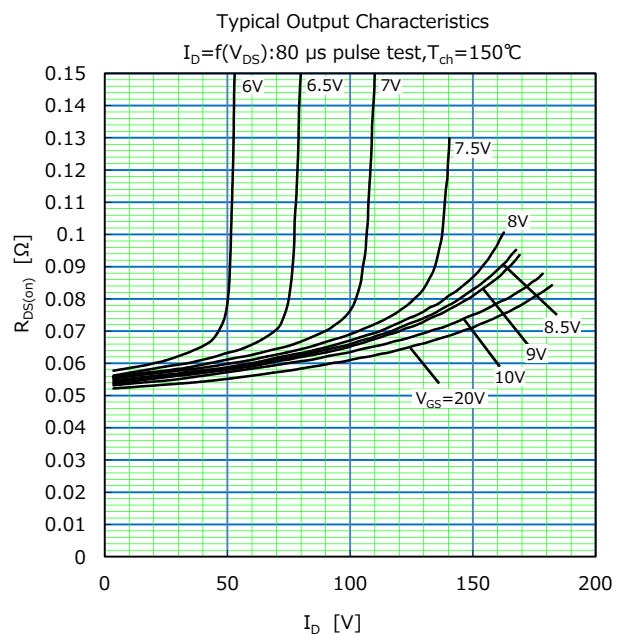
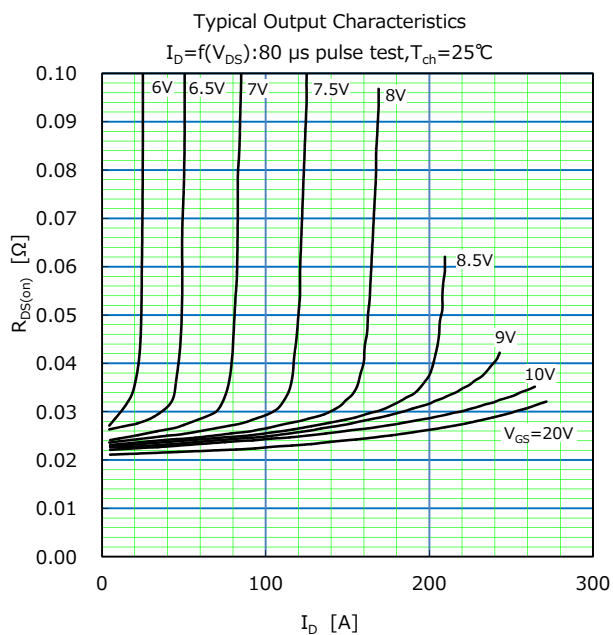
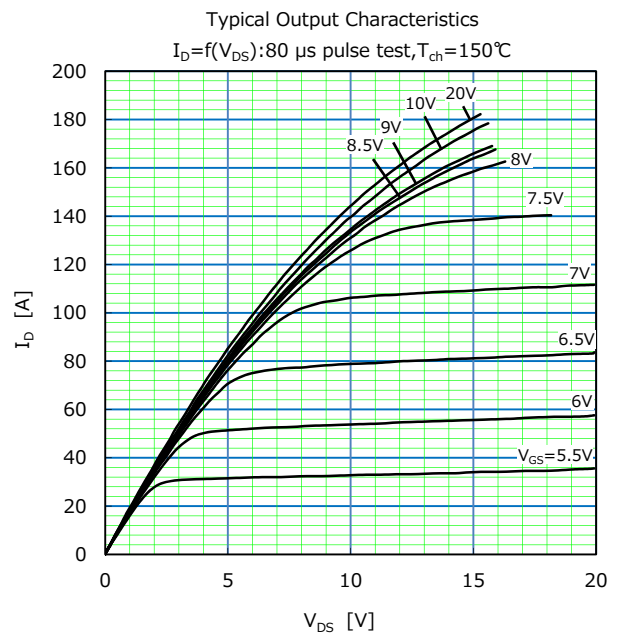
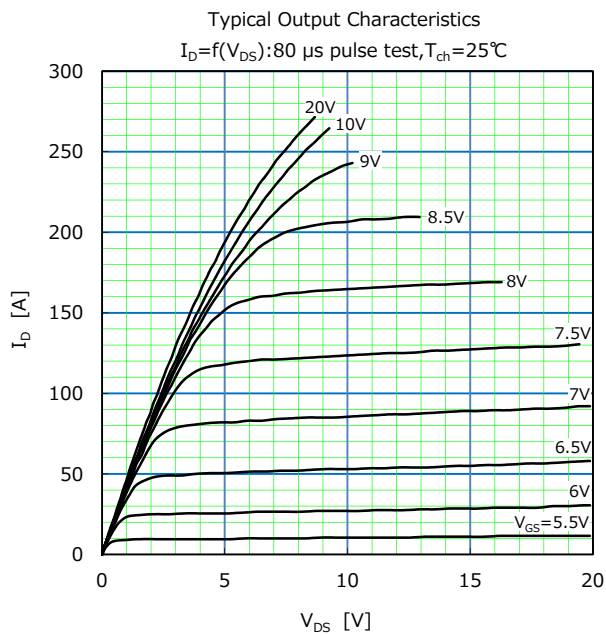
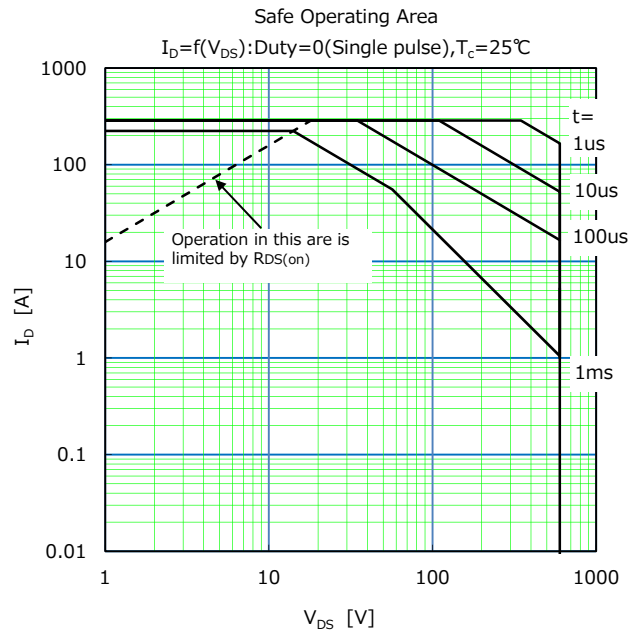
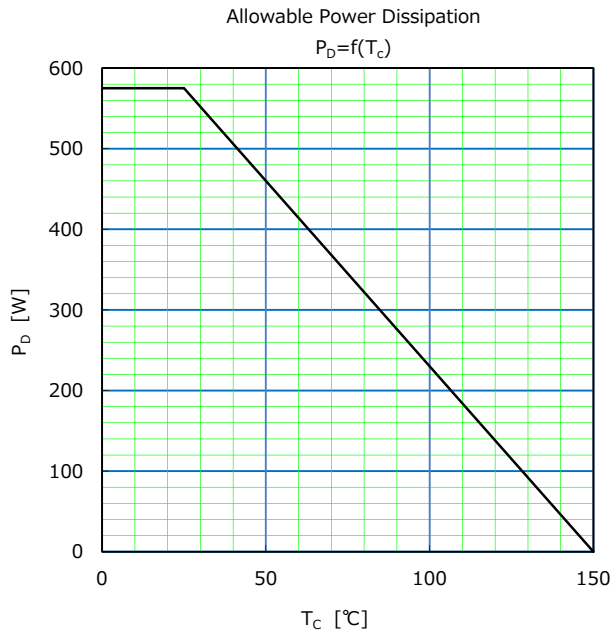
Note *6 : C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.Note *7 : C_{o(tr)} is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

• Reverse Diode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	V _{SD}	I _{SD} =95.5A, V _{GS} =0V T _{ch} =25°C	-	0.95	1.35	V
Reverse Recovery Time	t _{rr}	V _{DD} =400V, I _{SD} =95.5A -di/dt=100A/μs T _{ch} =25°C See Fig.6 and Fig.7	-	490	-	ns
Reverse Recovery Charge	Q _{rr}		-	11	-	μC
Peak Reverse Recovery Current	I _{rp}		-	44	-	A

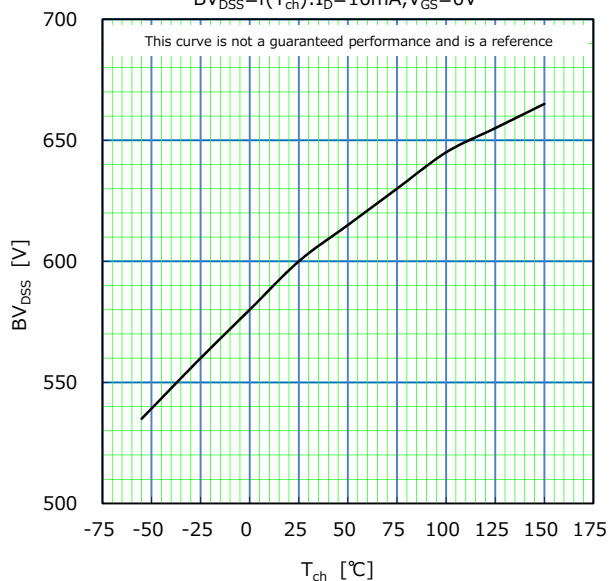
■ Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Channel to Case	R _{th(ch-c)}	-	-	0.217	°C/W
Channel to Ambient	R _{th(ch-a)}	-	-	50	°C/W



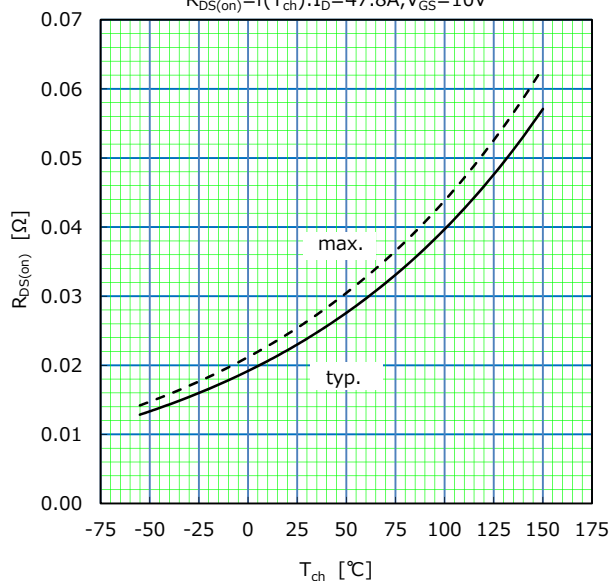
Drain-Source Breakdown Voltage

$$BV_{DS} = f(T_{ch}) : I_D = 10\text{mA}, V_{GS} = 0\text{V}$$

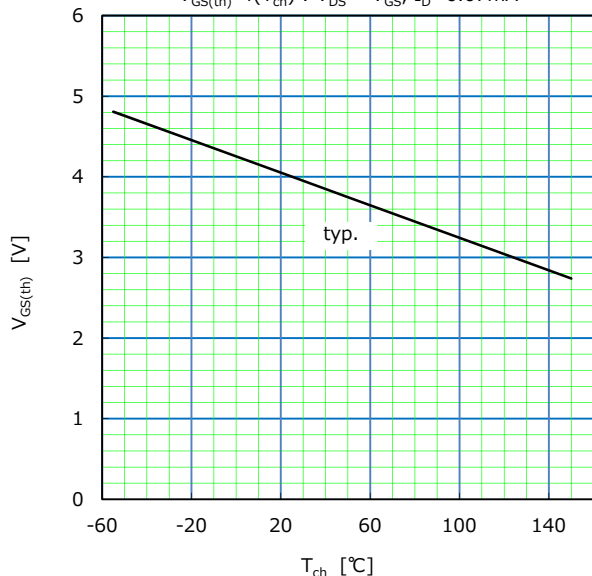


Drain-Source On-state Resistance

$$R_{DS(on)} = f(T_{ch}) : I_D = 47.8\text{A}, V_{GS} = 10\text{V}$$

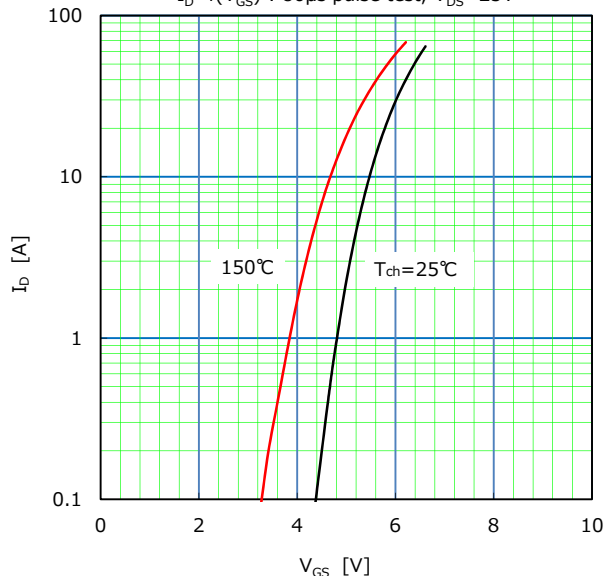
Gate Threshold Voltage vs. T_{ch}

$$V_{GS(th)} = f(T_{ch}) : V_{DS} = V_{GS}, I_D = 6.07\text{mA}$$



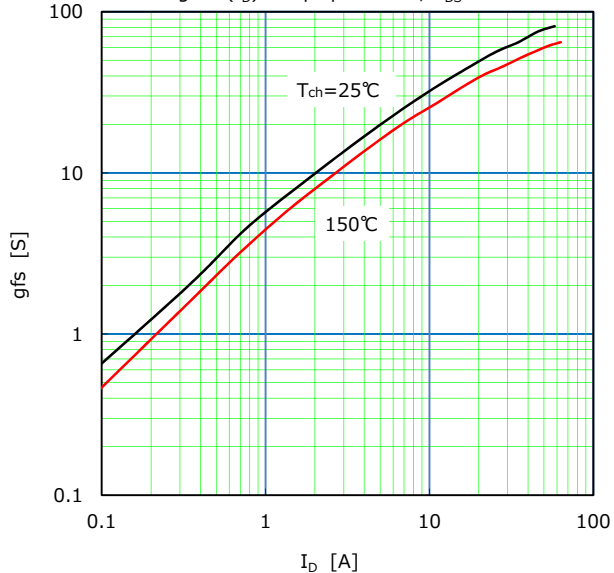
Typical Transfer Characteristic

$$I_D = f(V_{GS}) : 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



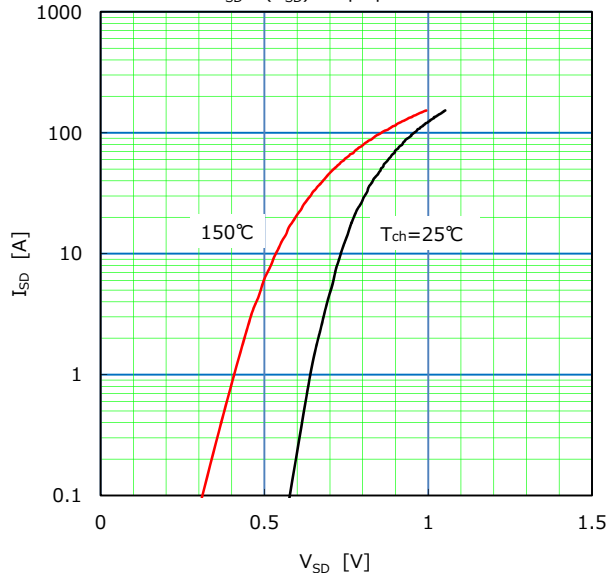
Typical Transconductance

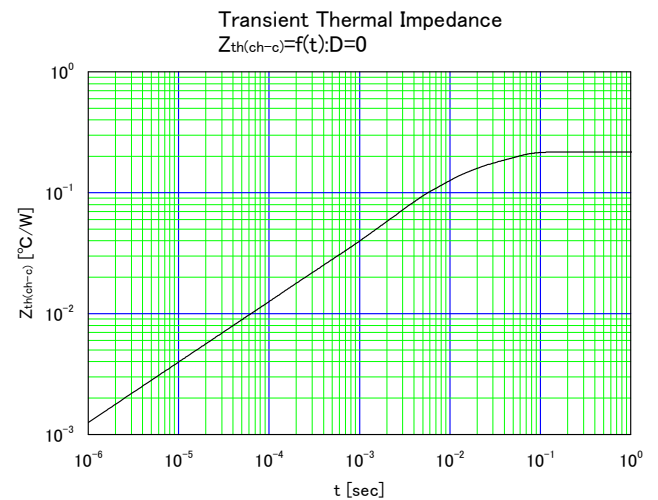
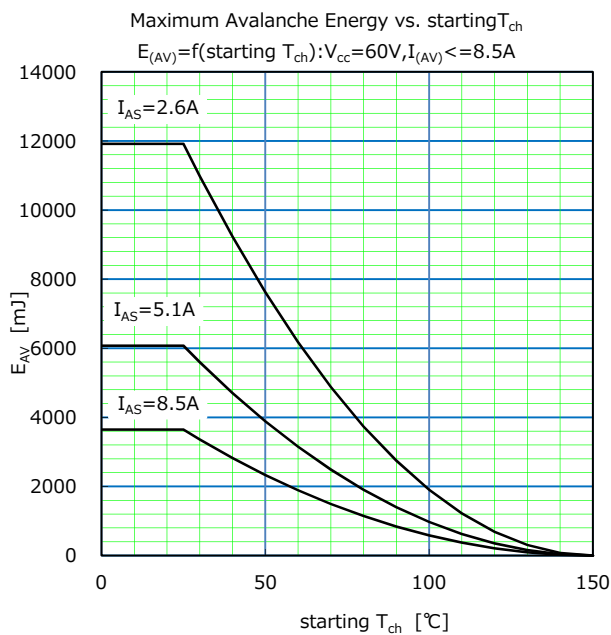
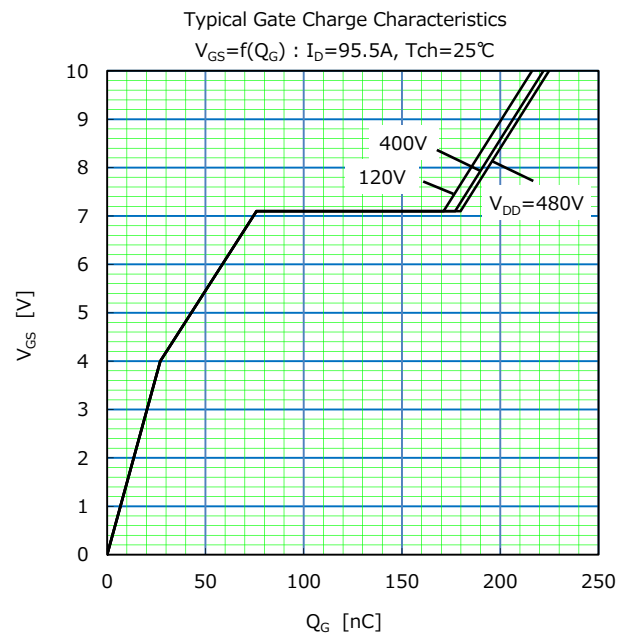
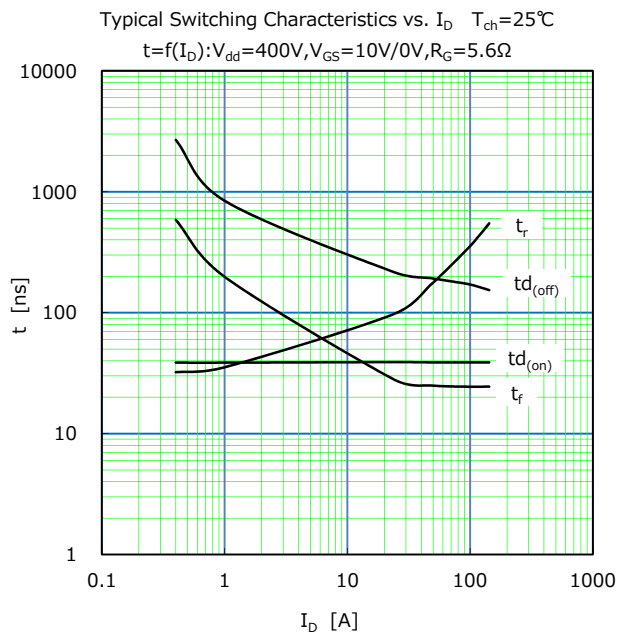
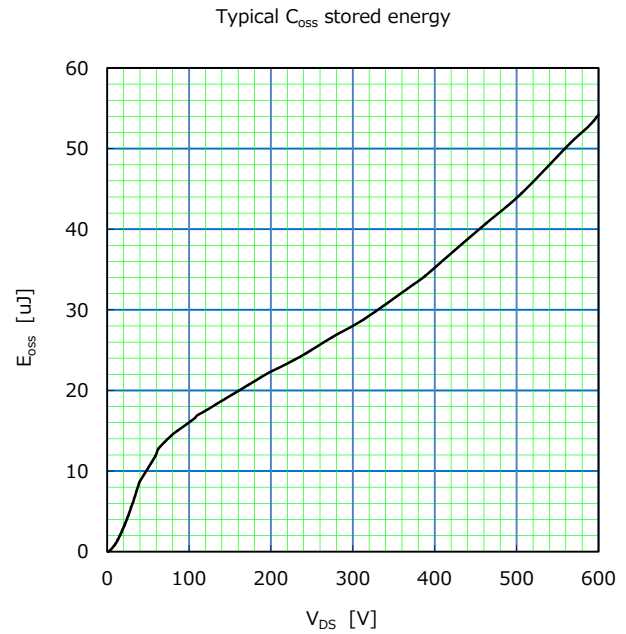
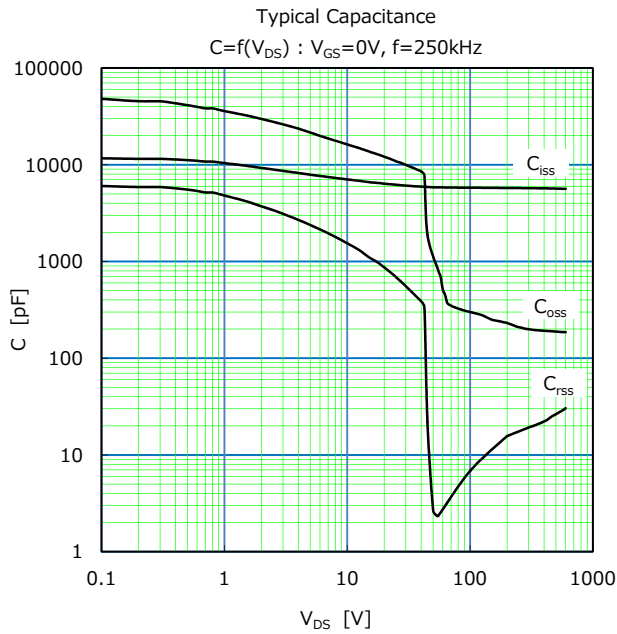
$$g_{fs} = f(I_D) : 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



Typical Forward Characteristics of Reverse Diode

$$I_{SD} = f(V_{SD}) : 80\mu\text{s pulse test}$$





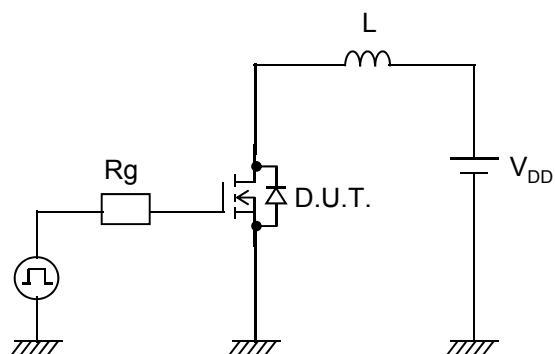


Fig.1 Avalanche Test circuit

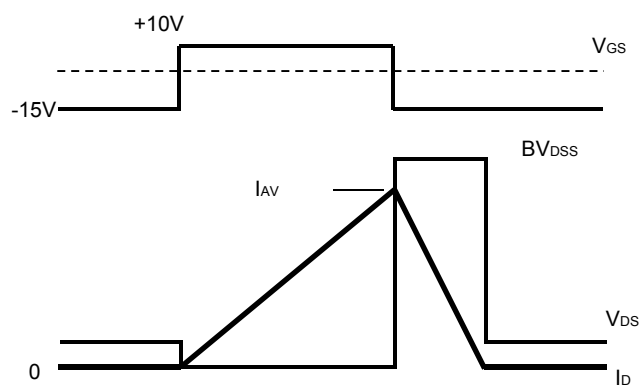


Fig.2 Operating waveforms of Avalanche Test

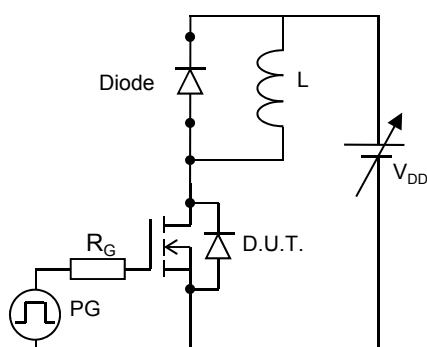


Fig.3 Switching Test circuit

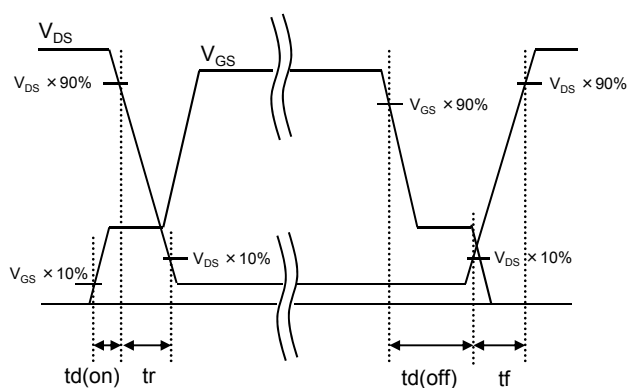


Fig.4 Operating waveform of Switching Test

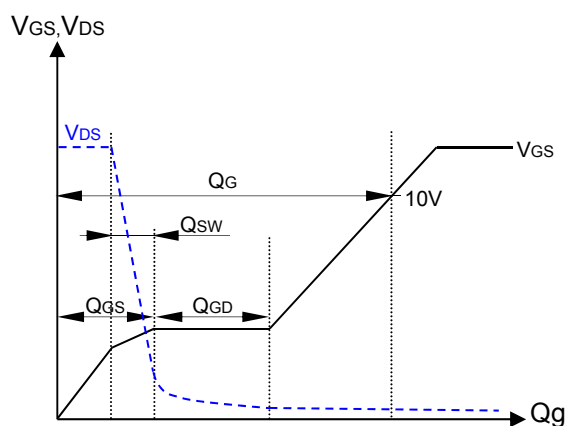


Fig.5 Operating waveform of Gate charge Test

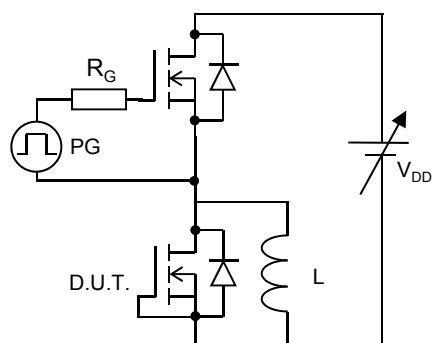


Fig.6 Reverse recovery Test circuit

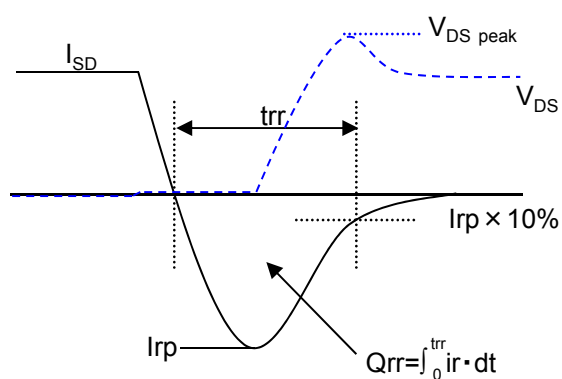
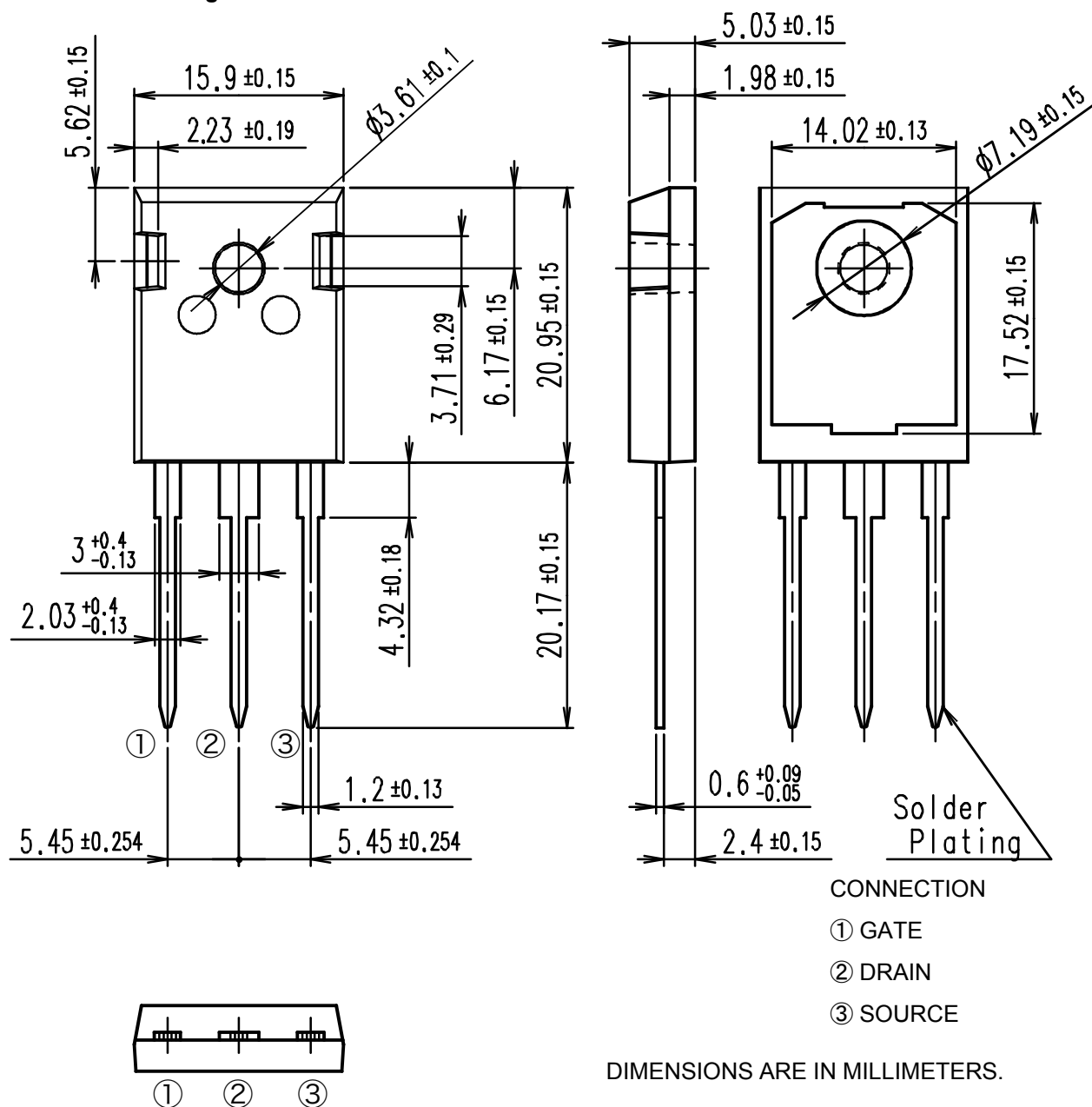
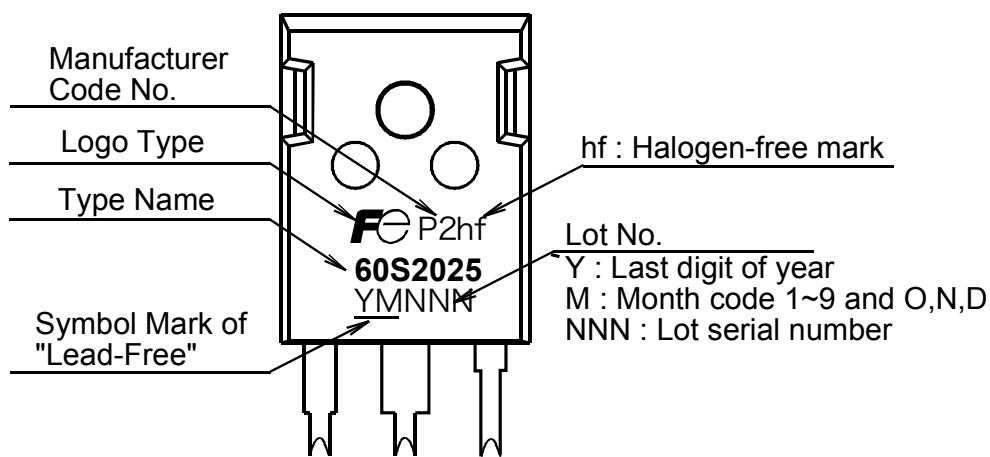


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-247 Package



■ Marking



* The font (font type,size) and the logo type size might be actually different.

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