# “Super J MOS S2 Series” and “Super J MOS S2FD Series” for DFN 8 × 8 Packages

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**ABSTRACT**

Fuji Electric has launched the DFN 8 × 8 package line-up of the “Super J MOS S2 Series” and “Super J MOS S2FD Series” 2nd-generation low power loss SJ-MOSFETs having a super-junction structure. This surface mount package is smaller and thinner than the previous D2-PACK package. The DFN 8 × 8 package doesn’t have a lead terminal, but all electrode pads are arranged on its back surface. Compared with the D2-PACK, the mounting area has been reduced by 58% and the package height to 0.85 mm, thus making high-density mounting possible. It also comes equipped with a sub-source terminal for speeding up switching operations.

## 1. Introduction

Energy consumption has been increasing steadily due to an increase in the global population mainly in emerging countries, economic development in China and other countries, and a greater volume of information being processed as a result of today’s IT innovation. Along with the increased energy consumption, securing the space for power converters has become important, not to mention improving their efficiency. In data centers and other facilities, small, thin and high-output power supplies are required as communication power supplies used in those facilities so that the limited space is effectively used. Recently, various devices including digital consumer electronics, in addition to IT-related devices such as PCs and servers, have come to be connected with the Internet by the Internet of Things (IoT). Due to the addition of various communication functions, the space available for the power supply mounted in those devices has come to be limited.

These circumstances have created increasing demand for smaller and thinner power supplies to be mounted in various devices. To reduce the size and thickness of power supplies, the size and thickness of passive components such as transformers and capacitors and semiconductor switching elements must be reduced. An effective way of achieving this is to increase the frequency at which power supplies operate. For that reason, power metal-oxide-semiconductor field-effect transistors (MOSFETs) capable of high-frequency operation are often used for semiconductor switching elements. This has created a demand for power MOSFETs that can switch at higher speeds and offer lower loss than those of conventional products.

## 2. Product Line-Up and Major Characteristics

To improve the power dissipation of power MOSFETs, Fuji Electric has launched the “Super J MOS Series” of SJ-MOSFETs, which apply a superjunction structure. We have replaced the conventional planar MOSFETs with them. To meet the demand for smaller and thinner power supplies, Fuji Electric launched the new surface-mount dual flat nonlead (DFN) 8 × 8 package that is smaller and thinner than the conventional D2-PACK package. They are included in the latest series of “Super J MOS S2 Series” (S2 Series) and “Super J MOS S2FD Series” (S2FD Series), which has a parasitic diode faster than that of the S2 Series. Figure 1 shows the external appearance of the DFN 8 × 8 package and Table 1 the product line-up and major characteristics.[1)-7)]

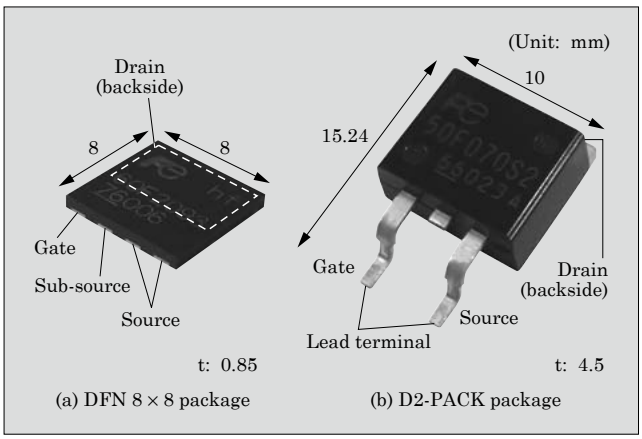


Fig.1 External appearance of package

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Table 1 Product line-up and major characteristics of DFN 8 × 8 package

| Series name | Type | On-state resistance $r_{DS(on)(max.)}$ (mΩ) | Drain-source voltage $V_{DS}$ (V) |
|---|---|---|---|
| Super J MOS S2 Series | FML60N091S2 | 91 | 600 |
| | FML60N103S2 | 103 | |
| | FML60N115S2 | 115 | |
| | FML60N146S2 | 146 | |
| | FML60N187S2 | 187 | |
| | FML60N223S2 | 223 | |
| Super J MOS S2FD Series | FML60N093S2FD | 93 | |
| | FML60N104S2FD | 104 | |
| | FML60N118S2FD | 118 | |
| | FML60N150S2FD | 150 | |
| | FML60N191S2FD | 191 | |

## 3. Features

### 3.1 Compact and low height

Figure 2 shows external dimensions of the DFN 8 × 8 package. It is a square of 8 mm × 8 mm with a greatly reduced thickness of 0.85 mm. The structure with all electrode pads arranged on the back surface of the package does not have lead terminals. This allows higher-density mounting on a printed circuit board than packages with lead terminals such as D2-PACK. The electrode pad arrangement includes (1) gate, (2) sub-source, (3) (4) source and (5) drain and one feature is the provision of a sub-source terminal.

The following shows major indicators of the external appearances of the DFN 8 × 8 package as ratios to those of the D2-PACK package, which is a conventional and typical surface mount package:

(a) Footprint: 58% smaller
(b) Package height: 81% lower
(c) Package volume (including lead terminals): 92% smaller

Table 2 shows on-state resistances per unit footprint and per unit mounting volume. DFN 8 × 8 package products have reduced the on-state resistances per unit footprint and per unit mounting volume by 52% and 91% respectively, compared with D2-PACK products. By reducing the package height to 0.85 mm, the package can be mounted on the back side of a double-sided board. This allows power supplies to be smaller and thinner and offer higher power density.

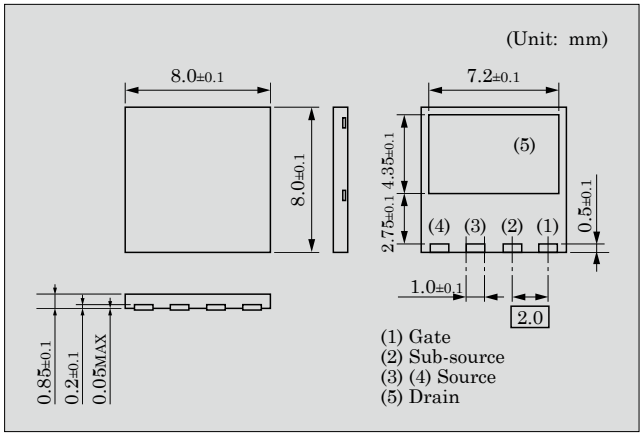


Fig.2 External dimensions of package

Table 2 On-state resistances per unit footprint and per unit mounting volume

| Package | Applicable $r_{DS(on)(max.)}$ | Per unit footprint $r_{DS(on)(max.)}$ | Per unit mounting volume $r_{DS(on)(max.)}$ |
|---|---|---|---|
| | Ω | Ω·mm² | Ω·mm³ |
| DFN 8 × 8 | 0.090 | 5.8 | 4.90 |
| D2-PACK | 0.079 | 12.0 | 54.18 |
| Ratio (DFN 8 × 8/ D2-PACK) | 113.9% | 47.8% | 9.0% |

### 3.2 Low switching loss

Figure 3 shows the gate drive circuits of a DFN 8 × 8 package product and a typical 3-terminal package product, such as TO-220 or D2-PACK. A typical 3-terminal package product has a structure where inductance $L_s$ such as lead inductance $L_{s1}$ and source substrate wiring inductance $L_{s2}$ inside the package is included in the gate drive circuit. Consequently, during MOSFET switching operation, a back electromotive force is generated on $L_s$ by the time derivative of drain current $di_D/dt$ and affects the gate drive voltage. This back electromotive force works to reduce the gate volt-

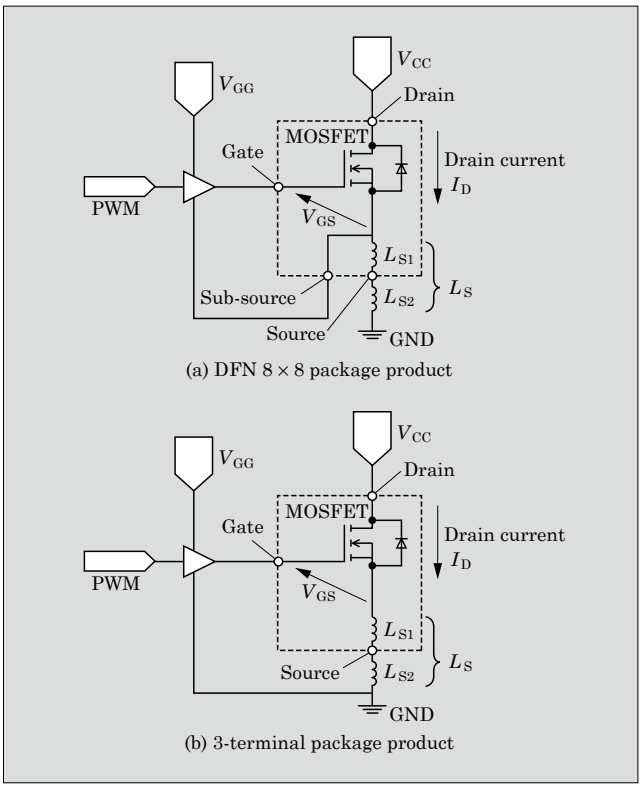


Fig.3 Drive circuits of DFN 8 × 8 package product and 3-terminal package product

age when the MOSFET is turned on, and to increase the gate voltage when the MOSFET is turned off. This causes a delay in the switching time and hinders any attempt to reduce the switching loss and achieve higher frequency.

On the other hand, a sub-source terminal is added to DFN 8 × 8 package products. This allows $L_s$ to be separated from the gate drive circuit and the influence of the back electromotive force generated on $L_s$ can be eliminated. As a result, shortening the switching time reduces the switching loss and achieves higher frequency.

Figure 4 shows a comparison of the gate resistance dependency of turn-on loss between a DFN 8 × 8 package product and a 3-terminal package product when used in a chopper circuit. Figure 5 shows the same with turn-off loss. For the measurement, we used "FML60N150S2FD" (600 V, 150 mΩ) as a DFN 8 × 8 package product and the TO-220 "FMP133S2FD" (600 V, 133 mΩ) as a 3-terminal package product. The measurement conditions were: $V_{CC}$ = 400 V, $I_D$ = 20 A and $V_{GG}$ = 10 V.

The DFN 8 × 8 package product showed a great improvement in both turn-on loss and turn-off loss in the entire range of 0 to 25 Ω of the external gate resistance. When the external gate resistance is 10 Ω, turn-on loss is reduced by 75% and turn-off loss is reduced by 35%.

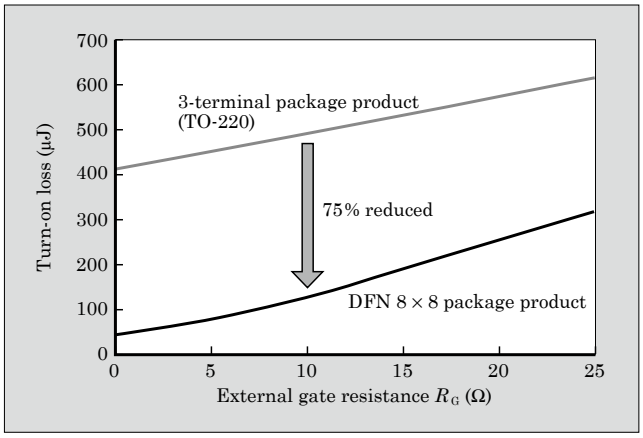


Fig.4 Comparison of turn-on loss

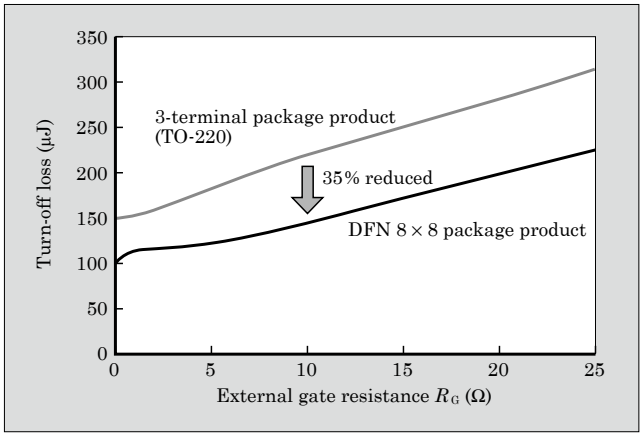


Fig.5 Comparison of turn-off loss

## 4. Effect of Application

For verifying the effect of application of DFN 8 × 8 package products, we used a DFN 8 × 8 package product and TO-220 as a typical 3-terminal package product in a power factor correction (PFC) circuit as shown in Fig. 6 to compare the power supply performance. As the control IC of the PFC circuit, we used "FA5612," Fuji Electric's continuous current mode PFC control IC. As the input and output conditions and circuit constant, we set the input voltage at 100 V/50 Hz, output voltage at 390 V DC and MOSFET gate resistance $R_G$ at 22 Ω. For the evaluation, we used "FML60N223S2" (600 V/223 mΩ) as a DFN 8 × 8 package product and the TO-220 "FMP60N190S2" (600 V/190 mΩ).

Figure 7 shows the load dependency of power supply efficiency. The DFN 8 × 8 package product shows a better efficiency compared with TO-220 in the range with a load factor of 50% or higher. In terms of efficiency with 100% load, the result shows an efficiency improvement of 0.2 points.

Figure 8 shows a comparison of switching loss under conditions where the maximum current flows in the MOSFET with 100% load. Both the turn-on loss and turn-off loss are smaller with the DFN 8 × 8 package product and the total switching loss has been reduced by 30%. In this way, power loss has been re-

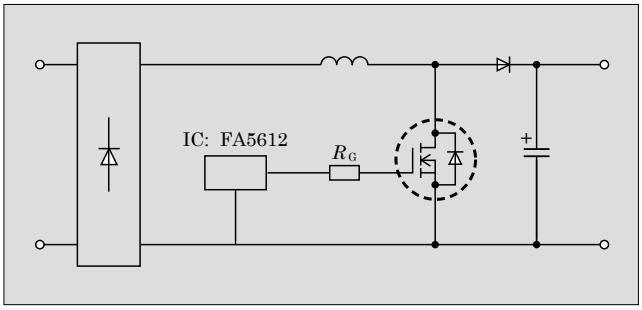


Fig.6 Circuit diagram of PFC demonstration board

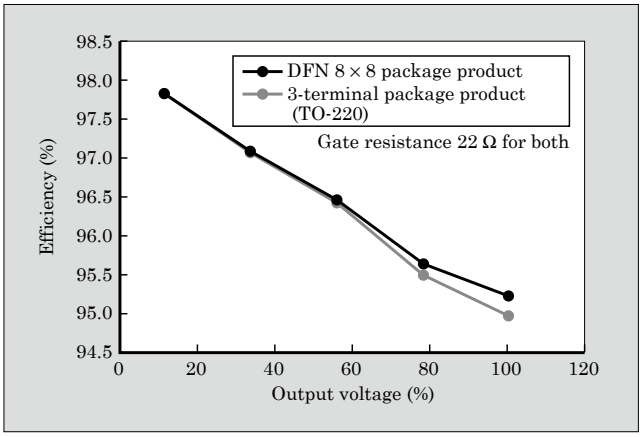


Fig.7 Efficiency characteristic of power supply

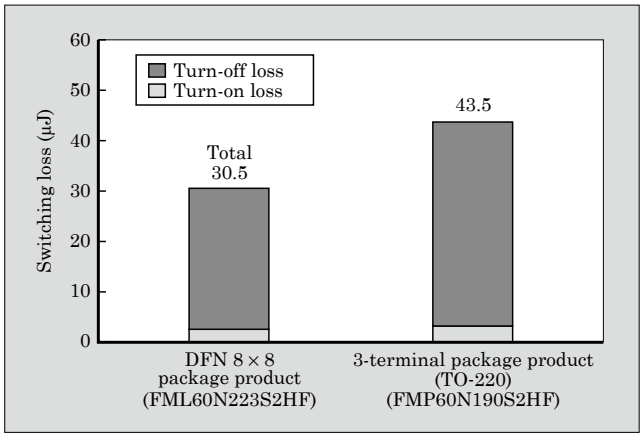


Fig.8 Switching loss comparison

duced and efficiency improved.

Figures 9 and 10 show turn-on and turn-off waveforms respectively under conditions where the maximum current flows in the MOSFET with 100% load. The solid lines show waveforms for the DFN 8 × 8 package product and the broken lines waveforms for TO-220. The switching speed is faster with the DFN 8 × 8 package product for both turn-on and turn-off. The period of crossover of drain voltage $V_{DS}$ waveform and drain current $I_D$ waveform at the time of switching is shorter, which indicates a smaller switching loss. This is an effect of separating $L_s$ from the gate drive circuit by using the sub-source terminal as shown in Fig. 3.

This leads to the conclusion that DFN 8 × 8 package products contribute to high-speed switching operation and improved power supply efficiency.

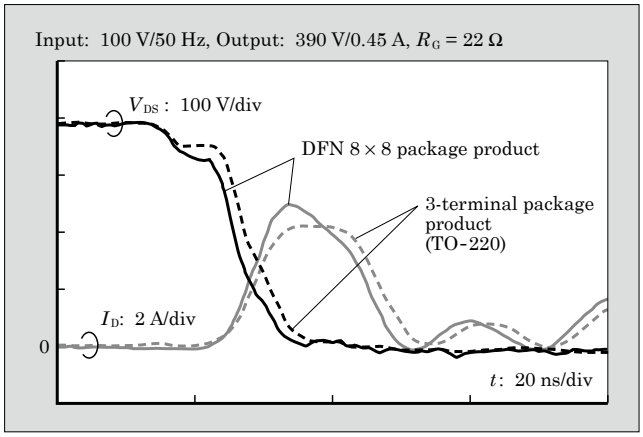


Fig.9 Turn-on waveforms

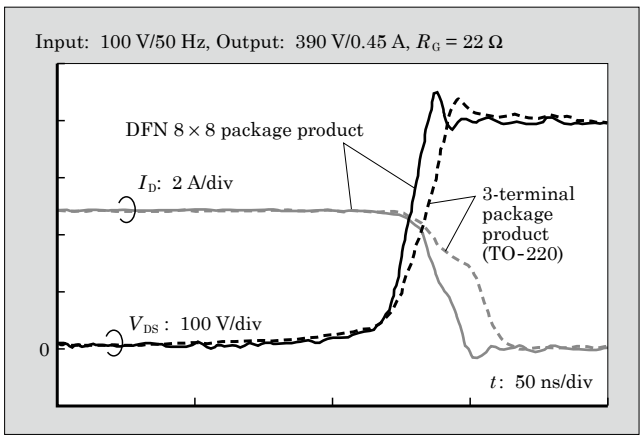


Fig.10 Turn-off waveforms

## 5. Postscript

This paper has presented a line-up of DFN 8 × 8 packages integrating the "Super J MOS S2 Series" and "Super J MOS S2FD Series," which achieve both low on-state resistance and low switching loss. The product line-up is capable of high-speed switching operation by utilizing the package effect in addition to having characteristics of low on-state resistance and low switching loss. This allows higher-frequency operation of power supplies than with conventional package products and raises expectations for contributions to size reduction and power density increase for power supplies.

In the future, to keep up with changes in market needs, we intend to continue to work on providing comprehensive solutions in ways such as expanding the package line-up in addition to improving the $r_{DS(on)} \cdot A$ performance and providing a wider drain-source voltage selection of power MOSFETs.

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