

FMP07N60S1

Super J MOS[®] S1 series

N-Channel enhancement mode power MOSFET

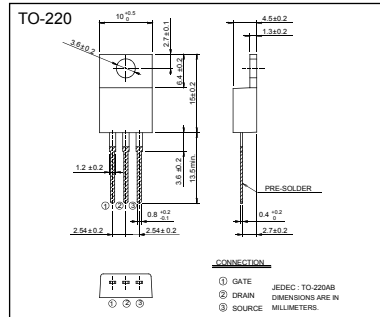
Features

- Pb-free lead terminal
- RoHS compliant

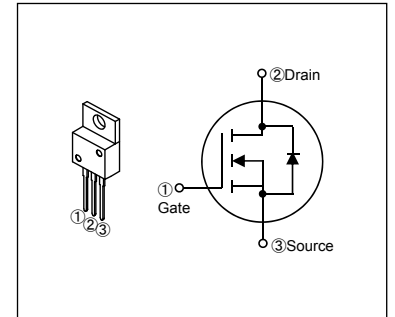
Applications

- For switching

Outline Drawings [mm]



Equivalent circuit schematic



Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V _{DS}	600	V	
	V _{DSX}	600	V	V _{GS} =-30V
Continuous Drain Current	I _D	±6.5	A	T _c =25°C Note*1
		±4.1	A	T _c =100°C Note*1
Pulsed Drain Current	I _{DP}	±19.5	A	
Gate-Source Voltage	V _{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I _{AR}	2.3	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E _{AS}	203.4	mJ	Note *3
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	kV/μs	V _{DS} ≤ 600V
Peak Diode Recovery dV/dt	dV/dt	15	kV/μs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *5
Maximum Power Dissipation	P _D	2.02	W	T _a =25°C
		60		T _c =25°C
Operating and Storage Temperature range	T _{ch}	150	°C	
	T _{stg}	-55 to +150	°C	

Note *1 : Limited by maximum channel temperature.

Note *2 : T_{ch} ≤ 150°C, See Fig.1 and Fig.2

Note *3 : Starting T_{ch}=25°C, I_{AS}=1.4A, L=190mH, V_{DD}=60V, R_G=50Ω, See Fig.1 and Fig.2
E_{AS} limited by maximum channel temperature and avalanche current.

Note *4 : I_F ≤ -I_D, -di/dt=100A/μs, V_{DD} ≤ 400V, V_{peak} ≤ BV_{DSS}, T_{ch} ≤ 150°C.

Note *5 : I_F ≤ -I_D, dV/dt=15kV/μs, V_{DD} ≤ 400V, V_{peak} ≤ BV_{DSS}, T_{ch} ≤ 150°C.

Electrical Characteristics at T_c=25°C (unless otherwise specified)

• Static Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V	600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I _D =250μA V _{DS} =V _{GS}	2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	I _{BSS}	V _{DS} =600V V _{GS} =0V	-	-	25	μA
		T _{ch} =25°C				
Zero Gate Voltage Drain Current	I _{BSS}	V _{DS} =480V V _{GS} =0V	-	-	250	μA
		T _{ch} =125°C				
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ± 30V V _{DS} =0V	-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =3.25A V _{GS} =10V	-	0.49	0.58	Ω
Gate resistance	R _G	f=1MHz, open drain	-	3.4	-	Ω

• Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g_{fs}	$I_D=3.25A$ $V_{DS}=25V$	3	6	-	S
Input Capacitance	C_{iss}	$V_{DS}=10V$	-	510	-	pF
Output Capacitance	C_{oss}	$V_{GS}=0V$	-	1130	-	
Reverse Transfer Capacitance	C_{rss}	$f=1MHz$	-	100	-	
Effective output capacitance, energy related (Note *6)	$C_{o(er)}$	$V_{GS}=0V$ $V_{DS}=0...480V$	-	43	-	
Effective output capacitance, time related (Note *7)	$C_{o(tr)}$	$V_{GS}=0V$ $V_{DS}=0...480V$ $ID=constant$	-	120	-	
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=400V, V_{GS}=10V/0V$ $I_D=3.25A, R_G=36\Omega$ See Fig.3 and Fig.4	-	9.5	-	ns
Turn-Off Time	$t_{d(off)}$ t_f		-	28	-	
Total Gate Charge	Q_G	$V_{DD}=480V, I_D=6.5A$ $V_{GS}=10V$ See Fig.5	-	73	-	nC
Gate-Source Charge	Q_{GS}		-	17.5	-	
Gate-Drain Charge	Q_{GD}		-	21	-	
Drain-Source crossover Charge	Q_{SW}		-	7	-	
			-	4.5	-	

Note *6 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS} .

Note *7 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS} .

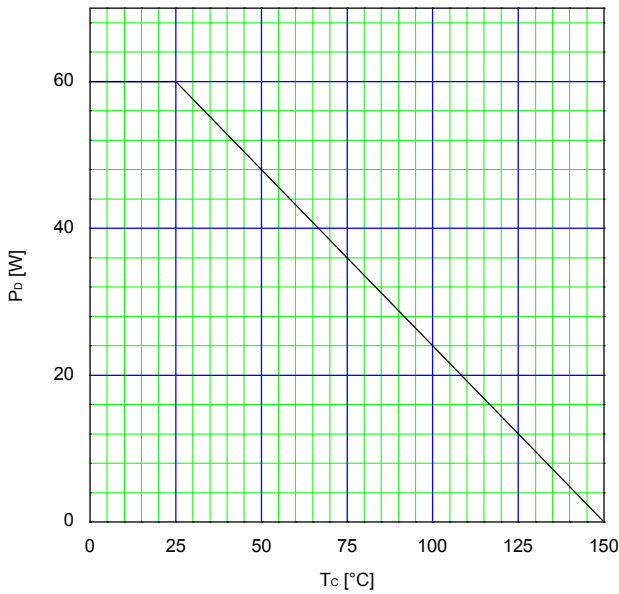
• Reverse Diode

Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	I_{AV}	$L=42.9mH, T_{ch}=25^\circ C$ See Fig.1 and Fig.2	2.3	-	-	A
Diode Forward On-Voltage	V_{SD}	$I_f=6.5A, V_{GS}=0V$ $T_{ch}=25^\circ C$	-	0.9	1.35	V
Reverse Recovery Time	t_{rr}	$I_f=6.5A, V_{DD}=400V$ $di/dt=100A/\mu s$	-	275	-	ns
Reverse Recovery Charge	Q_{rr}	$V_{GS(Q1)}=short, V_{GS(Q2)}=10V/0V$ $R_G=300\Omega$ $T_{ch}=25^\circ C$	-	2.7	-	μC
Peak Reverse Recovery Current	I_{rp}	See Fig.6 and Fig.7	-	18	-	A

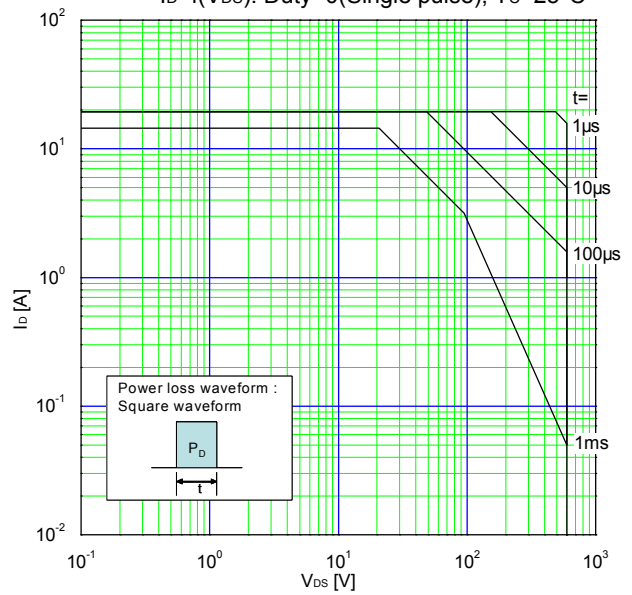
■ Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	2.08	$^\circ C/W$
Channel to Ambient	$R_{th(ch-a)}$	-	-	62	$^\circ C/W$

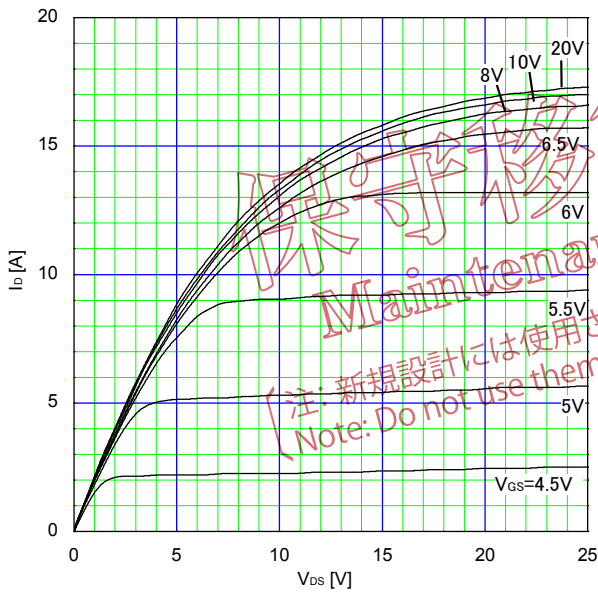
Allowable Power Dissipation
 $P_D = f(T_C)$



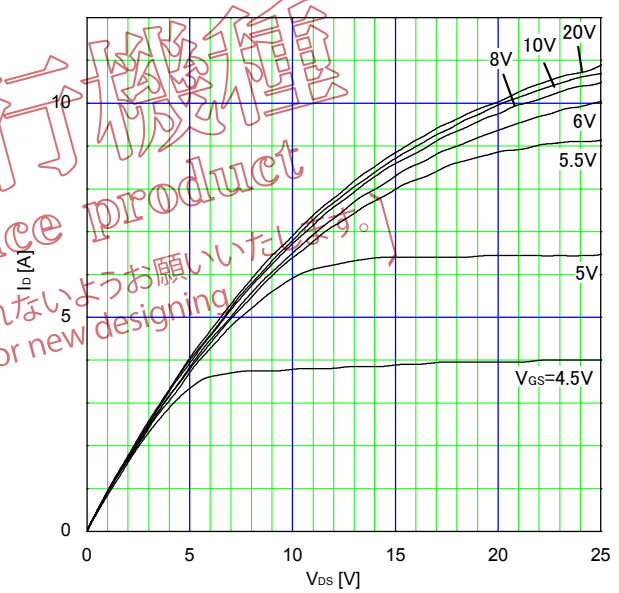
Safe Operating Area
 $I_D = f(V_{DS})$: Duty=0 (Single pulse), $T_C = 25^\circ\text{C}$



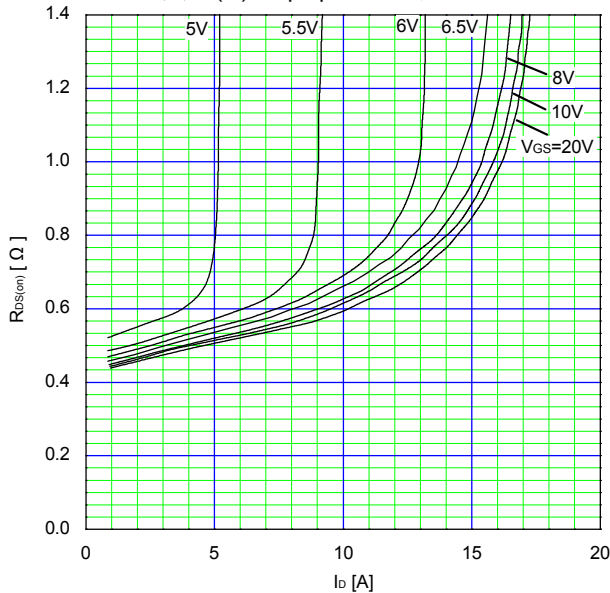
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80µs pulse test, $T_{ch} = 25^\circ\text{C}$



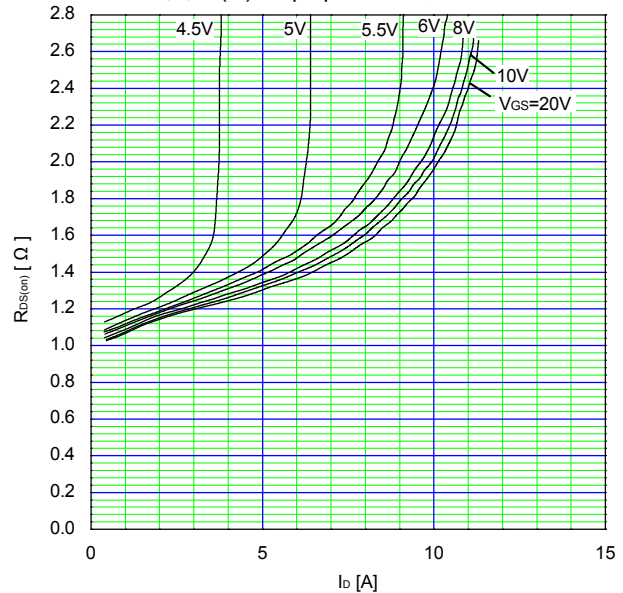
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80µs pulse test, $T_{ch} = 150^\circ\text{C}$



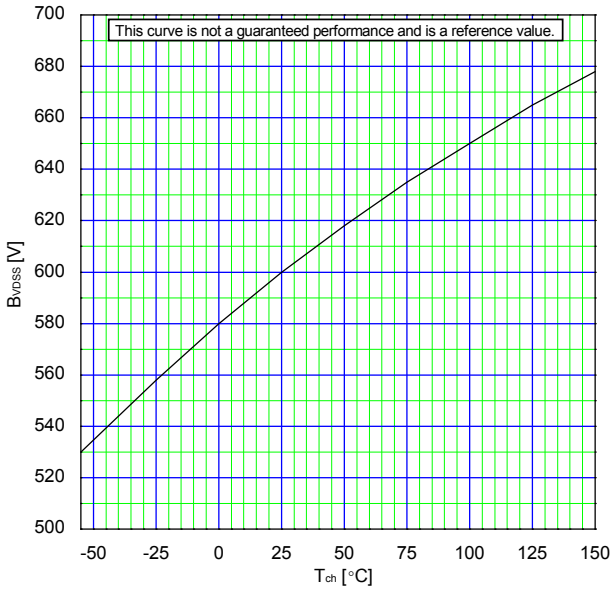
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80µs pulse test, $T_{ch} = 25^\circ\text{C}$



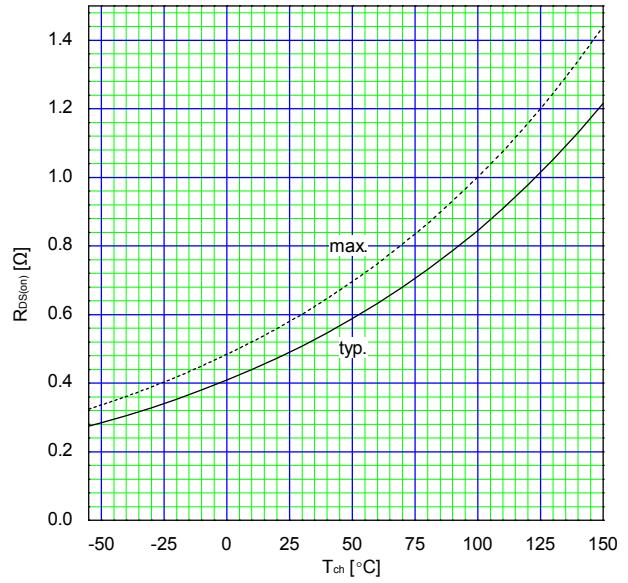
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80µs pulse test, $T_{ch} = 150^\circ\text{C}$



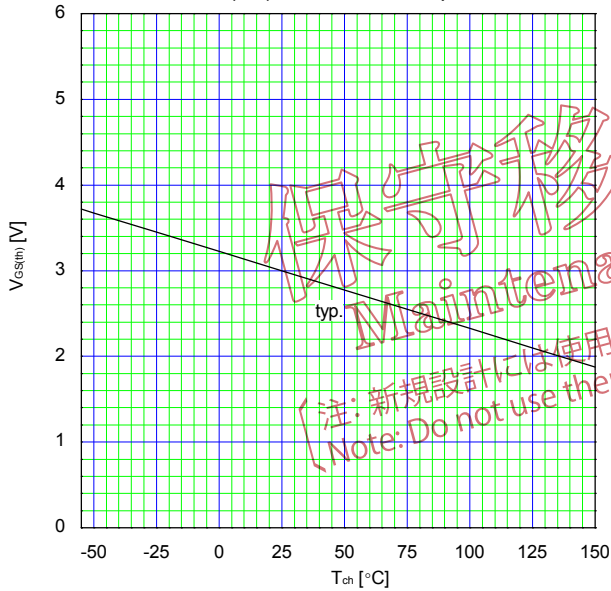
Drain-Source Breakdown Voltage
 $B_{V_{DS}}=f(T_{ch}): I_D=10\text{mA}, V_{GS}=0\text{V}$



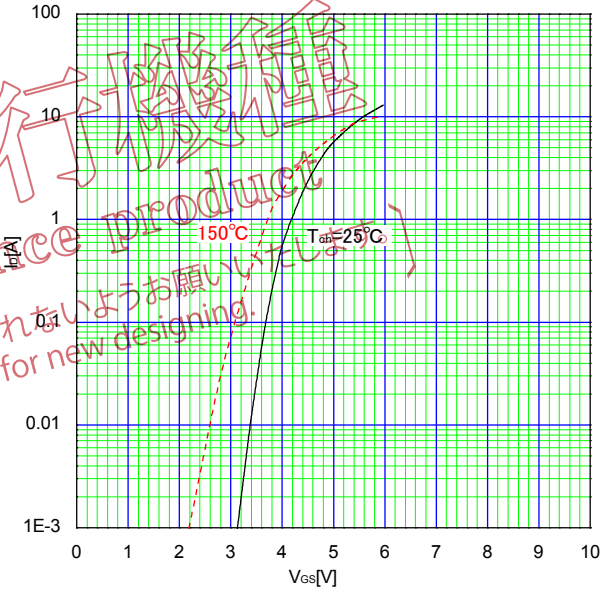
Drain-Source On-state Resistance
 $R_{DS(on)}=f(T_{ch}): I_D=3.25\text{A}, V_{GS}=10\text{V}$



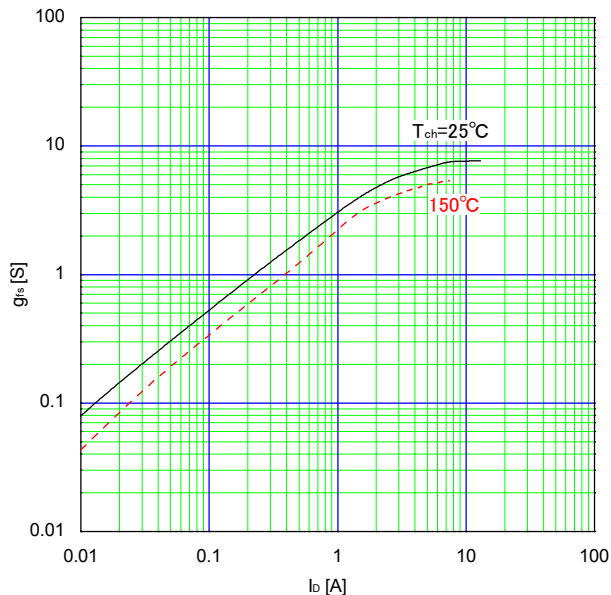
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)}=f(T_{ch}): V_{DS}=V_{GS}, I_D=250\mu\text{A}$



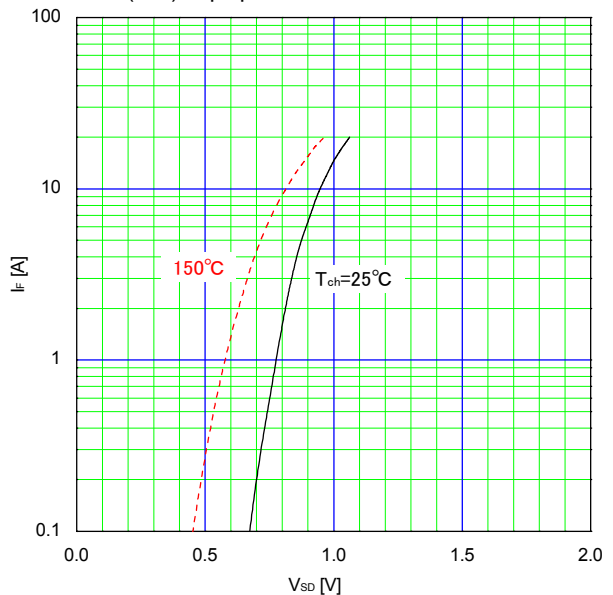
Typical Transfer Characteristic
 $I_D=f(V_{GS}): 80\mu\text{s pulse test}, V_{DS}=25\text{V}$



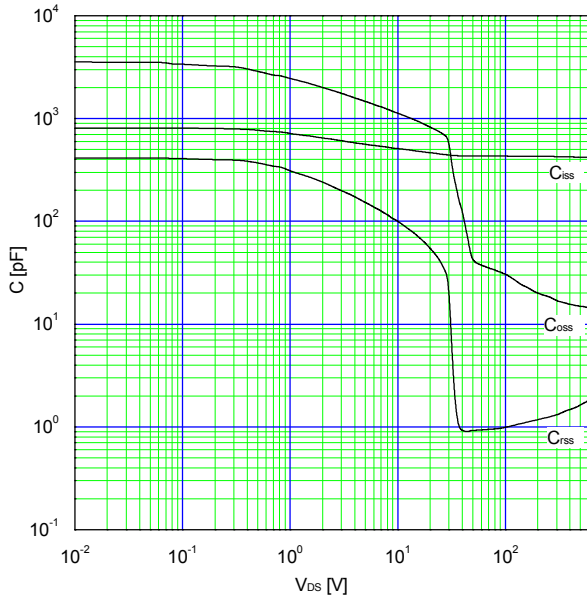
Typical Transconductance
 $g_{fs}=f(I_D): 80\mu\text{s pulse test}, V_{DS}=25\text{V}$



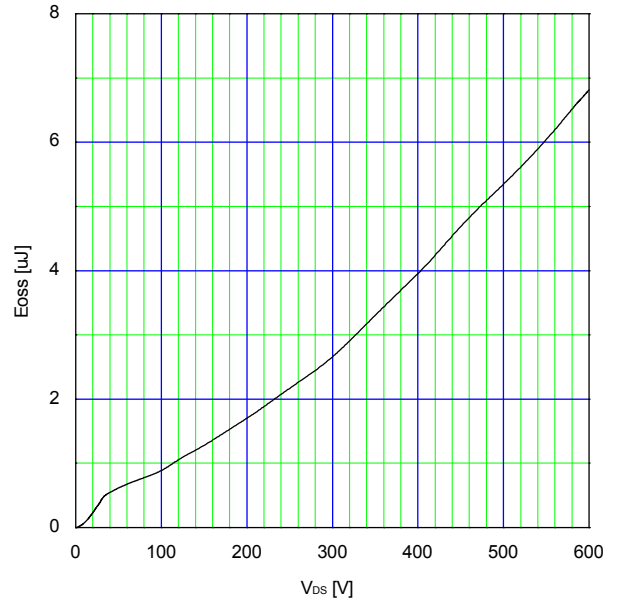
Typical Forward Characteristics of Reverse Diode
 $I_F=f(V_{SD}): 80\mu\text{s pulse test}$



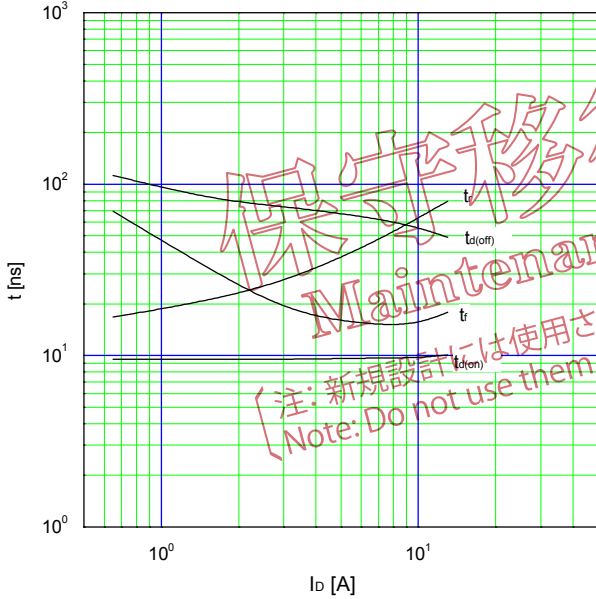
Typical Capacitance
 $C=f(V_{DS}):V_{GS}=0V,f=1MHz$



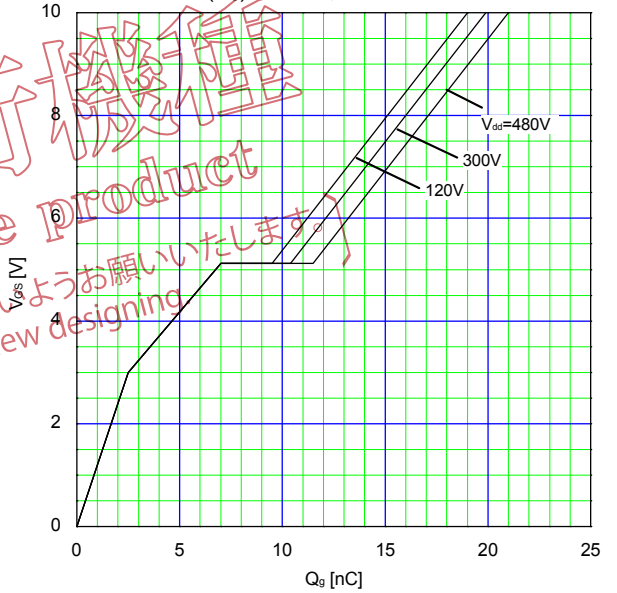
Typical Coss stored energy



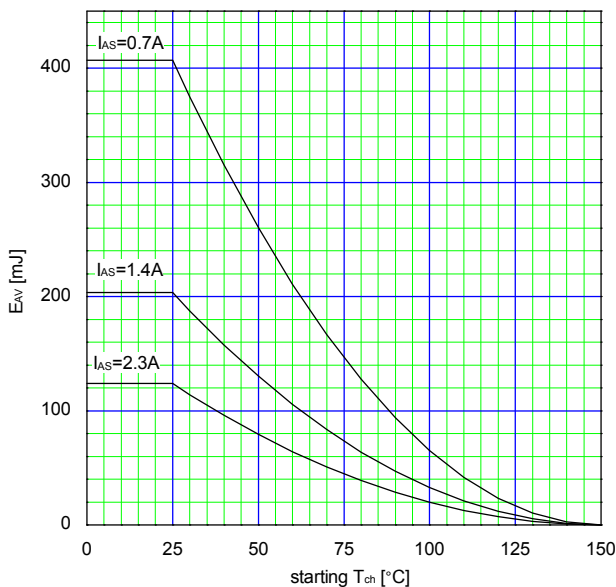
Typical Switching Characteristics vs. Id Tch=25°C
 $t=f(I_D):V_{dd}=400V,V_{GS}=10V/0V,R_G=36\Omega,L=500uH$



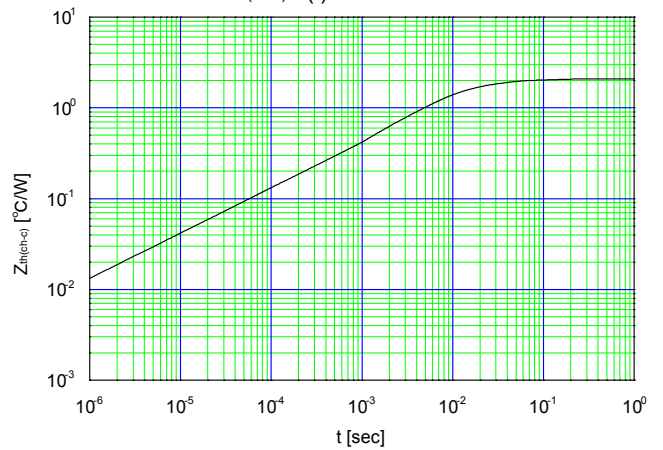
Typical Gate Charge Characteristics
 $V_{GS}=f(Q_g):I_D=6.5A,T_{ch}=25^\circ C$



Maximum Avalanche Energy vs. starting Tch
 $E_{(AV)}=f(\text{starting } T_{ch}):V_{CC}=60V,I_{(AV)}\leq 2.3A$



Transient Thermal Impedance
 $Z_{th(ch-c)}=f(t):D=0$



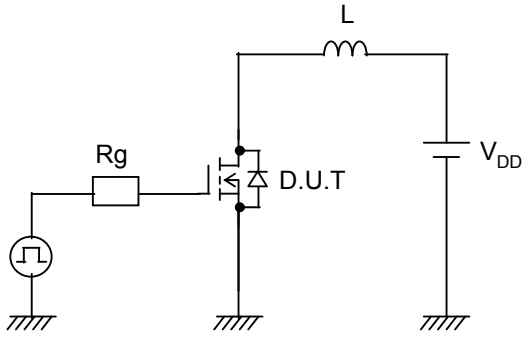


Fig.1 Avalanche Test circuit

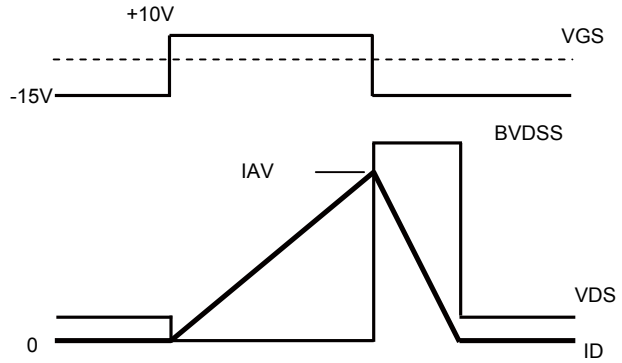


Fig.2 Operating waveforms of Avalanche Test

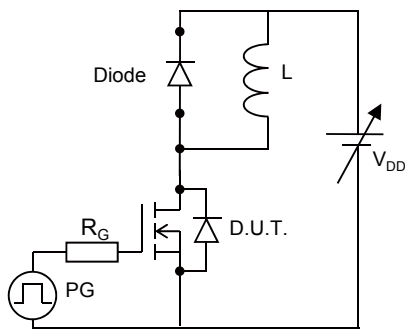


Fig.3 Switching Test circuit

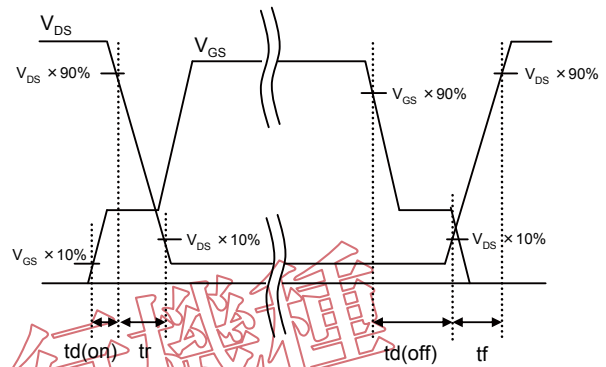


Fig.4 Operating waveform of Switching Test

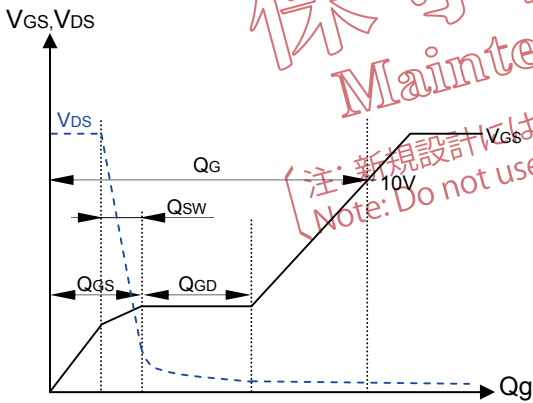


Fig.5 Operating waveform of Gate charge Test

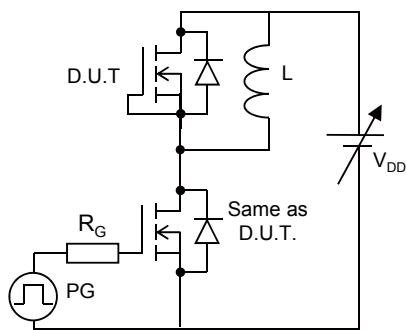


Fig.6 Reverse recovery Test circuit

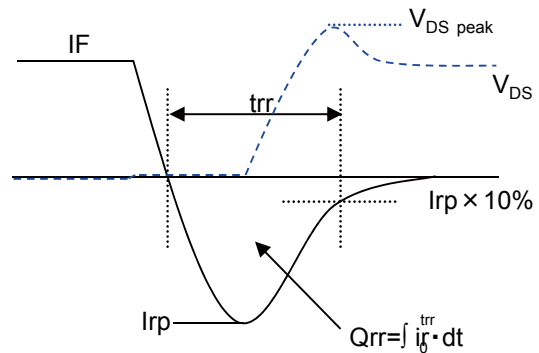
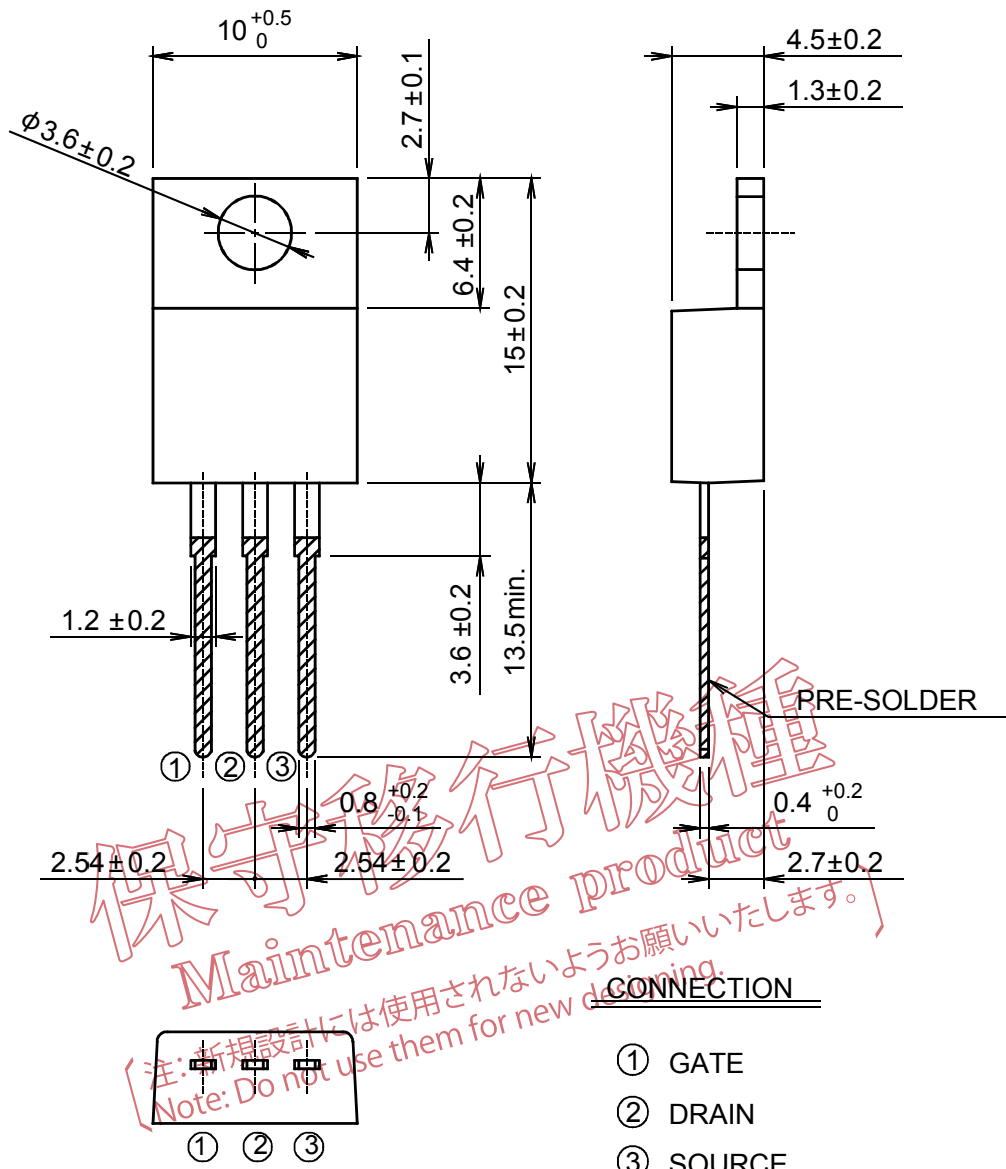


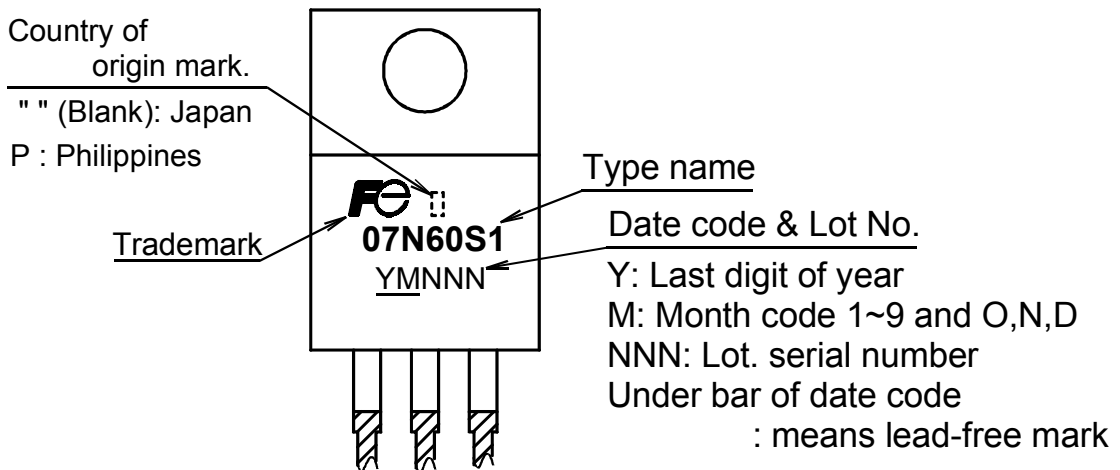
Fig.7 Operating waveform of Reverse recovery Test

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■ Outview: TO-220 Package



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