

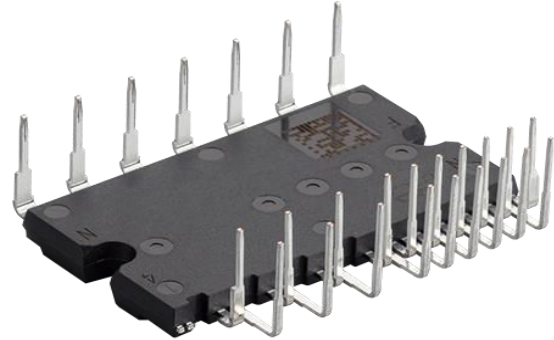
# 6MBP40XRVF065-50

IGBT Modules

IGBT Module (X series)  
650V / 40A / IPM

### Features

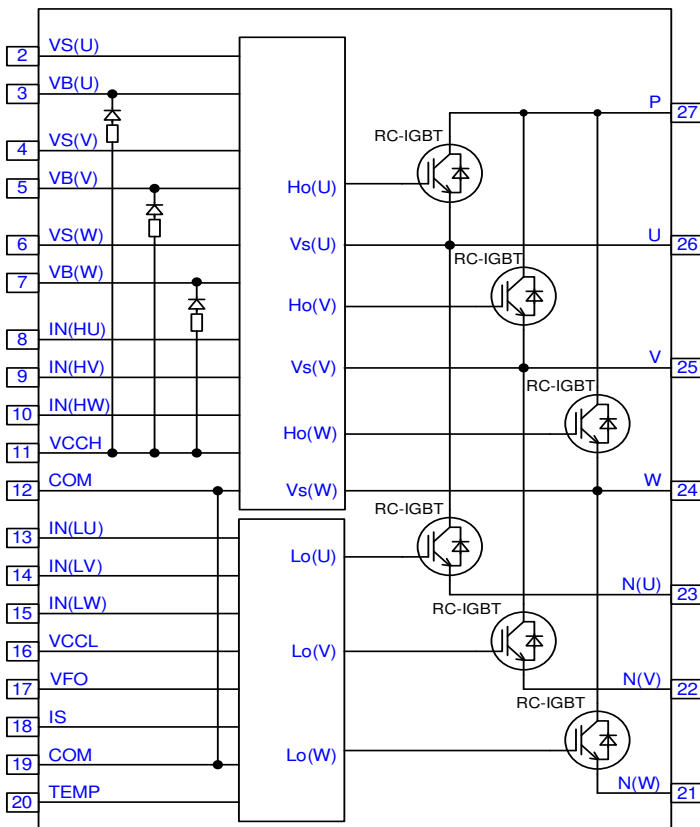
- Low-side RC-IGBTs are separate emitter type
- Short circuit protection
- Temperature sensor output function
- Overheating protection
- Under voltage protection
- Fault signal output function
- Input interface : TTL(3.3V/5V) Active high logic



### Applications

AC 100 ~ 240V (DC voltage 400V or below) three phase small power motor inverter drive.

### Terminal assign and Internal circuit



Pin No.	Pin Name	Pin Description
2	VS(U)	High-side U-phase drive supply GND
3	VB(U)	High-side bias voltage for U-phase IGBT driving
4	VS(V)	High-side V-phase drive supply GND
5	VB(V)	High-side bias voltage for V-phase IGBT driving
6	VS(W)	High-side W-phase drive supply GND
7	VB(W)	High-side bias voltage for W-phase IGBT driving
8	IN(HU)	Signal input for high side U-phase
9	IN(HV)	Signal input for high side V-phase
10	IN(HW)	Signal input for high side W-phase
11	V <sub>CCH</sub>	High-side control supply
12	COM	Common supply ground
13	IN(LU)	Signal input for low side U-phase
14	IN(LV)	Signal input for low side V-phase
15	IN(LW)	Signal input for low side W-phase
16	V <sub>CCL</sub>	Low-side control supply
17	VFO	Fault output
18	IS	Over current sensing voltage input
19	COM	Common supply ground
20	TEMP	Temperature sensor output
21	N(W)	Negative bus voltage input for W-phase
22	N(V)	Negative bus voltage input for V-phase
23	N(U)	Negative bus voltage input for U-phase
24	W	Motor W-phase output
25	V	Motor V-phase output
26	U	Motor U-phase output
27	P	Positive bus voltage input

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**IGBT Modules**
**■ Absolute maximum ratings ( $T_{vj}=25^{\circ}\text{C}$ ,  $T_c=25^{\circ}\text{C}$ ,  $V_{cc}=15\text{V}$  unless otherwise specified)**

Items		Symbol	Characteristics	Unit	Remarks
Inverter block	Collector-Emitter voltage(Terminal)	$V_{CE(\text{Surge})}$	500	V	Note*1
	Collector-Emitter voltage	$V_{CE(\text{chip})}$	650	V	Note*1
	Collector current	$I_C$	40	A	Note*2
	Peak collector current	$I_{CP}$	80	A	$V_{CC} \geq 15\text{V}$ , $V_{B(*)} \geq 15\text{V}$ Note*2,*3,*4
	Reverse-conducting current	$I_{RC}$	40	A	Note*2
	Peak reverse-conducting current	$I_{RCP}$	80	A	Note*2
	Power dissipation	$P_{D\_RC\text{-IGBT}}$	89.2	W	per single RC-IGBT $T_c=25^{\circ}\text{C}$
	Self operation "DC bus voltage" of circuit protection between upper-arm and lower-arm	$V_{DC(\text{SC})}$	400	V	$V_{CC}=V_{B(*)}=13.5\sim 16.5\text{V}$ $T_{vj}=125^{\circ}\text{C}$ , arm short circuit, non-repetitive less than 2 $\mu\text{s}$
	Virtual junction temperature	$T_{vj}$	+150	$^{\circ}\text{C}$	Note*8
	Operating virtual junction temperature (under switching conditions)	$T_{vjop}$	-40~+150	$^{\circ}\text{C}$	
Control circuit block	High-side supply voltage	$V_{CCH}$	-0.5~20	V	Applied between VCCH-COM
	Low-side supply voltage	$V_{CCL}$	-0.5~20	V	Applied between VCCL-COM
	High-side bias absolute voltage	$V_{VB(\text{U})\text{-COM}}$ $V_{VB(\text{V})\text{-COM}}$ $V_{VB(\text{W})\text{-COM}}$	-0.5~670	V	Applied between VB(U)-COM, VB(V)-COM, VB(W)-COM
	High-side bias voltage for IGBT gate driving	$V_{B(\text{U})}$ $V_{B(\text{V})}$ $V_{B(\text{W})}$	-0.5~20	V	Applied between VB(U)-U, VB(V)-V, VB(W)-W Note*4
	High-side bias offset voltage	$V_U$ $V_V$ $V_W$	-5~650	V	Applied between U-COM, V-COM, W-COM Note*5
	Input signal voltage	$V_{IN}$	-0.5~ $V_{CCH}+0.5$ -0.5~ $V_{CCL}+0.5$	V	Note*6
	Input signal current	$I_{IN}$	3	mA	sink current
	Fault signal voltage	$V_{FO}$	-0.5~ $V_{CCL}+0.5$	V	Applied between VFO-COM
	Fault signal current	$I_{FO}$	1	mA	sink current
	Over current sensing input voltage	$V_{IS}$	-0.5~ $V_{CCL}+0.5$	V	Applied between IS-COM
	Temp signal voltage	$V_{TEMP}$	-0.5 ~ 5.0	V	
	Temp signal current	$I_{TEMP}$	-0.05 / 3	mA	source / sink current
	Junction temperature	$T_{vj}$	150	$^{\circ}\text{C}$	
	Operating case temperature	$T_c$	-40~+125	$^{\circ}\text{C}$	See Fig.1-1
	Storage temperature	$T_{stg}$	-40~+125	$^{\circ}\text{C}$	
Isolation voltage	$V_{isol}$	AC 2000	Vrms	Sine wave,60Hz $t = 1\text{min}$ ,Note*7	
Mounting torque of screws	$M_s$	0.59~0.78	N·m	Mounting screw : M3	
Creepage distance	Between live terminal with high potential	$d_s$	3.00	mm	
	Between live terminal and heat sink	$d_a$	3.00	mm	
Clearance	Between live terminal with high potential	$d_s$	2.50	mm	
	Between live terminal and heat sink	$d_a$	1.55	mm	

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**IGBT Modules**
**Note**

\*1 :  $V_{CE(Surge)}$  is applied voltage between P-U,P-V,P-W or U-N(U),V-N(V),W-N(W).

$V_{CE(chip)}$  is Collector-Emitter voltage of internal RC-IGBT chip.

\*2 : Pulse width and duty are limited by  $T_{vj,max}$ .

\*3 :  $V_{CC}$  is applied between VCCH-COM,VCCL-COM.

\*4 :  $V_{B(*)}$  is applied between VB(U)-VS(U),VB(V)-VS(V), VB(W)-VS(W).

\*5 : Over 13.0V applied between VB(U)-VS(U),VB(V)-VS(V), VB(W)-VS(W). This IPM module might make incorrect response if the high-side bias offset voltage is less than -5V.

\*6 : Applied between IN(HU)-COM,IN(HV)-COM,IN(HW)-COM,IN(LU)-COM,IN(LV)-COM,IN(LW)-COM.

\*7 : Applied between shorted all terminal and isolation substrate.

\*8 : The maximum temperature during continuous operation is  $T_{vj}=150^{\circ}C$ .

The operating conditions have to be decided so that the temperature is below  $T_{vj}=150^{\circ}C$ .

Operation at over  $T_{vj}=150^{\circ}C$  may result in degradation of product lifetime such as power cycling capability.

## ■ Electrical characteristics

### ● Inverter block ( $T_{vj}=25^{\circ}C$ unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit	
Zero gate voltage collector current	$I_{CE}$	$V_{CE}=650V$	$T_{vj}=25^{\circ}C$	-	-	1	mA
		$V_{IN}=0V$	$T_{vj}=125^{\circ}C$	-	-	10	mA
Collector-Emitter saturation voltage	$V_{CE(sat)}$	$I_C=40A$	$T_{vj}=25^{\circ}C$	-	1.55	1.86	V
		$V_{CC}=+15V$ $V_{B(*)}=+15V$ $V_{IN}=5V$ $V_{IS}=0V$ Note *3, *4	$T_{vj}=125^{\circ}C$	-	1.70	2.05	
Reverse-conducting voltage	$V_{RC}$	$I_{RC}=40A$	$T_{vj}=25^{\circ}C$	-	1.45	1.75	V
		$V_{IN}=0V$	$T_{vj}=125^{\circ}C$	-	1.50	-	
Turn-on time	$t_{on}$	$V_{DC}=300V$		0.60	1.00	1.40	$\mu s$
Turn-on delay time	$t_{d(on)}$	$I_C=40A$		-	0.90	-	
Turn-on rise time	$t_r$	$V_{CC}=15V$		-	0.10	-	
$V_{CE}/I_C$ cross time of turn-on	$t_{c(on)}$	$V_{B(*)}=15V$		-	0.50	0.90	
Turn-off time	$t_{off}$	$T_{vj}=125^{\circ}C$		-	1.20	1.60	
Turn-off delay time	$t_{d(off)}$	$V_{IN}=0V \leftrightarrow 5V$		-	1.10	-	
Turn-off fall time	$t_f$	$V_{IS}=0V$		-	0.10	-	
$V_{CE}/I_C$ cross time of turn-off	$t_{c(off)}$	See Fig.2-1		-	0.35	0.70	
Reverse recovery time	$t_{rr}$	Note *3, *4		-	0.25	-	

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## Electrical characteristics

● Control circuit block ( $T_{vj}=25^{\circ}\text{C}$ ,  $V_{CC}=15\text{V}$ ,  $V_{B(*)}=15\text{V}$ ,  $V_{IN}=0\text{V}$ ,  $V_{IS}=0\text{V}$  unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit	
Circuit current of low-side	$I_{CCL}$	$V_{CCL}=15\text{V}$ $V_{IN}=5\text{V}$	-	0.6	0.9	mA	
		$V_{CCL}=15\text{V}$ $V_{IN}=0\text{V}$	-	0.6	0.9		
Circuit current of high-side	$I_{CCH}$	$V_{CCH}=15\text{V}$ $V_{IN}=5\text{V}$	-	0.8	1.9	mA	
		$V_{CCH}=15\text{V}$ $V_{IN}=0\text{V}$	-	0.8	1.9		
Circuit current of bootstrap circuit (per one unit)	$I_{CCHB}$	$V_{B(U)}=15\text{V}$ , $V_{B(V)}=15\text{V}$ , $V_{B(W)}=15\text{V}$	$V_{IN}=5\text{V}$	-	-	0.20	mA
			$V_{IN}=0\text{V}$	-	-	0.20	
Input signal threshold voltage	$V_{th(on)}$	$PW \geq 0.7\mu\text{s}$	1.20	1.70	2.35	V	
	$V_{th(off)}$		0.80	1.30	1.80		
Input signal threshold hysteresis voltage	$V_{th(hys)}$		0.25	0.40	-	V	
Operational input pulse width of turn-on	$t_{IN(ON)}$	$V_{IN}=0\text{V}$ to $5\text{V}$ rise up Note*6	0.2	-	-	$\mu\text{s}$	
Operational input pulse width of turn-off	$t_{IN(OFF)}$	$V_{IN}=5\text{V}$ to $0\text{V}$ fall down Note*6	0.2	-	-	$\mu\text{s}$	
Input current	$I_{IN}$	$V_{IN}=5\text{V}$ Note*6	0.7	1.0	1.5	mA	
Input pull-down resistance	$R_{IN}$	Note*6	3.3	5.0	7.2	k $\Omega$	
Fault output voltage	$V_{FO(H)}$	$V_{IS}=0\text{V}$ , $V_{FO}$ terminal pull up to $5\text{V}$ by $10\text{k}\Omega$	4.9	-	-	V	
	$V_{FO(L)}$	$V_{IS}=1\text{V}$ , $I_{FO}=1\text{mA}$	-	-	0.95	V	
Fault output pulse width	$t_{FO}$	Note*9 See Fig.2-2	20	-	-	$\mu\text{s}$	
Over current protection voltage level	$V_{IS(ref)}$	$V_{CC}=15\text{V}$	0.455	0.480	0.505	V	
Over current protection delay time	$t_{d(IS)}$	Note*3,*10	0.3	0.8	1.3	$\mu\text{s}$	
Output voltage of temperature sensor	$V_{(temp)}$	Note*11	$T_{vj(LVIC)}=90^{\circ}\text{C}$	2.63	2.77	2.91	V
			$T_{vj(LVIC)}=25^{\circ}\text{C}$	0.88	1.13	1.39	
LVIC overheating protection	$T_{vjOH}$	Note*11	136	143	150	$^{\circ}\text{C}$	
$T_{OH}$ hysteresis	$T_{vjOH(hys)}$	See Fig.2-6	4	10	20		
$V_{CC}$ under voltage trip level of low-side	$V_{CCL(OFF)}$	$T_{vj}<150^{\circ}\text{C}$	10.3	-	12.5	V	
$V_{CC}$ under voltage reset level of low-side	$V_{CCL(ON)}$	See Fig.2-3	10.8	-	13.0		
$V_{CC}$ under voltage hysteresis	$V_{CCL(hys)}$		-	0.5	-		
$V_{CC}$ under voltage trip level of high-side	$V_{CCH(OFF)}$	$T_{vj}<150^{\circ}\text{C}$	8.3	-	10.3	V	
$V_{CC}$ under voltage reset level of high-side	$V_{CCH(ON)}$	See Fig.2-4	8.8	-	10.8		
$V_{CC}$ under voltage hysteresis	$V_{CCH(hys)}$		-	0.5	-		
$V_B$ under voltage trip level	$V_{B(OFF)}$	$T_{vj}<150^{\circ}\text{C}$	10.0	-	12.0	V	
$V_B$ under voltage reset level	$V_{B(ON)}$	See Fig.2-5	10.5	-	12.5		
$V_B$ under voltage hysteresis	$V_{B(hys)}$		-	0.5	-		
Forward voltage of bootstrap diode	$V_{F(BSD)}$	$T_{vj}=25^{\circ}\text{C}$ $I_{F(BSD)}=10\text{mA}$	1.5	1.7	1.9	V	
Built-in limiting series resistance (BSD)	$R_{S(BSD)}$	$T_{vj}=25^{\circ}\text{C}$	80	100	120	$\Omega$	

Note

\*9 : Fault signal is asserted corresponding to “Over-current protection”, “Under-voltage protection” at low-side, and “Overheat protection”.

Under the condition of “Over-current protection”, “Under-voltage protection” or “Overheat protection”, the fault signal is asserted continuously while these conditions are continuing.

However, the minimum fault output pulse width is minimum  $20\mu\text{sec}$  even if very short failure condition (which is less than  $20\mu\text{s}$ ) is triggered.

\*10 : Over current protection is functioning only for the low-side arms.

\*11 : Fig.1-1 shows the measurement position of temperature sensor.

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## Thermal characteristic( $T_c=25^\circ\text{C}$ )

Description	Symbol	min.	typ.	max.	Unit
Junction to case thermal resistance (per single RC-IGBT) Note*12	$R_{th(j-c)}$	-	-	1.4	$^\circ\text{C/W}$

Note

\*12 : Thermal compound with good thermal conductivity should be applied evenly with about  $+100\mu\text{m}\sim+200\mu\text{m}$  on the contacting surface of this device and heat-sink.

## Mechanical characteristics( $T_c=25^\circ\text{C}$ )

Description	Symbol	Conditions	min.	typ.	max.	Unit
Mounting torque of screws	$M_S$	Mounting screw : M3	0.59	0.69	0.78	$\text{N}\cdot\text{m}$
Heat-sink side flatness	-	Insulation substrate part See (A1),(A2) of Fig.1-2	-30	-	80	$\mu\text{m}$
Weight	-	-	-	5.6	-	g
Resistance to soldering heat	-	Solder temp : $260 \pm 5^\circ\text{C}$ Immersion time : $10 \pm 1\text{s}$ Solder alloy : Sn-Ag-Cu type	-	-	1	time

Fig.1-1 :  
The measurement position of case temperature

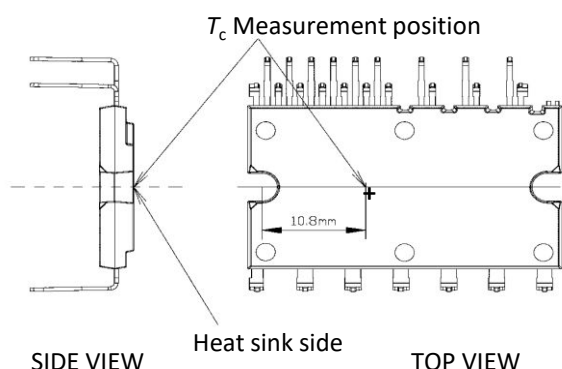
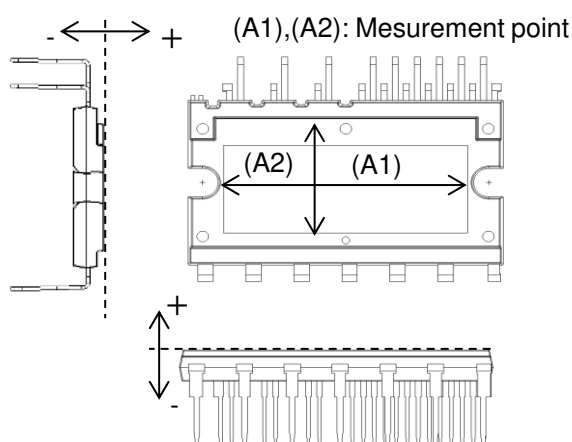


Fig.1-2 :  
The measurement position of heat sink flatness



Depending on the control method, the point at which  $T_c$  is highest may differ from the above. In such cases, it is necessary to change the measurement point and measure  $T_c$  directly under the chip where the loss is highest.

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**IGBT Modules**
**■ Recommend operation conditions(Note\*15)**

Description	Symbol	min.	typ.	max.	Unit
DC bus voltage	$V_{DC}$	0	300	400	V
High-side bias voltage for IGBT gate driving	$V_{B(*)}$	13.0	15.0	18.5	V
High-side supply voltage	$V_{CCH}$	13.5	15.0	16.5	V
Low-side supply voltage	$V_{CCL}$	13.5	15.0	16.5	V
Control supply variation (under swiching conditions)	$\Delta V_B$	-1	-	1	V/ $\mu$ s
	$\Delta V_{CC}$	-1	-	1	
Input signal voltage	$V_{IN}$	0	-	5	V
Voltage for current sensing	$V_{IS}$	0	-	5	V
Potential difference of between COM to N (including surge)	$V_{COM\_N}$	-5	-	5	V
Dead time for preventing arm-short ( $T_c \leq 125^\circ\text{C}$ )	$t_{DEAD}$	1.0	-	-	$\mu$ s
Minimum input pulse widht (Note*13,Note*14)	$PW_{IN(on)}$	0.5	-	-	$\mu$ s
	$PW_{IN(off)}$	0.7	-	-	$\mu$ s
PWM input frequency	$f_{PWM}$	-	-	20	kHz
Operating virtual junction temperature	$T_{vjop}$	-40	-	150	$^\circ\text{C}$

**Note**

\*13 : In the pulse width of 0.5 $\mu$ s, the loss of RC-IGBT increases for the saturation operation.

To reduce the loss of RC-IGBT, please enlarge the pulse width more than the switching time of RC-IGBT.

\*14 : This IPM module might response according to input signal pulse even when the input signal pulse width is less than  $PW_{IN(on)}$  and  $PW_{IN(off)}$ .

\*15 : Recommended operating conditions are conditions for guaranteeing that the product operates normally.

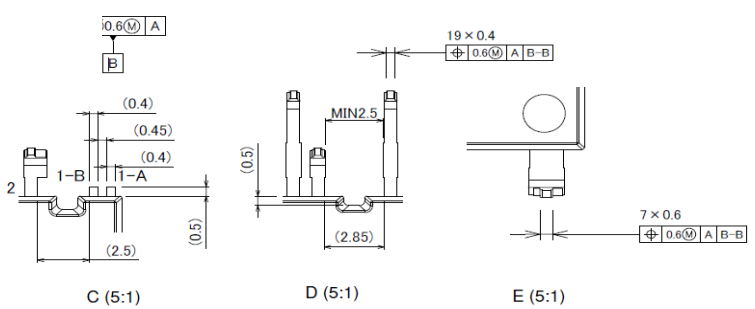
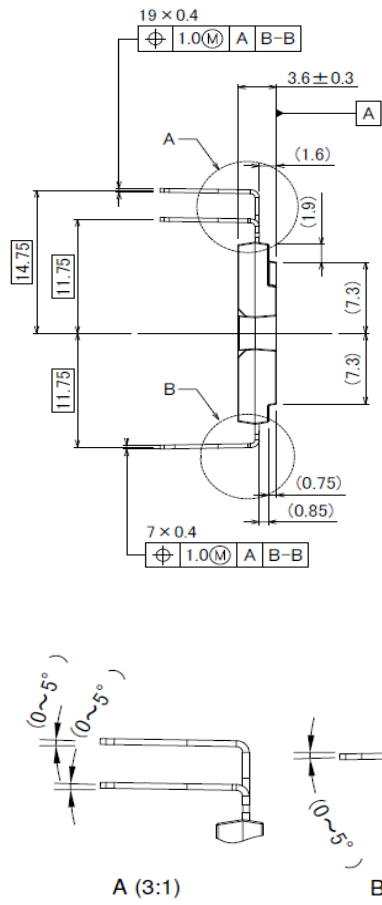
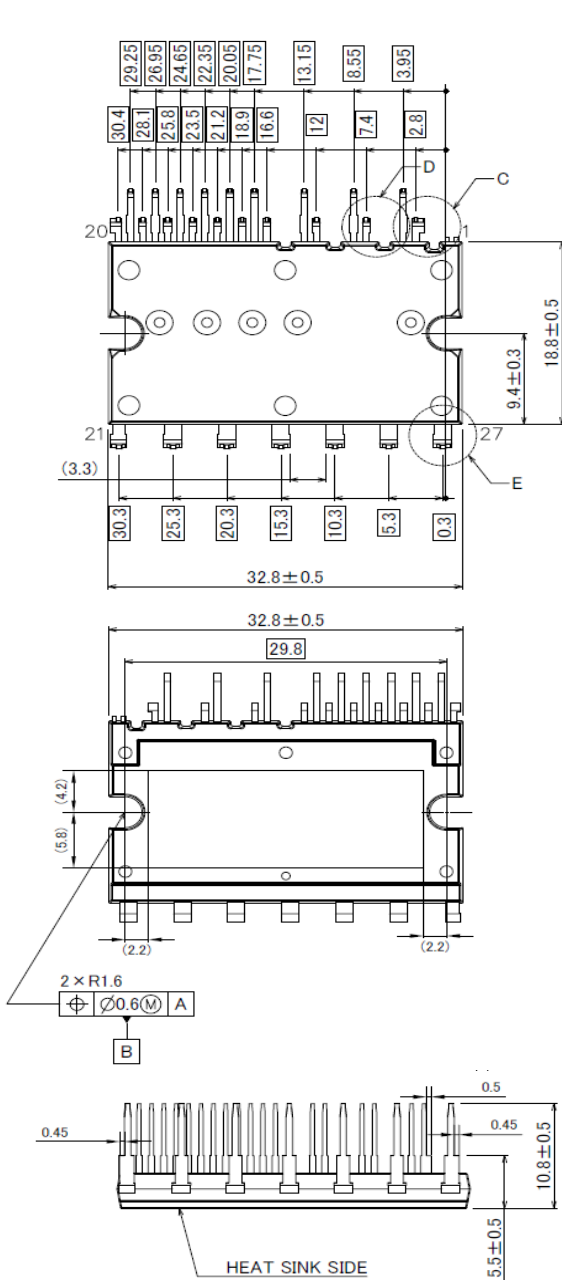
If it is used beyond this condition, operation and reliability may be adversely affected.

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IGBT Modules

■ Packing outline dimensions ( $T_c=25^\circ\text{C}$ )

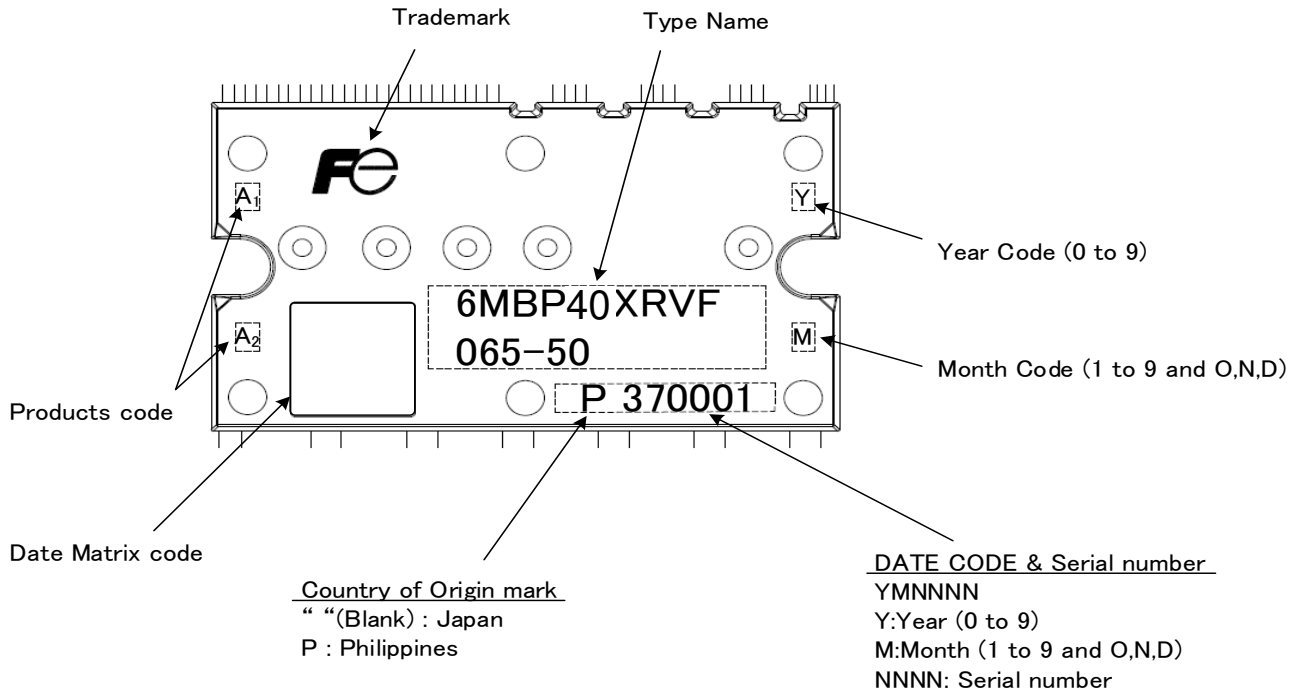
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1a	( COM )	10	IN(HW)	20	TEMP
1b	( VCCH )	11	VCCH	21	N(W)
2	VS(U)	12	COM	22	N(V)
3	VB(U)	13	IN(LU)	23	N(U)
4	VS(V)	14	IN(LV)	24	W
5	VB(V)	15	IN(LW)	25	V
6	VS(W)	16	VCCL	26	U
7	VB(W)	17	VFO	27	P
8	IN(HU)	18	IS		
9	IN(HV)	19	COM		



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IGBT Modules

■ **Marking**



**Note**

Product code A<sub>1</sub> means current ratings , and “N” is marked.

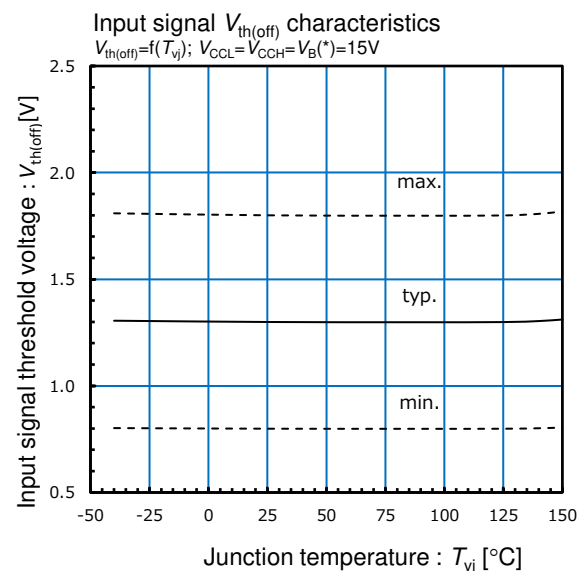
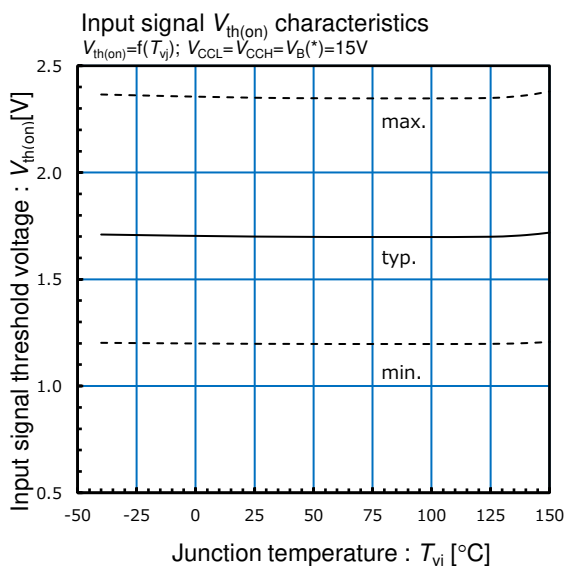
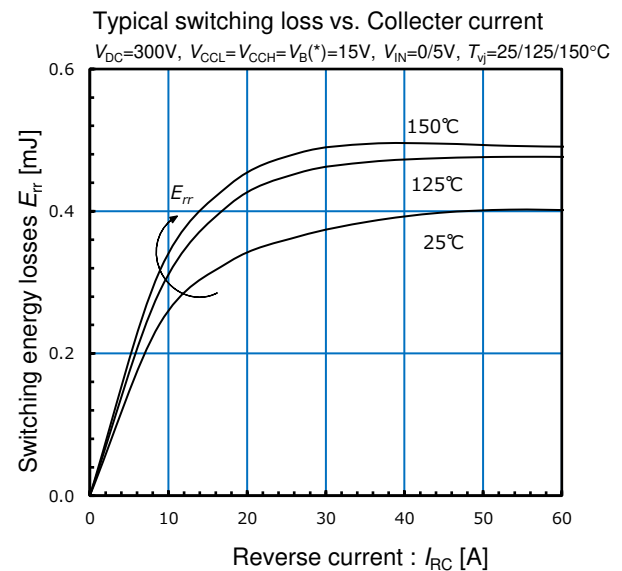
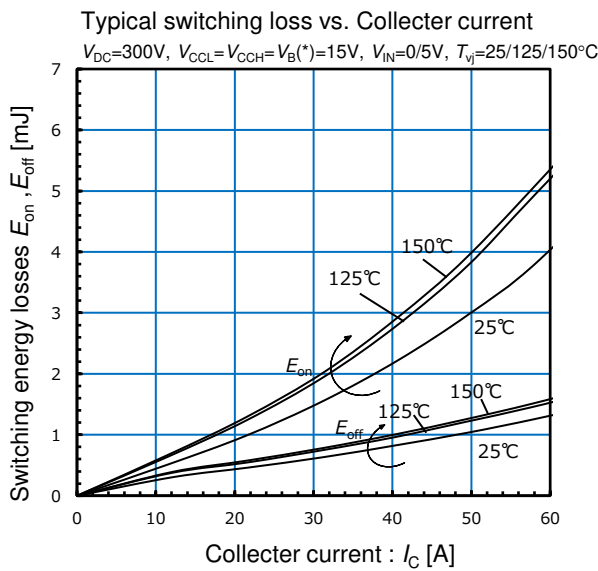
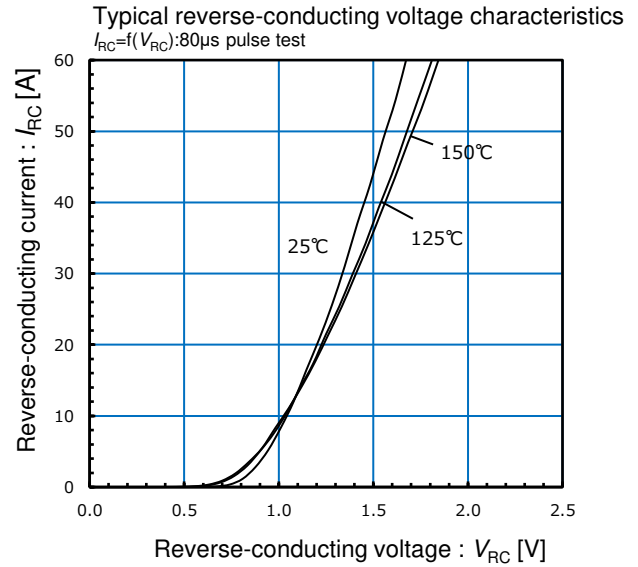
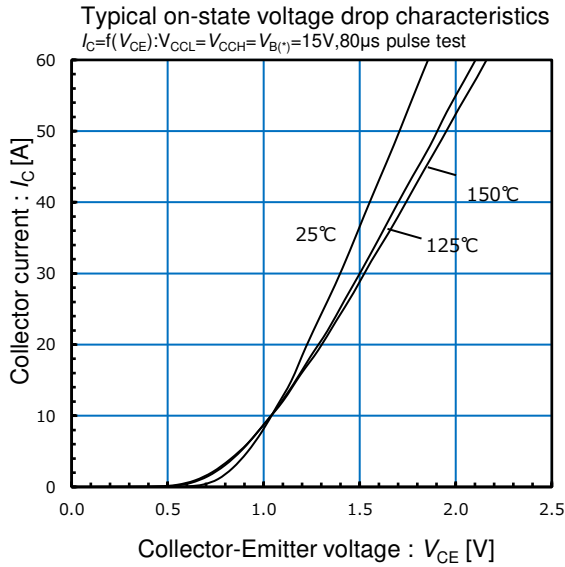
Product code A<sub>2</sub> means variations , and “F” is marked.

Data matrix is not covered by warranty.

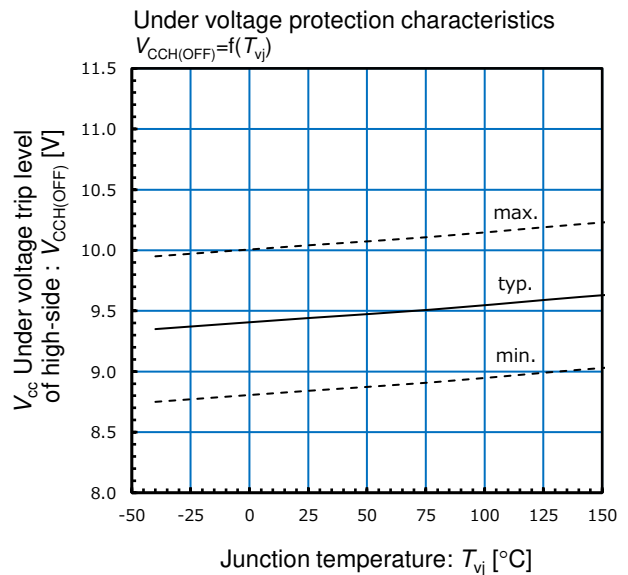
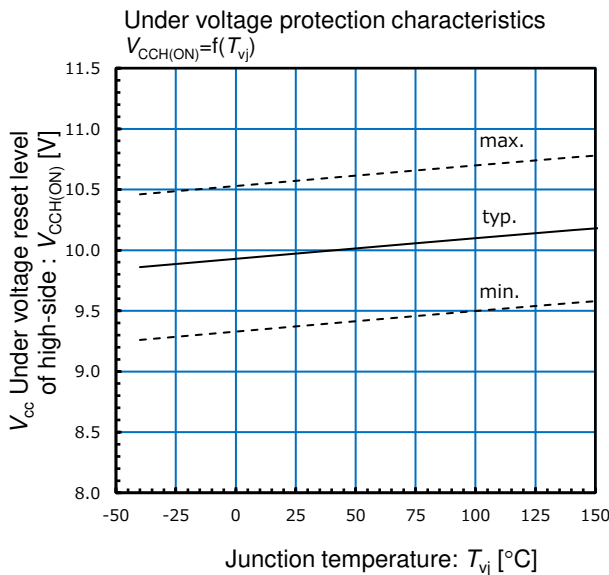
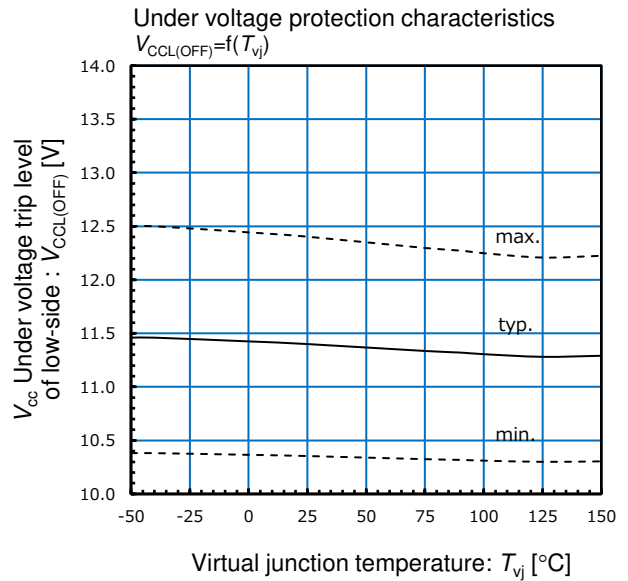
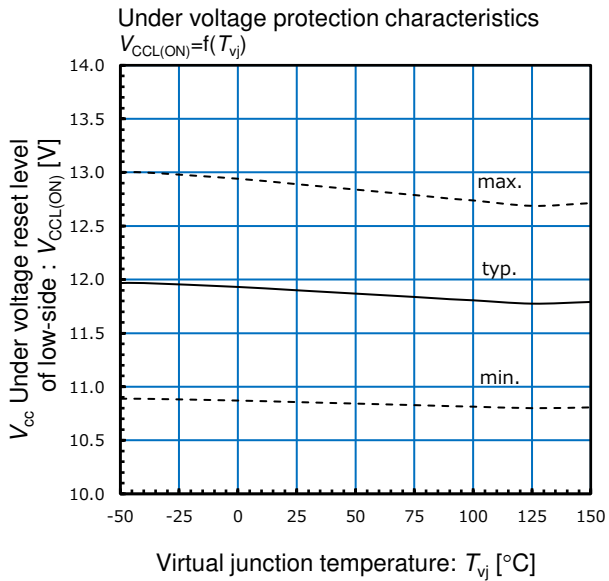
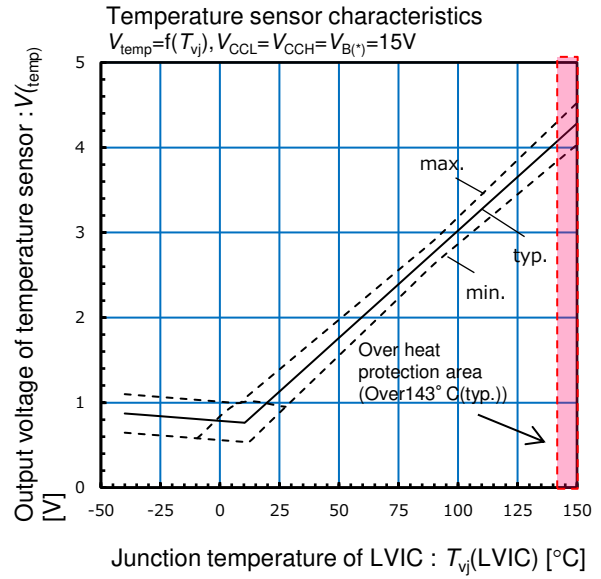
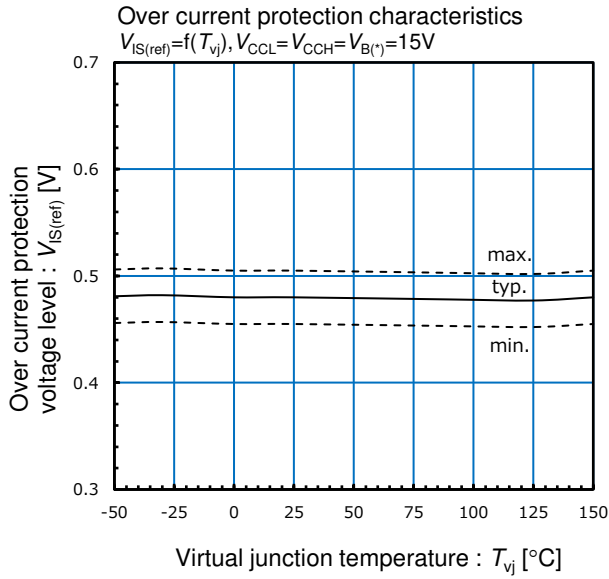
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## DC typical characteristics

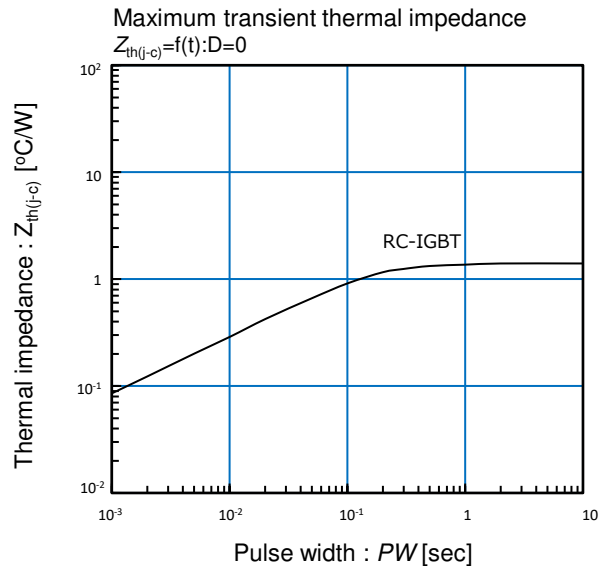
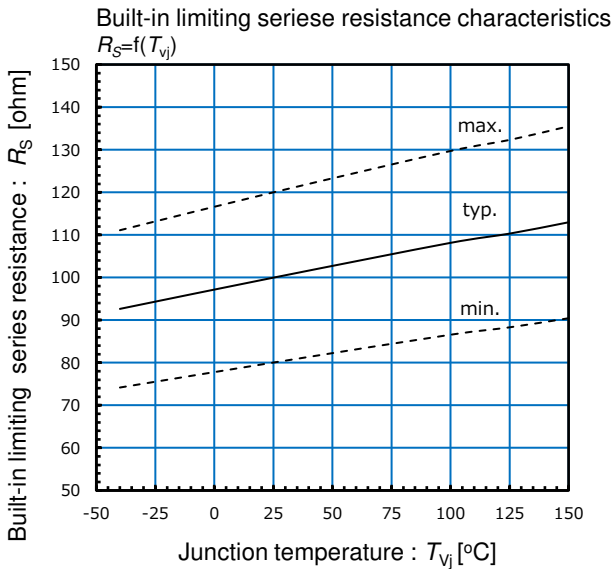
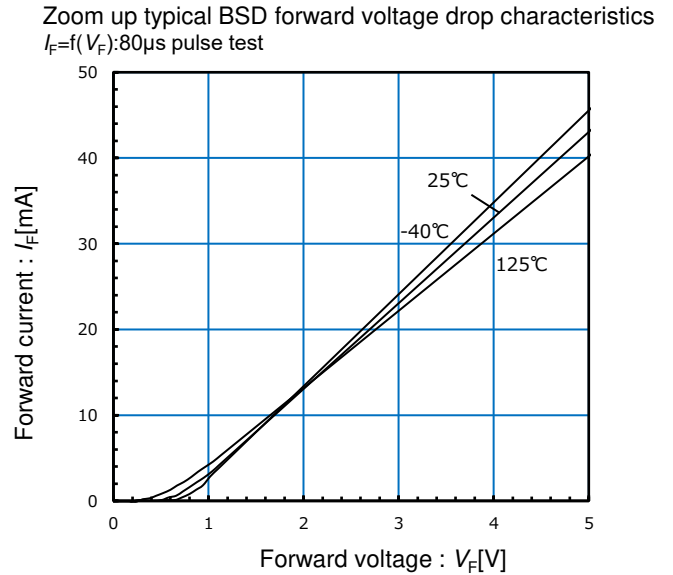
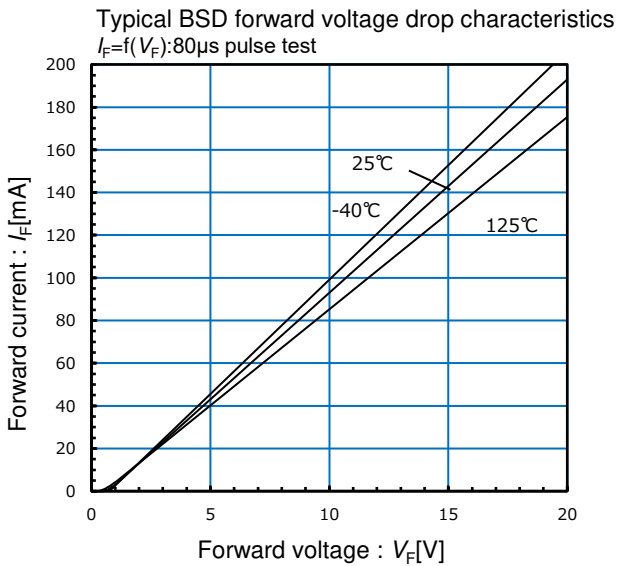
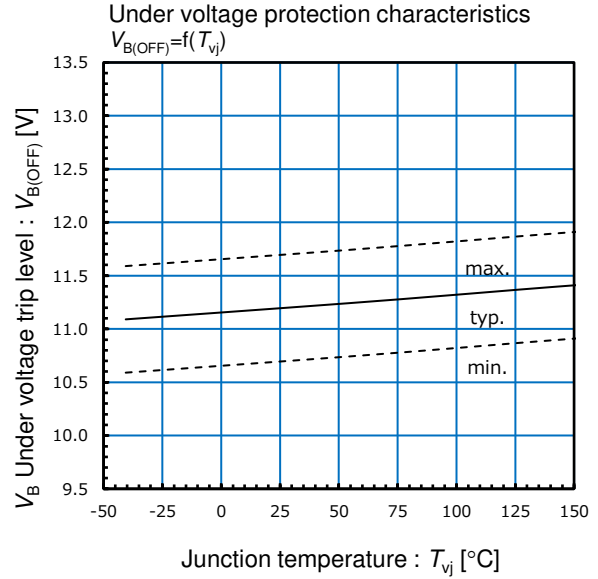
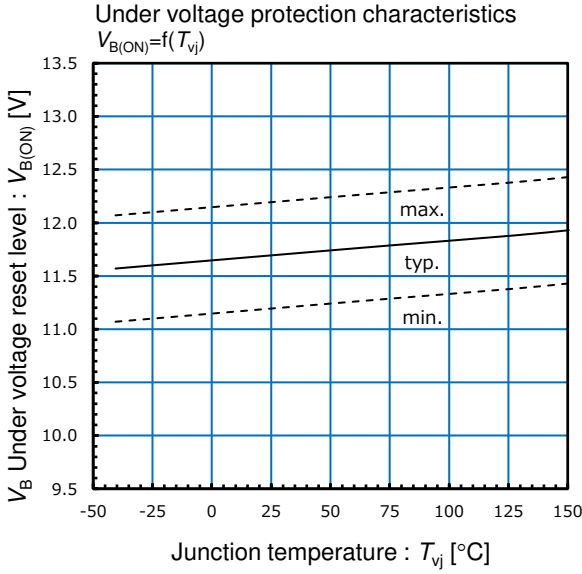


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IGBT Modules

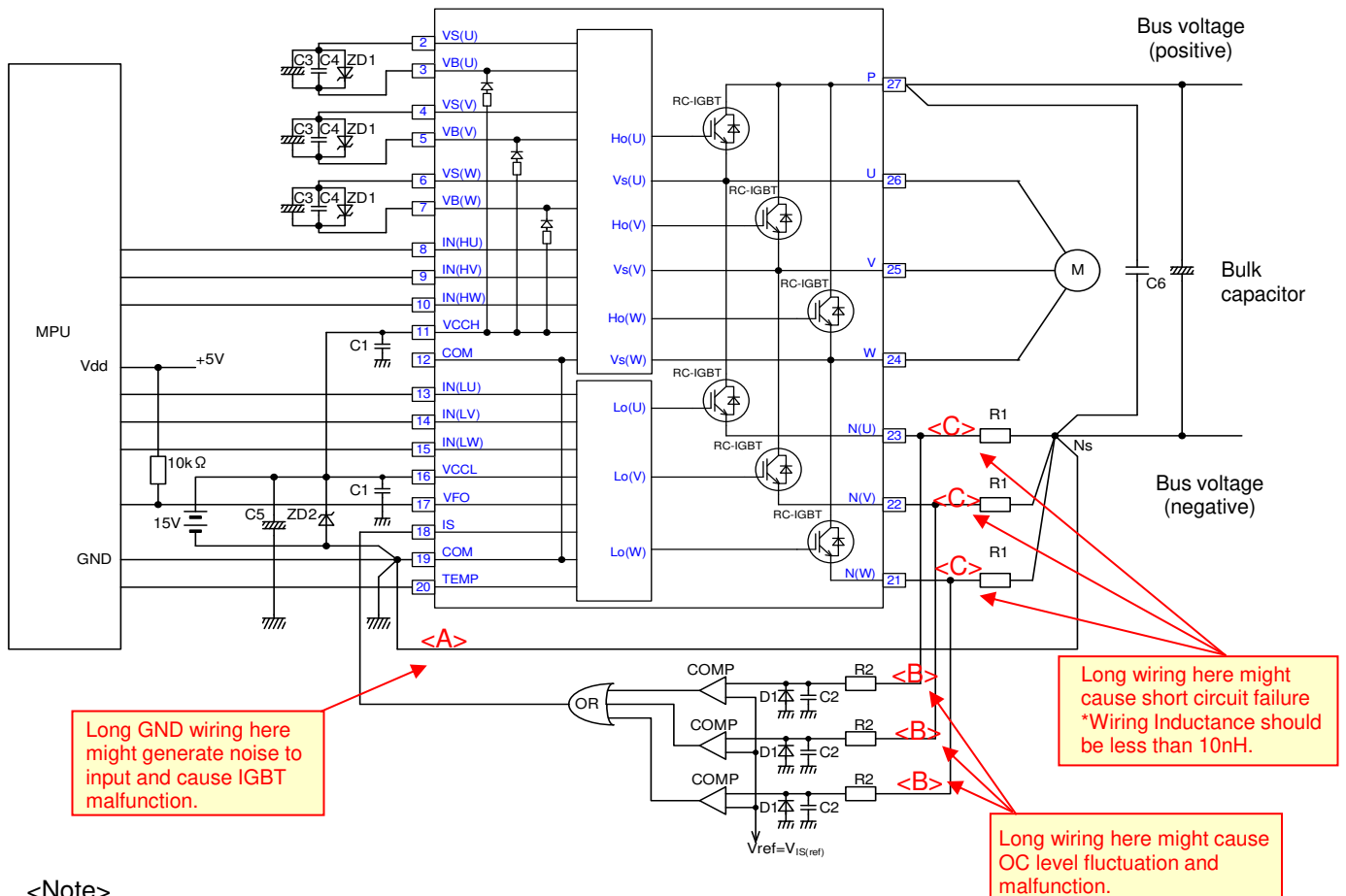


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IGBT Modules

■ An example of application circuit.

● Fig.shows an example of an application circuit.



<Note>

1. Input signal for drive is High-Active. There is a pull-down resistor built in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using R-C coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
2. By the function of the HVIC, it is possible of the direct coupling to microprocessor (MPU) without any photo-coupler or pulse-transformer isolation.
3.  $V_{FO}$  output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10k $\Omega$ .
4. To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 0.7 $\mu$ s. Over current (OC) shutdown time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. Please set the threshold voltage of the comparator reference input to be same as the IPM OC trip reference voltage  $V_{IS(ref)}$ .
7. Please use high speed type comparator and logic IC to detect OC condition quickly.
8. If negative voltage of R1 at the switching timing is applied, the schottky barrier diode D1 is recommended to be inserted parallel to R1.
9. All capacitors should be mounted as close to the terminals of the IPM as possible. (C1, C4 : narrow temperature drift, higher frequency and DC bias characteristic ceramic type are recommended, and C3, C5: select electrolytic type considering allowable ripple current and lifespan)
10. To prevent surge destruction, the wiring between the snubber capacitor and the P terminal, Ns node should be as short as possible. Generally a 0.1 $\mu$  to 0.22 $\mu$ F snubber capacitor (C6) between the P terminal and Ns node is recommended.
11. Two COM terminals (12 & 19 pin) are connected inside the IPM, it must be connected either one to the signal GND outside and leave another one open.
12. It is recommended to insert a zener-diode (22V) between each pair of control supply terminals to prevent surge destruction.
13. If signal GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect signal GND and power GND at only a point.

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## Operation sequence

Fig.2-1 Switching waveforms

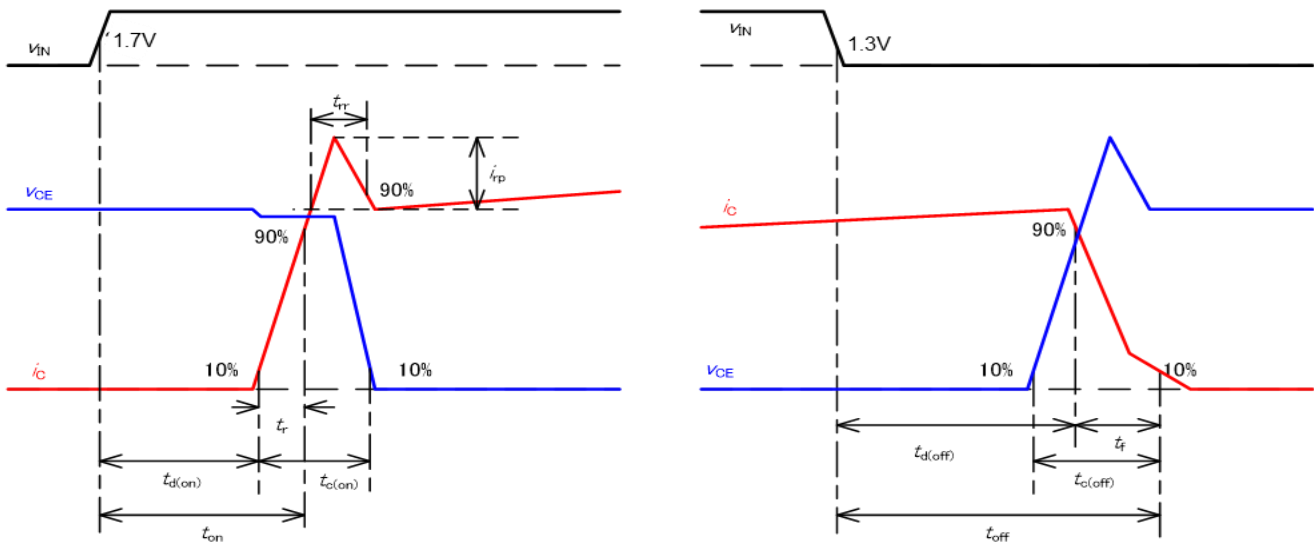
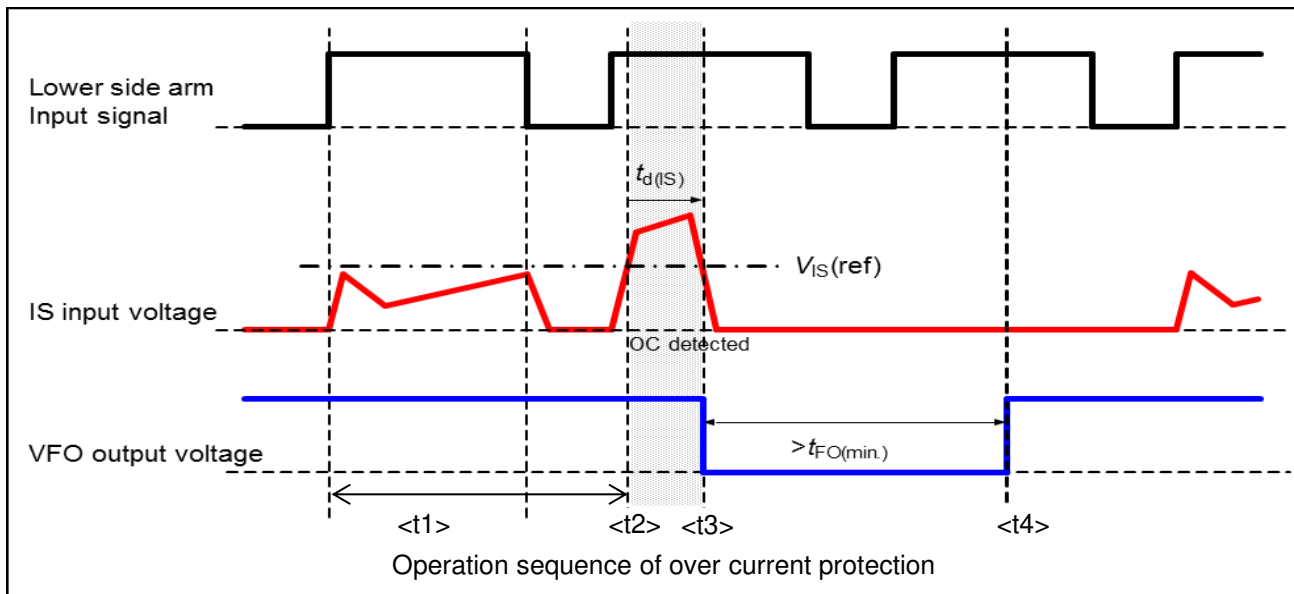


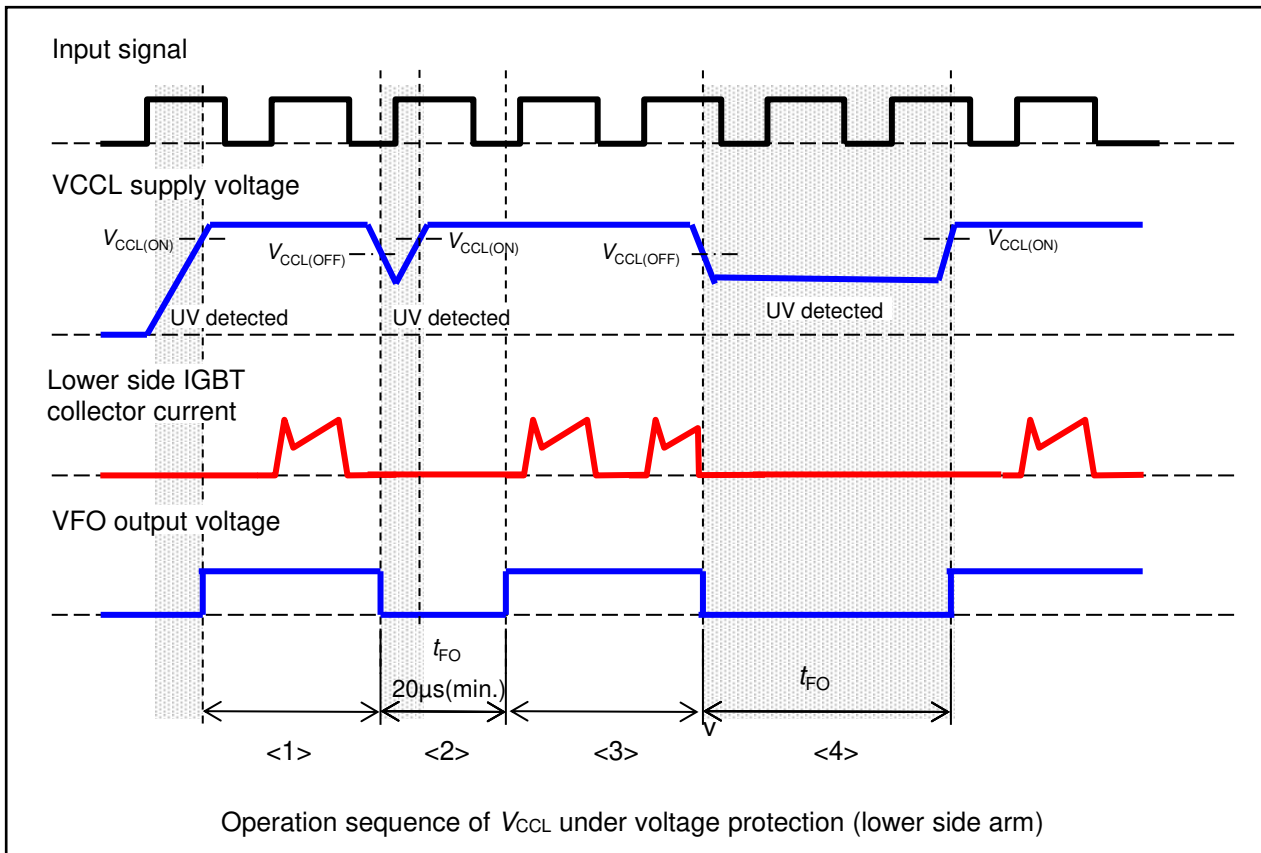
Fig.2-2 Operation sequence of over current protection



- <t1> : IS input voltage does not exceed  $V_{IS(ref)}$ , while the collector current of the lower side IGBT is under the normal operation.
- <t2> : When IS input voltage exceeds  $V_{IS(ref)}$ , the OC is detected.
- <t3> : The fault output  $V_{FO}$  is activated and all lower side IGBT shut down simultaneously after the over current protection delay time  $t_{d(IS)}$ . Inherently there is dead time of LVIC in  $t_{d(IS)}$ .
- <t4> : After the fault output pulse width  $t_{FO}$ , the OC is reset. Then next input signal is activated.

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Fig.2-3 Operation sequence of  $V_{CCL}$  Under voltage protection (lower side arm)

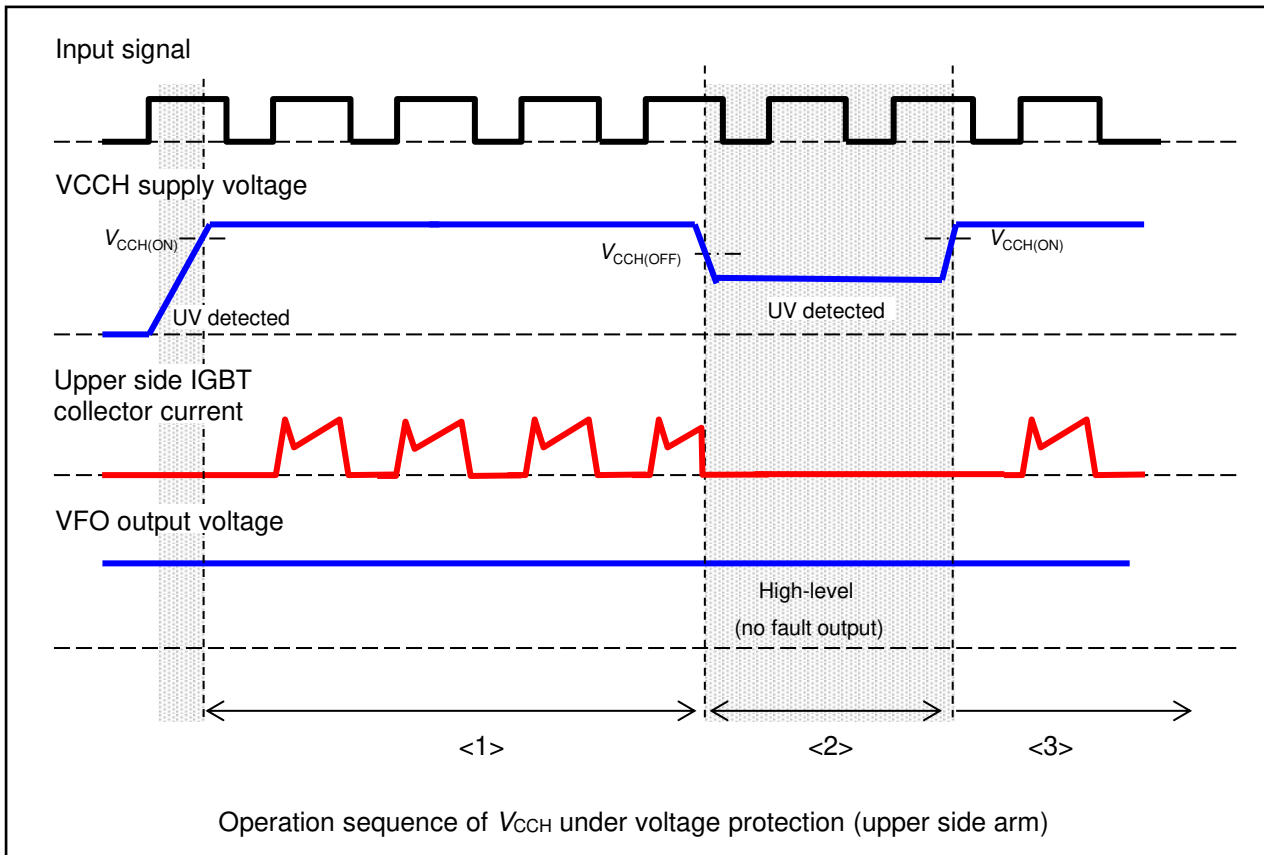


When  $V_{CCL}$  is under 4V, UV and fault output are not activated.

- <1> When  $V_{CCL}$  is under  $V_{CCL(ON)}$ , all lower side IGBTs are OFF state.  
After  $V_{CCL}$  rises to  $V_{CCL(ON)}$ , the fault output  $V_{FO}$  is released (high level).  
And the LVIC starts to operate, then next input is activated.
- <2> The fault output VFO is activated when  $V_{CCL}$  falls below  $V_{CCL(OFF)}$ , and all lower side IGBT remains OFF state.  
When the voltage drop time is less than  $20\mu s$ , the fault output pulse width is generated minimum  $20\mu s$  and all lower side IGBTs are OFF state in spite of input signal condition during that time.
- <3> UV is reset after  $t_{FO}$  when  $V_{CCL}$  exceeds  $V_{CCL(ON)}$  and the fault output  $V_{FO}$  is reset simultaneously.  
And the LVIC starts to operate, then next input is activated.
- <4> When the voltage drop time is more than  $t_{FO}$ , the fault output pulse width is generated and all lower side IGBTs are OFF state in spite of input signal condition during the same time.

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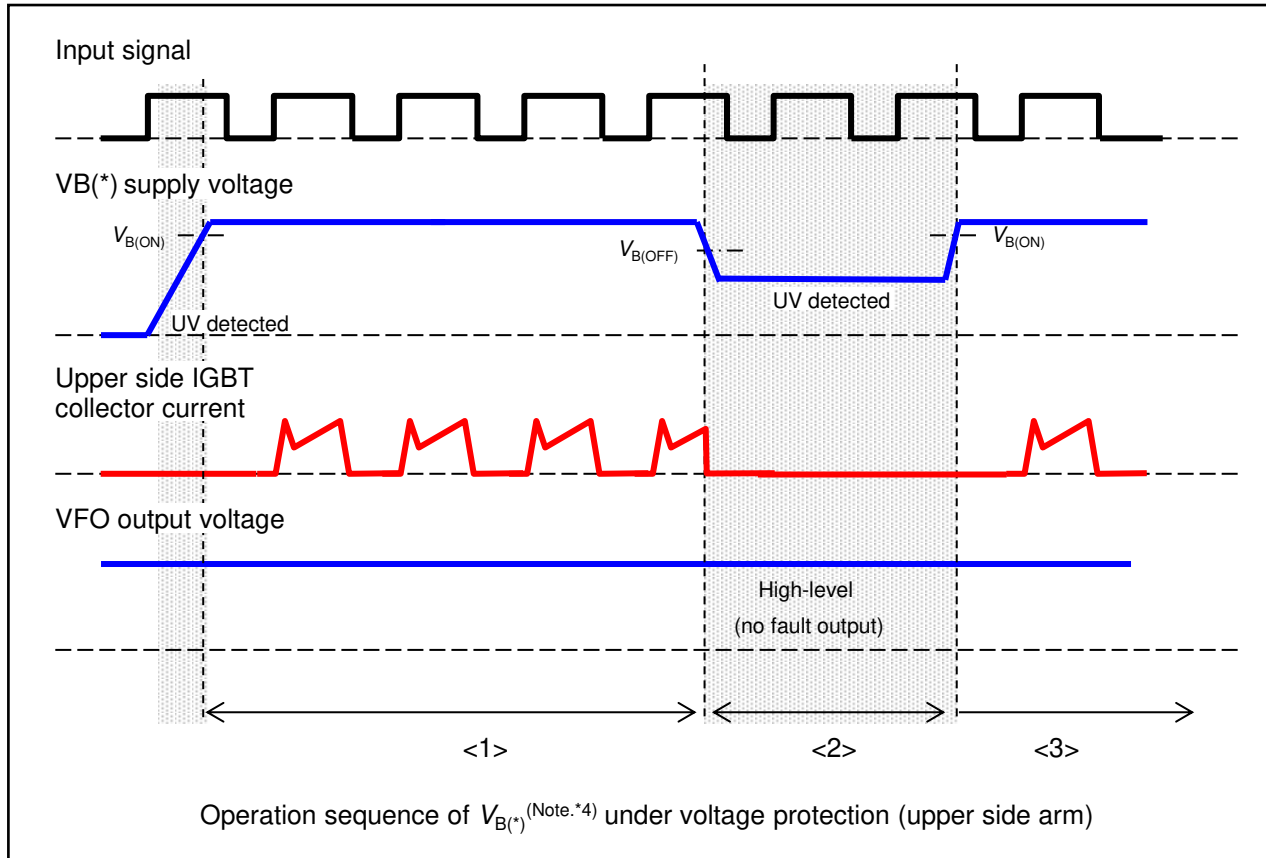
Fig.2-4 Operation sequence of  $V_{CCH}$  under voltage protection (upper side arm)



- <1> When  $V_{CCH}$  is under  $V_{CCH(ON)}$ , the upper side IGBT is OFF state.  
After  $V_{CCH}$  exceeds  $V_{CCH(ON)}$ , the HVIC starts to operate. Then next input is activated.  
The fault output  $V_{FO}$  is constant (high level) not depending on  $V_{CCH}$ .
- <2> After  $V_{CCH}$  falls below  $V_{CCH(OFF)}$ , the upper side IGBT remains OFF state.  
But the fault output  $V_{FO}$  remains at high level.
- <3> The HVIC starts to operate after UV is reset, then next input is activated.

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Fig.2-5 Operation sequence of  $V_{B(*)}$  under voltage protection (upper side arm)



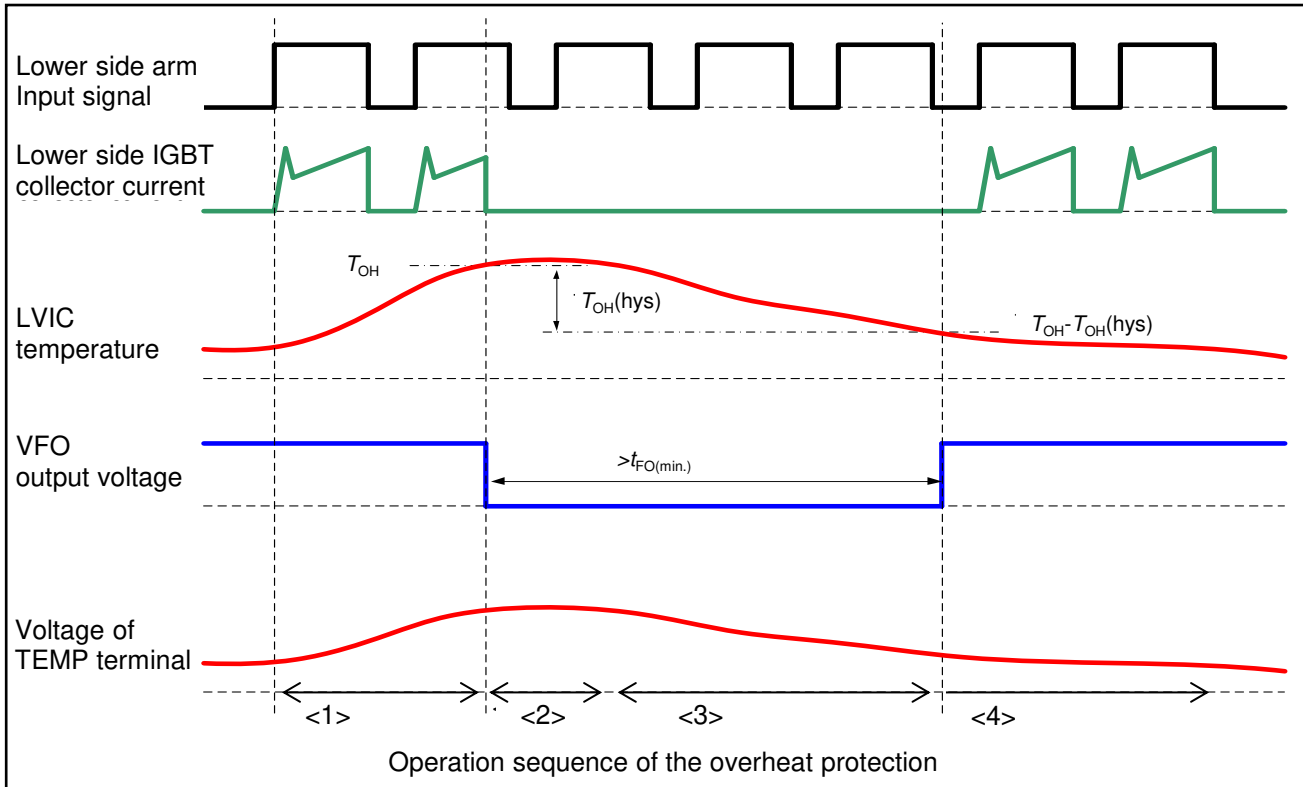
Operation sequence of  $V_{B(*)}$  (Note.\*4) under voltage protection (upper side arm)

- <1> When  $V_{B(U)}$ ,  $V_{B(V)}$  or  $V_{B(W)}$  are under  $V_{B(ON)}$ , the corresponding upper side IGBTs are OFF state. After  $V_{B(U)}$ ,  $V_{B(V)}$  or  $V_{B(W)}$  exceed  $V_{B(ON)}$ , the corresponding upper side IGBTs start to operate. Then next input is activated. The fault output  $V_{FO}$  is constant (high level) not depending on  $V_{B(*)}$ . (Note\*16)
- <2> After  $V_{B(U)}$ ,  $V_{B(V)}$  or  $V_{B(W)}$  fall below  $V_{B(OFF)}$ , the corresponding upper side IGBTs remain OFF state. But the fault output  $V_{FO}$  keeps high level.
- <3> The HVIC starts to operate after UV is reset, then next input is activated.

Note \*16 : The fault output is not given HVIC bias conditions.

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**Fig.2-6 Overheat protection**



The IPM has Overheat protection (OH) function by monitoring the LVIC temperature. The  $T_{OH}$  sensor position is shown in Fig.1-1.

- <1> The collector current of the lower side IGBT is under the normal operation while the LVIC temperature does not exceed  $T_{OH}$ .
- <2> The IPM shutdown all lower side IGBTs while the LVIC temperature exceeds  $T_{OH}$ .
- <3> The TEMP terminal continue to output the voltage which correspond to temperature of LVIC even if IPM is in OH condition.
- <4> The fault status is reset when the LVIC temperature drops below  $(T_{OH} - T_{OH(hys.)})$ . All lower side IGBTs restart to normal operation.

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