Fuji Electric **Innovating Energy Technology**

FML60N093S2FDHF

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FUJI POWER MOSFET

Super J MOS® S2 series

N-Channel enhancement mode power MOSFET

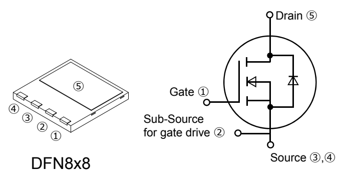
Features

Pb-free lead terminal
RoHS compliant
Halogen-free molding compound
MSL:1, Reflow available

Applications

For switching

Package and Internal circuit chart



DFN8x8
(Out view: see to 7/8 page)

Absolute Maximum Ratings at T_C=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	V_{GS}=-30V
Continuous Drain Current	I_D	42.3	A	T_C=25°C Note*1,2
		26.8	A	T_C=100°C Note*1,2
Pulsed Drain Current	I_{DP}	125.6	A	Note *2
Gate-Source Voltage	V_{GS}	±30	V	
Non-Repetitive Maximum Avalanche Current	I_{AS}	5.5	A	Note *3
Non-Repetitive Maximum Avalanche Energy	E_{AS}	964.2	mJ	Note *4
Maximum MOSFET dv/dt	dv_{DS}/dt	50	V/ns	$V_{DS}\leq$ 600V
Continuous Diode Forward Current	I_{DR}	42.3	A	T_C=25°C Note*1,2
		26.8	A	T_C=100°C Note*1,2
Pulsed Diode Forward Current	I_{DRP}	125.6	A	Note *2
Peak Diode Recovery dv/dt	dv/dt	30	V/ns	Note *5
Peak Diode Recovery -di$_{DR}$/dt	$-di_{DR}/dt$	100	A/μs	Note *6
Maximum Power Dissipation	P_{tot}	263	W	T_C=25°C
		2.78	W	T_a=25°C
Operating Channel Temperature	T_{ch}	150	°C	
Storage Temperature	T_{stg}	-55 to +150	°C	

Note *1 : Maximum duty cycle D=0.53
Note *2 : Limited by maximum channel temperature.
Note *3 : $T_{ch}\leq$ 150 °C, See Figure 1 and 2.
Note *4 : Starting T_{ch} = 25 °C, I_{AS} = 3 A, L = 165 mH, V_{DD} = 60 V, R_G = 50 Ω, See Figure 1 and 2.
E_{AS} limited by maximum channel temperature and avalanche current.
Note *5 : $I_{DR}\leq$32.8 A , $-di_{DR}/dt\leq$ 100 A/μs, $V_{DS\ peak}\leq$ 600 V, $T_{ch}\leq$ 150 °C.
Note *6 : $I_{DR}\leq$32.8 A , $dv/dt\leq$ 30 V/ns, $V_{DS\ peak}\leq$ 600 V, $T_{ch}\leq$ 150 °C.

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Electrical Characteristics at T_c=25°C (unless otherwise specified)

• Static characteristics

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V I_D = 250 μA		600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 5.6 mA		3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V V_{GS} = 0 V	T_{ch} = 25 °C	-	-	25	μA
		V_{DS} = 480 V V_{GS} = 0 V	T_{ch} = 125 °C	-	-	-	
Gate-Source Leakage Current	I_{GSS}	V_{DS} = 0 V V_{GS} = ± 30 V		-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V I_D = 9.3 A		-	0.083	0.093	Ω
Gate resistance	r_g	f = 1 MHz, open drain		-	7.2	-	Ω

• Dynamic characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 18.6 A	7.5	30	-	S
Input Capacitance	C_{iss}	V_{DS} = 400 V V_{GS} = 0 V f = 250 kHz	-	1950	-	pF
Output Capacitance	C_{oss}		-	67	-	
Reverse Transfer Capacitance	C_{rss}		-	8.6	-	
Effective output capacitance, energy related (Note *7)	$C_{o(er)}$	V_{DS} = 0…400 V V_{GS} = 0 V	-	160	-	
Effective output capacitance, time related (Note *8)	$C_{o(tr)}$	V_{DS} = 0…400 V V_{GS} = 0 V I_D = constant	-	660	-	
Turn-On Time	$t_{d(on)}$	V_{DD} = 400 V, V_{GS} = 10 V I_D = 18.6 A, R_G = 18 Ω See Figure 3 and 4	-	31	-	ns
	t_r		-	20	-	
Turn-Off Time	$t_{d(off)}$		-	247	-	
	t_f		-	23	-	
Total Gate Charge	Q_G	V_{DD} = 400 V, V_{GS} = 10 V I_D = 37.1 A See Figure 5	-	93	-	nC
Gate-Source Charge	Q_{GS}		-	31	-	
Gate-Drain Charge	Q_{GD}		-	43	-	

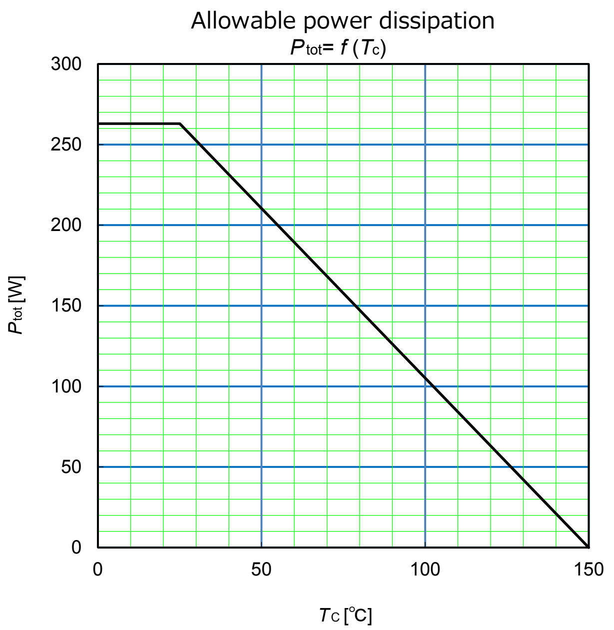
Note *7 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.
Note *8 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400 V.

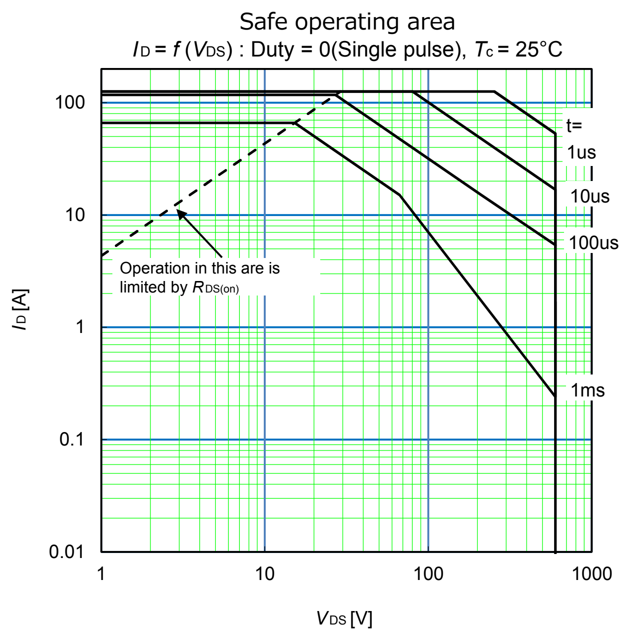
• Reverse diode characteristics

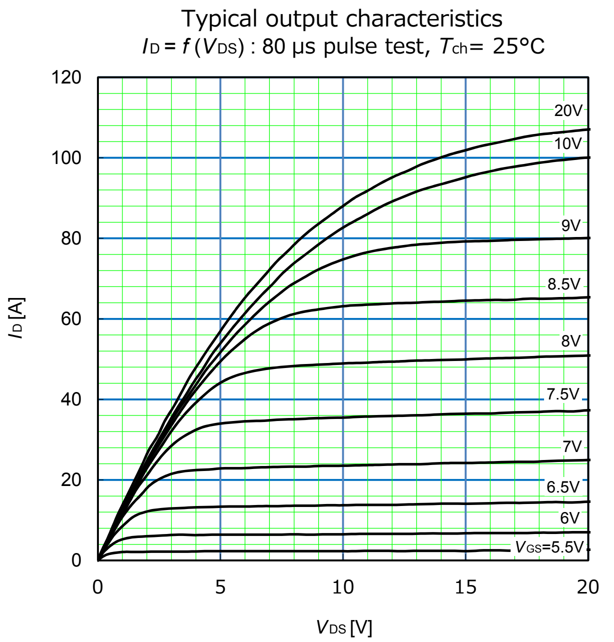
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	V_{DSR}	I_{DR} = 37.1 A, V_{GS} = 0 V T_{ch} = 25 °C	-	1.00	1.35	V
Reverse Recovery Time	t_{rr}	V_{DD} = 400 V I_{DR} = 37.1 A V_{GS} = 0 V -di_{DR}/dt = 100 A/μs T_{ch} = 25 °C See Figure 6 and 7	-	190	-	ns
Reverse Recovery Charge	Q_{rr}		-	1.6	-	μC
Peak Reverse Recovery Current	I_{rrm}		-	16	-	A

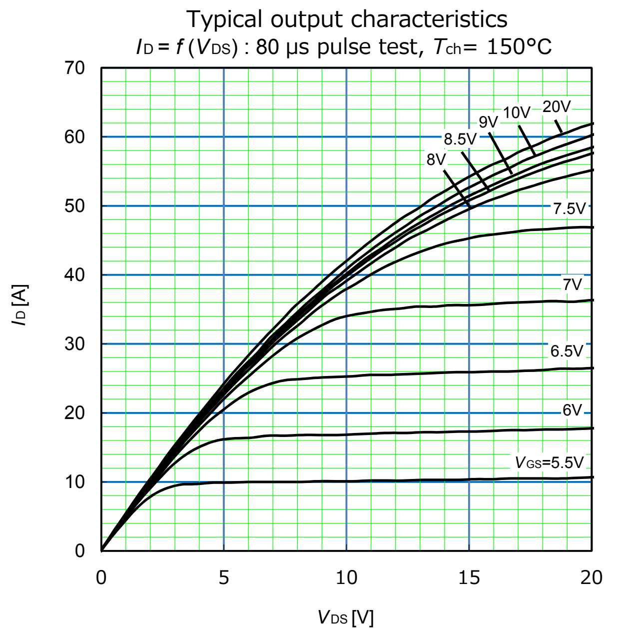
Thermal Resistance

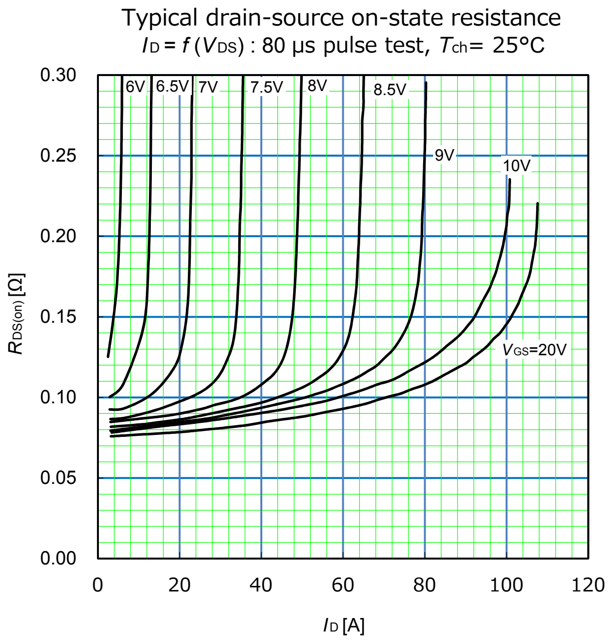
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance, Channel – Ambient	$R_{th(ch-a)}$	Device mounted on PCB (FR4) Size: 40mm*40mm*1.5mm with 6cm² copper area (one layer, 70μm thickness) for drain connection and cooling.	-	-	45	°C/W
Thermal Resistance, Channel – Case	$R_{th(ch-c)}$		-	-	0.475	°C/W

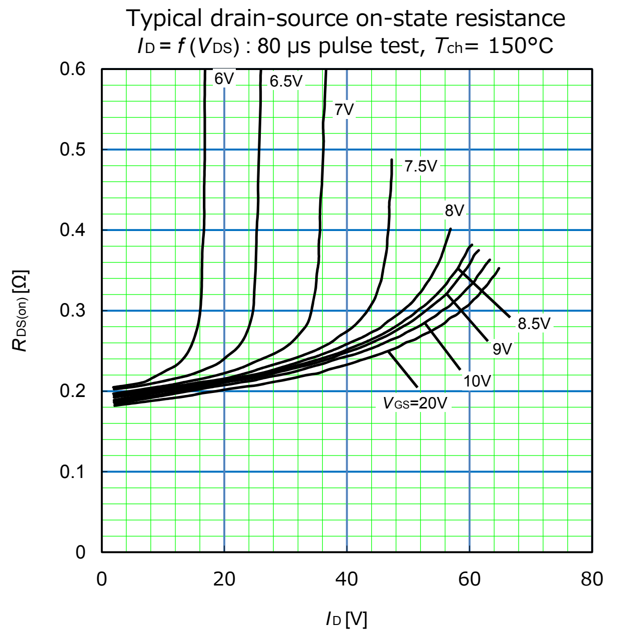

Allowable power dissipation
Ptot= f (Tc)
Ptot [W]
Tc [℃]


Safe operating area
ID = f (VDS) : Duty = 0(Single pulse), Tc = 25°C
t=
1us
10us
100us
1ms
Operation in this are is limited by RDS(on)
ID [A]
VDS [V]

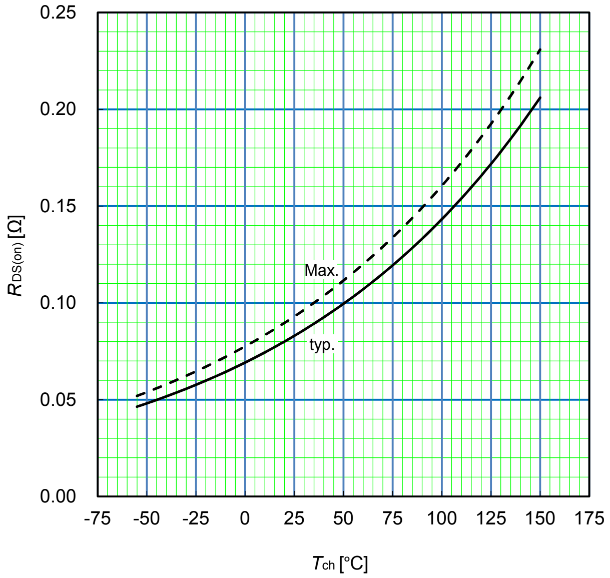

Typical output characteristics
ID = f (VDS) : 80 μs pulse test, Tch= 25°C
20V
10V
9V
8.5V
8V
7.5V
7V
6.5V
6V
VGS=5.5V
ID [A]
VDS [V]


Typical output characteristics
ID = f (VDS) : 80 μs pulse test, Tch= 150°C
20V
10V
9V
8.5V
8V
7.5V
7V
6.5V
6V
VGS=5.5V
ID [A]
VDS [V]

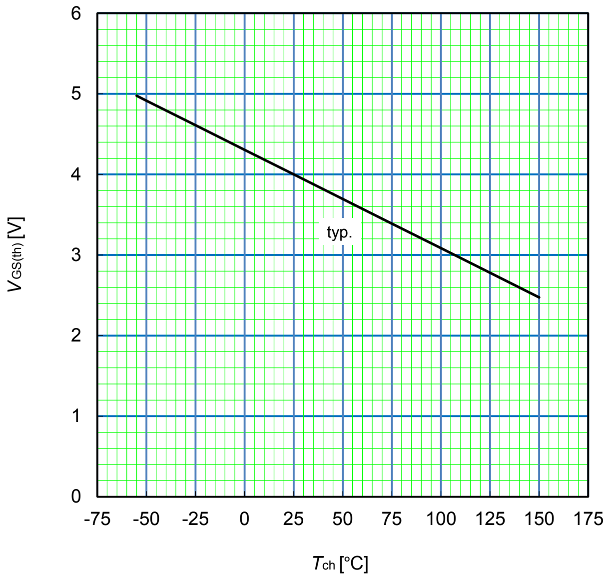

Typical drain-source on-state resistance
ID = f (VDS) : 80 μs pulse test, Tch= 25°C
6V
6.5V
7V
7.5V
8V
8.5V
9V
10V
VGS=20V
RDS(on) [Ω]
ID [A]


Typical drain-source on-state resistance
ID = f (VDS) : 80 μs pulse test, Tch= 150°C
6V
6.5V
7V
7.5V
8V
8.5V
9V
10V
VGS=20V
RDS(on) [Ω]
ID [V]

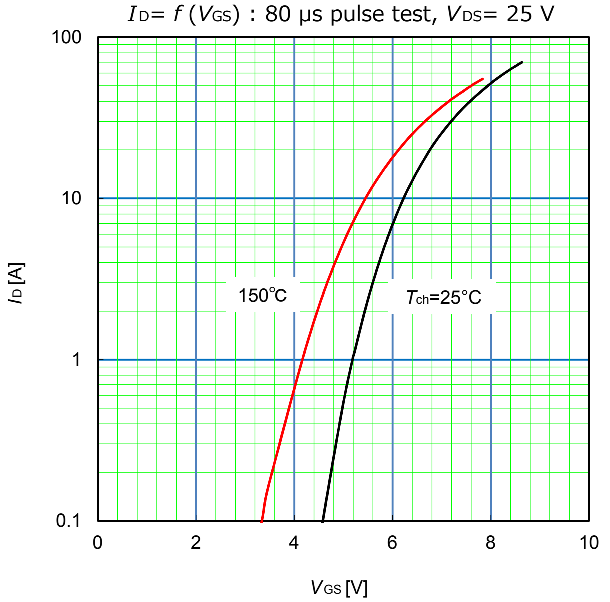
Drain-source on-state resistance
$R_{DS(on)} = f(T_{ch})$: I_D = 18.6 A, V_{GS} = 10 V



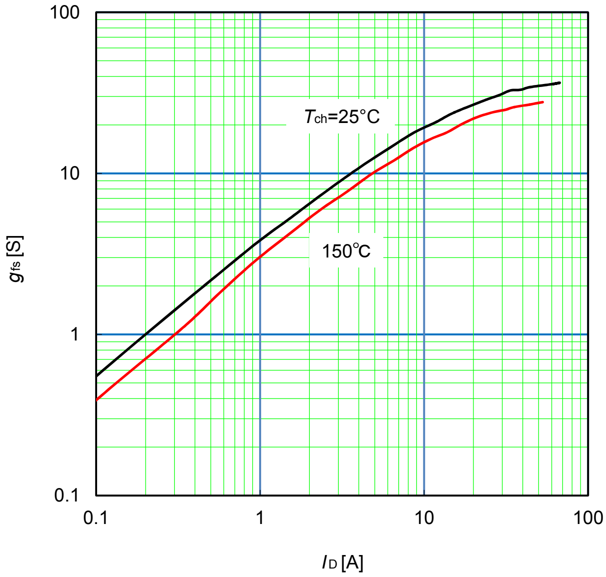
Gate threshold voltage
$V_{GS(th)} = f(T_{ch})$: $V_{DS} = V_{GS}$, I_D = 5.6 mA



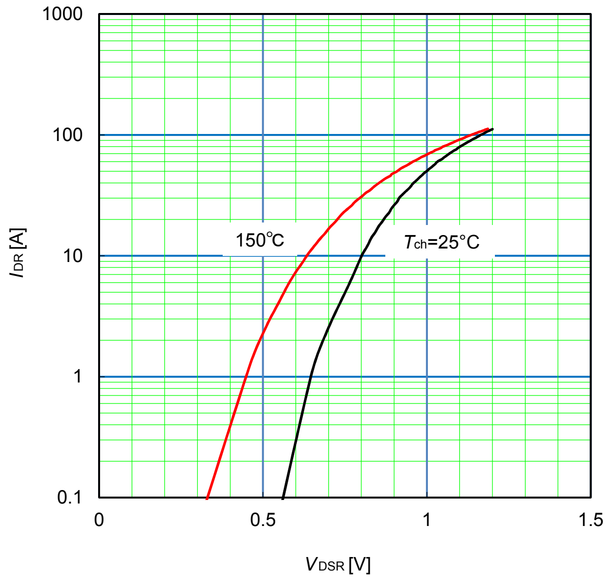
Typical transfer characteristic
$I_D = f(V_{GS})$: 80 μs pulse test, V_{DS} = 25 V



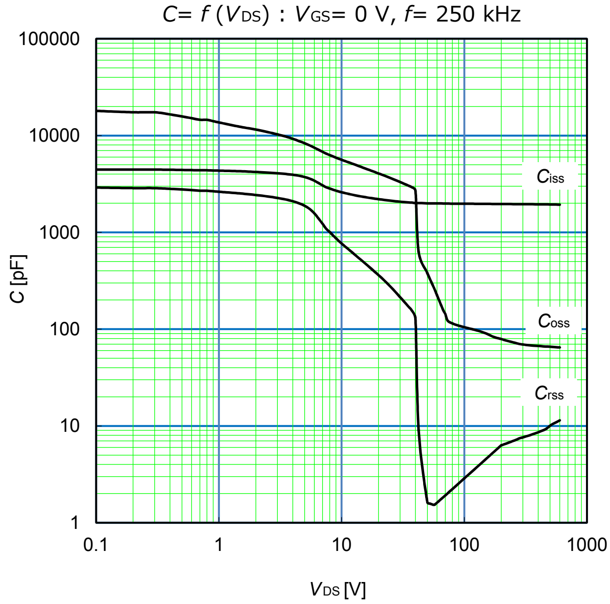
Typical transconductance
$g_{fs} = f(I_D)$: 80 μs pulse test, V_{DS} = 25 V



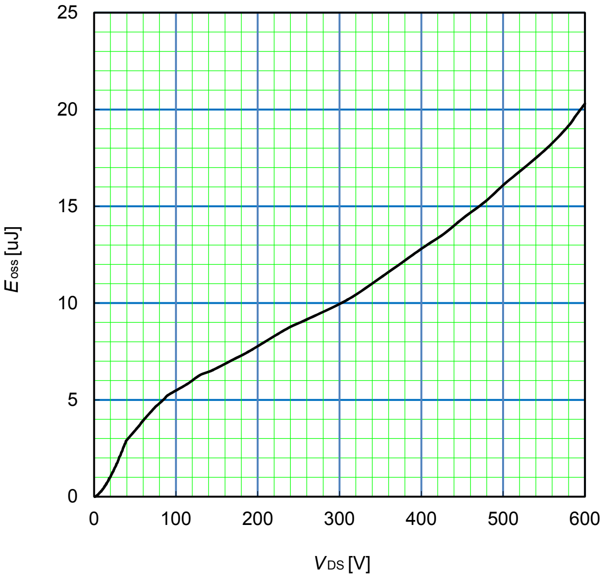
Typical forward characteristics of reverse diode
$I_{DR} = f(V_{DSR})$: 80 μs pulse test



Typical capacitance
$C = f(V_{DS})$: V_{GS} = 0 V, f = 250 kHz

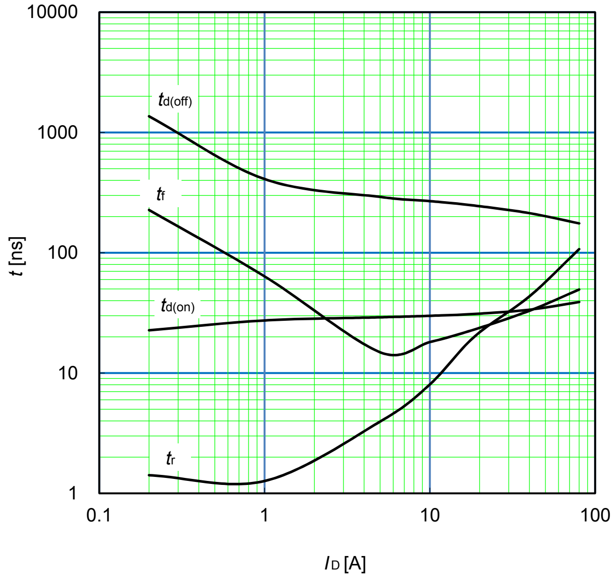


Typical C_{oss} stored energy



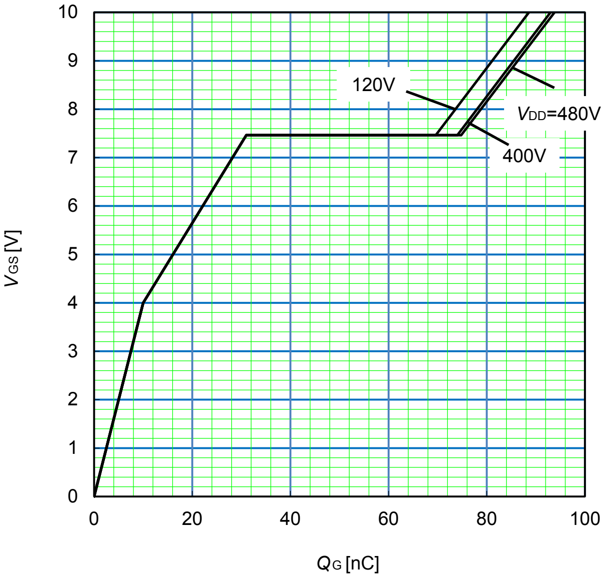
Typical switching times vs. I_D

$t= f(I_D)$: V_{DD}= 400 V, V_{GS}= 10 V/0 V, R_G= 18 Ω, T_{ch}= 25°C



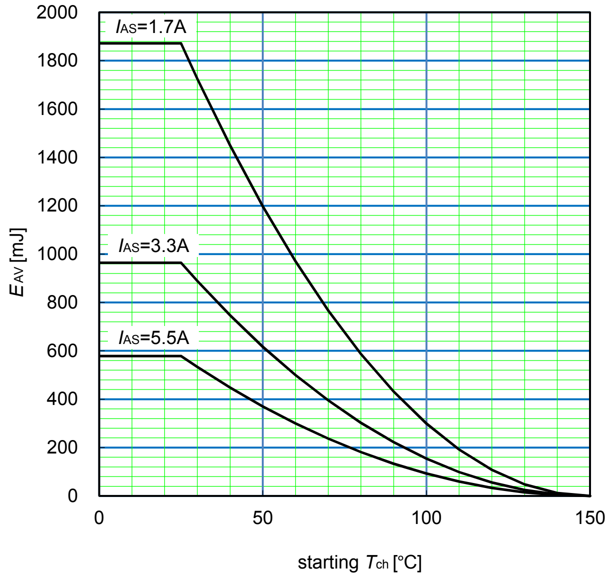
Typical gate charge

$V_{GS}= f(Q_G)$: I_D= 37.1 A, T_{ch}= 25°C



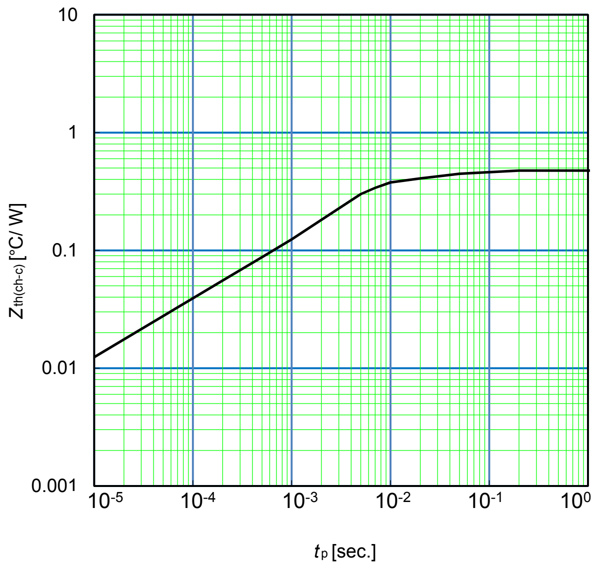
Maximum Avalanche Energy

$E_{AV} = f$ (starting T_{ch}) : V_{DD}= 60 V, I_{AV}≤5.5 A



Transient Thermal Impedance

$Z_{th(ch-c)}= f(t)$: D= 0



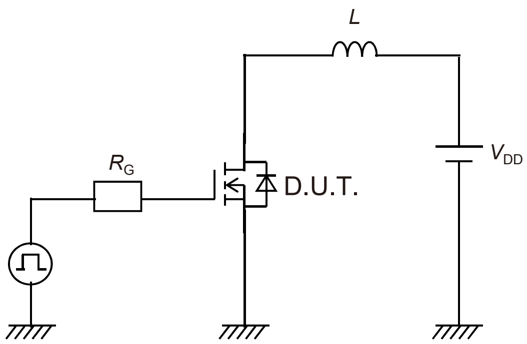


Figure 1. Unclamped inductive load test circuit

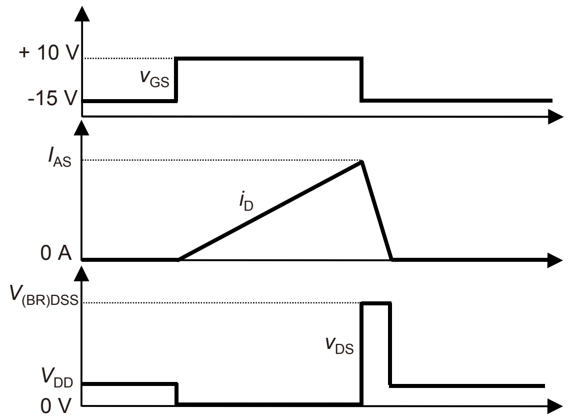


Figure 2. Unclamped inductive waveform

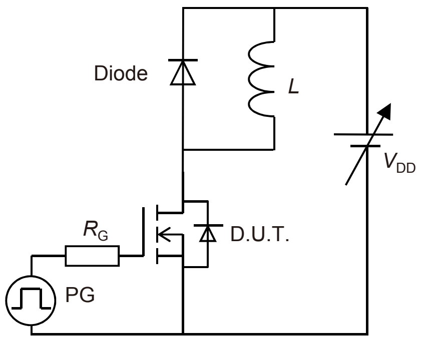


Figure 3. Switching test circuit

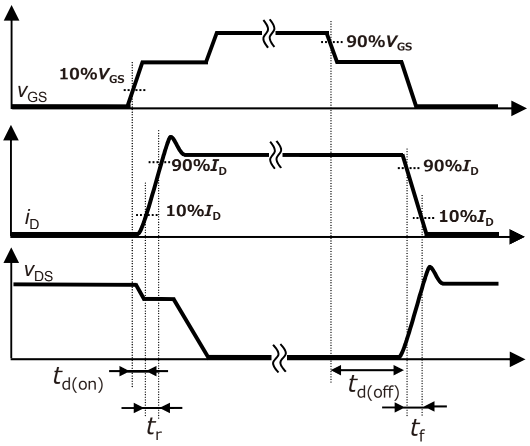


Figure 4. Switching times waveform

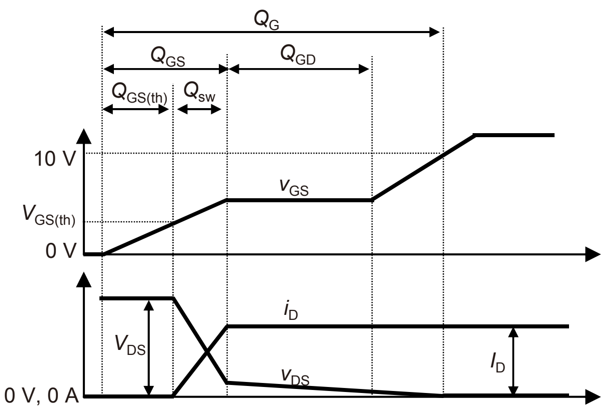
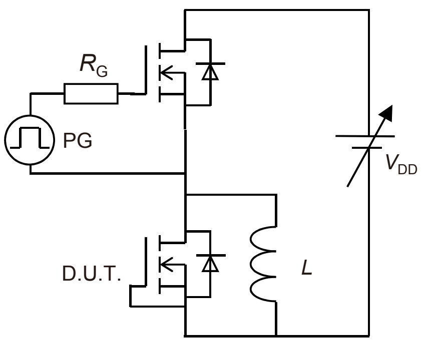
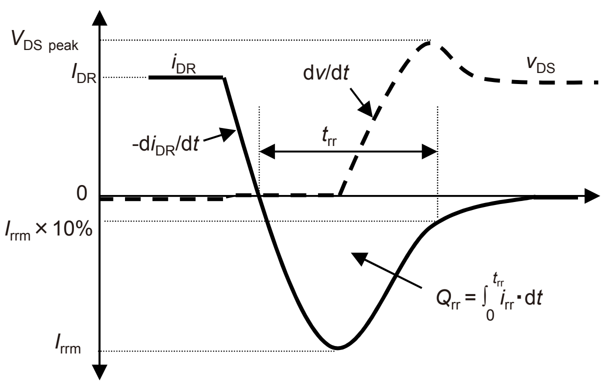
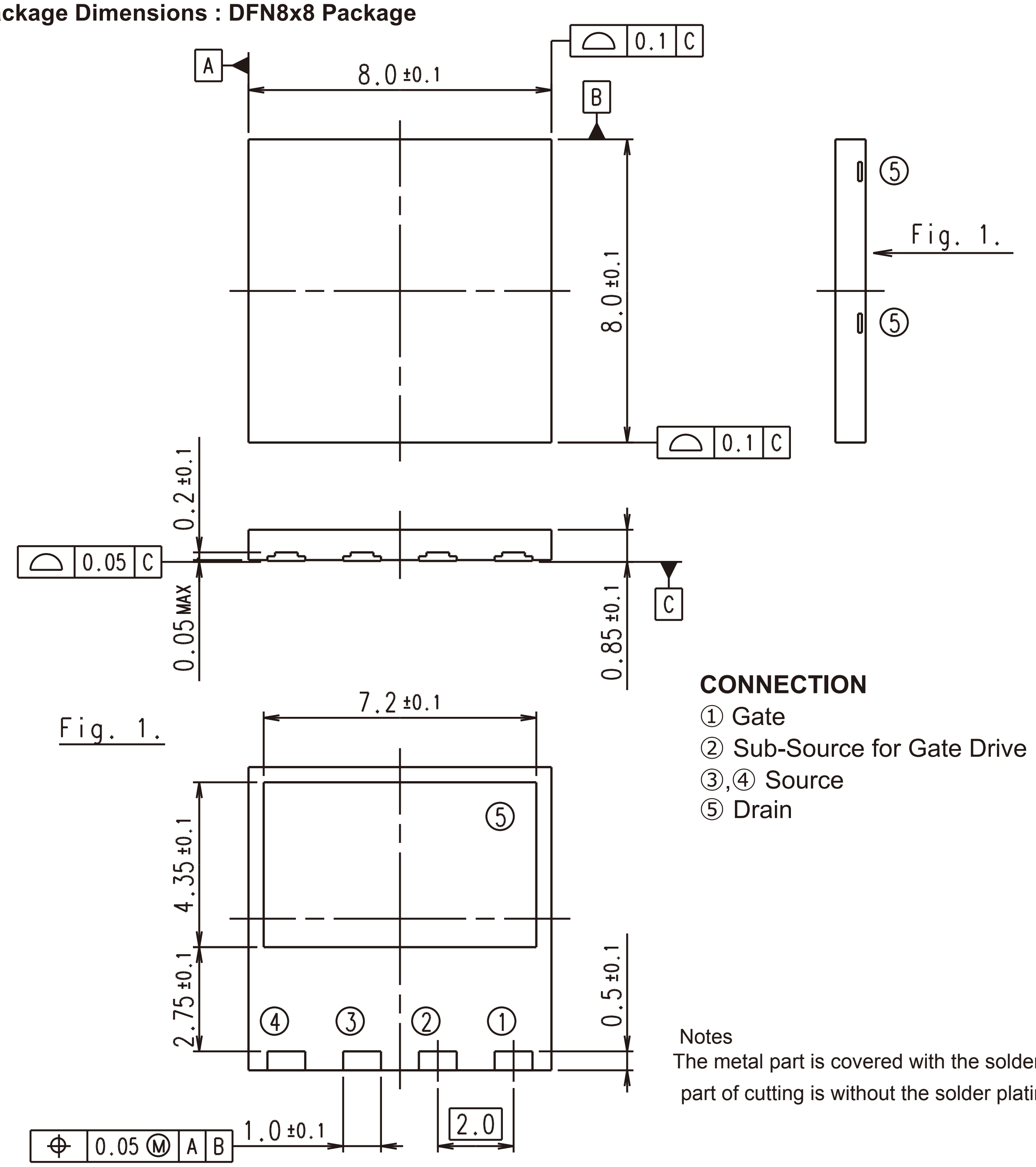


Figure 5. Gate charge waveform





Package Dimensions : DFN8x8 Package

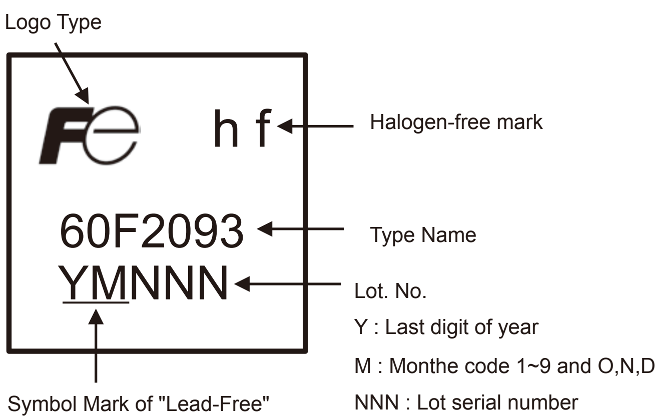


CONNECTION

① Gate
② Sub-Source for Gate Drive
③,④ Source
⑤ Drain

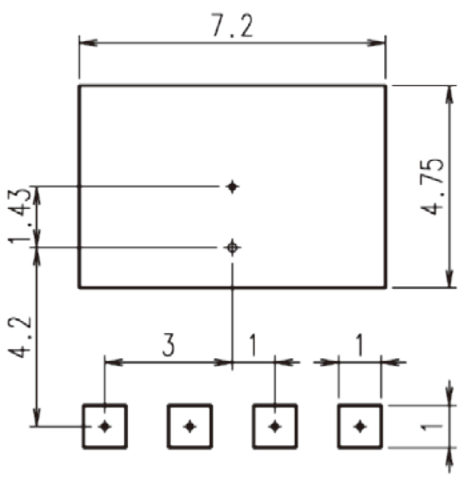
Notes
The metal part is covered with the solder plating, part of cutting is without the solder plating.

Marking



* The font (font type,size) and the trademark-size might be actually different.

Recommended footprint



WARNING

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• Machine tools • Audiovisual equipment • Electrical home appliances • Personal equipment • Industrial robots etc.

5. If you need to use a product in this Catalog for equipment requiring higher reliability than normal, such as for the equipment listed below, it is imperative to contact Fuji Electric Co., Ltd. to obtain prior approval. When using these products for such equipment, take adequate measures such as a backup system to prevent the equipment from malfunctioning even if a Fuji's product incorporated in the equipment becomes faulty.
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• Traffic-signal control equipment • Gas leakage detectors with an auto-shut-off feature
• Emergency equipment for responding to disasters and anti-burglary devices • Safety devices
• Medical equipment

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• Submarine repeater equipment

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